



Memory Stick PRO Host Interface

Reference Design

FPGA-RD-02094-1.1

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1. Introduction

Memory Stick PRO was introduced in 2003 as a joint effort between Sony and SanDisk. Memory Stick is a removable Flash memory card which is used as storage media for portable devices such as digital cameras, digital music players, PDAs, cellular phones, etc. Memory Stick PRO has a maximum data transfer of 19.7 Mbytes/s and a theoretical maximum capacity of up to 32 GB.

The WISHBONE Bus interface is a free, open-source standard that is gaining popularity in digital systems that require the use of IP cores. This bus interface encourages IP reuse by defining a common interface among IP cores. This, in turn, provides portability for the system, speeds up time to market, and reduces the cost of the end product.

This design is targeted to provide an interface between Memory Stick PRO and its Host Controller. This design can be used in applications where a WISHBONE-compliant Host Controller has the necessary drivers needs to communicate with the Memory Stick PRO. The Host Interface acts as a bridge and takes care of the various bus state transitions.

2. Memory Stick PRO Host Interface

The Host Interface handles the Bus State and generates all necessary signals for the transfer. The Host Controller and the Memory Stick PRO communicate through two interfaces:

1. Serial interface protocol to transfer data on three signal lines: SCLK, BS, SDIO.
2. Parallel interface protocol to transfer data on six signal lines: SCLK, BS, DATA [3:0].

The Host accesses the registers and data buffer of the Memory Stick PRO with a group of commands called Transfer Protocol Commands (TPC). When the Memory Stick PRO is turned ON, it operates in Serial Interface mode and can be switched to Parallel Interface mode with a TPC and vice-versa. The Host Controller accesses the register set of the host interface through the WISHBONE bus.

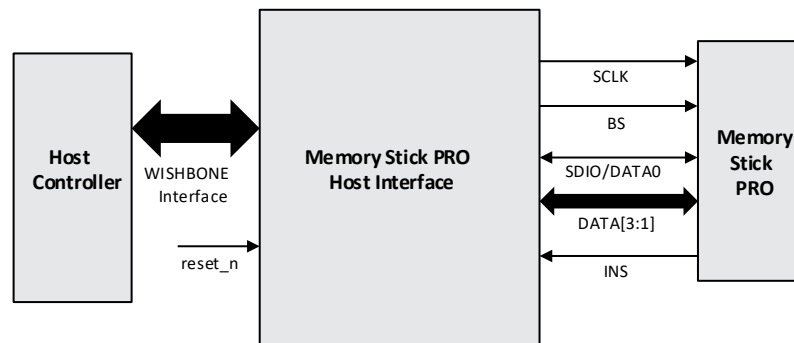


Figure 2.1. Memory Stick PRO Host Interface Block Diagram

3. Port Descriptions

Table 3.1. Port Descriptions

Port	I/O	Width	Description
SCLK	O	1	Clock signal to the Memory Stick PRO
BS	O	1	Bus state signal
SDIO/DATA[0]	I/O	1	Serial Data Signal/ Bit0 of parallel data signal
DATA[3:1]	I/O	3	Parallel data signal
INS	I	1	Insert/removal detect signal. This signal goes low when Memory Stick PRO is inserted into the socket.
Reset_n	I	1	Hardware reset signal. Active low signal.
WB_CLK_I	I	1	Positive edge clock used by WISHBONE interface registers. This is the master clock for the design.
WB_CYC_I	I	1	Active-high signal, asserted by the WISHBONE master, indicates a valid bus cycle is present on the bus. In a multiple-master configuration, this signal serves as a bus request by a WISHBONE master.
WB_STB_I	I	1	Active-high strobe, input signal, indicating the WISHBONE slave is the target for the current transaction on the bus. The WISHBONE slave asserts an acknowledgment in response to the assertion of the strobe.
WB_WE_I	I	1	Level sensitive write/read control signal. Low indicates a read operation, and high indicates a write operation.
WB_ADR_I	I	8	Address used to select a specific register
WB_DAT_I	I	8	Data path used to write a byte of data to a specific register.
WB_DAT_O	O	8	Data path used to read a byte of data from a specific register.
WB_ACK_O	O	1	Active-high, transfer acknowledge signal asserted by the WISHBONE slave interface, indicating the requested transfer is acknowledged.
WB_INT_O	O	1	Interrupt used to specify the completion of a transfer cycle.

4. Architecture

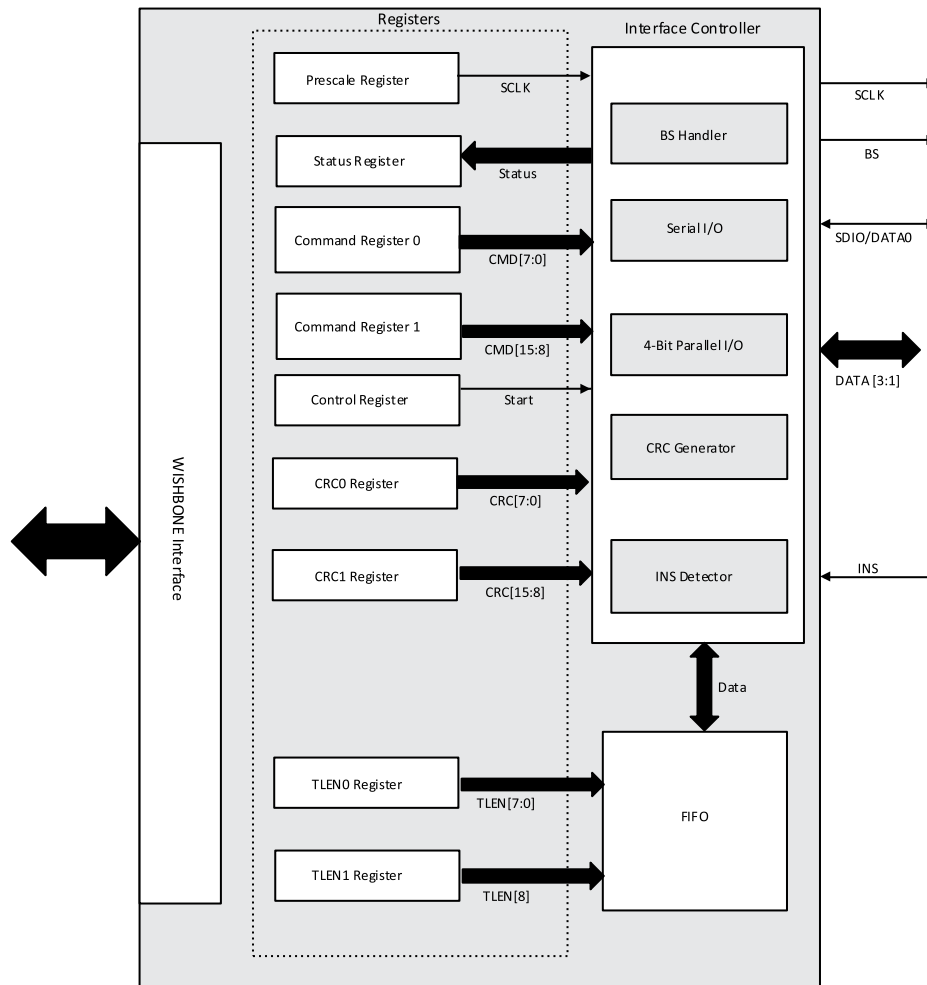


Figure 4.1. Design Architecture

4.1. Interface Controller Description

BS Handler

The Bus State (BS) Handler generates the necessary BS signal which determines the direction of data flow and the type of data being transferred.

Serial I/O

The Serial I/O Blocks receive parallel data and transmit data serially following the clock signal SCLK generated by the Clock Generator. The Most Significant bit (MSB) is transferred first. Data is transmitted at the falling edge of SCLK and latched at the rising edge of SCLK.

Parallel I/O

The Parallel I/O Block receives parallel data and transfers four bits per clock edge. The Most Significant (MSB) four bits are transferred first followed by the Least Significant (LSB) four bits.

CRC Generator

Generates the CRC code from the polynomial and data bytes to be transmitted or checked.

Note: the standard CRC format is assumed to be CRC16.

INS Detector

Monitors the INS pin for a 0 or 1. The Memory Stick PRO is inserted if the level is 0, otherwise it is removed.

5. Register Set

Table 5.1. Register Set

Register	Address	R/W	Value at Reset
Pre Scale Register	0x00	W	0x01
Status Register	0x01	R	0x01
Command Register0	0x02	W	0x00
Command Register1	0x03	W	0x00
Control Register	0x04	W	0x00
CRC0	0x05	W	0x00
CRC1	0x06	W	0x00
TLEN0	0x07	W	0x00
TLEN1	0x08	W	0x00
FIFO Base	0x09	R/W	N/A

5.1. Register Set Description

Prescale Register

The clock divider value is stored in the prescale register. The SCLK is generated from the WISHBONE clock and is equal to $WB_CLK_I/(2 \times \text{prescale value})$. The valid prescale values are 1, 2, 4, 8, 16, 32, 64, 128 and 256. The default value is 1. The maximum SCLK frequency can go up to 20 MHz. The user should make sure the generated clock does not exceed the maximum clock specifications.

Status Register

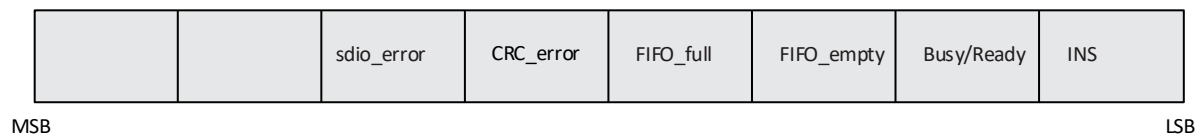


Figure 5.1. Status Register

INS	R	Memory Stick PRO Insert/Removal detect bit 0- Inserted 1- Removed
Busy/Ready	R	Host Controller busy/ready bit 1- Busy with previous transmission 0- Ready for next transmission
FIFO_Empty	R	Set when the FIFO is empty
FIFO_Full	R	Set when the FIFO is full
CRC_error	R	CRC error detection bit
sdio_error	R	Error during data transfer from Host Interface to Memory Stick PRO

Command Register0

First byte of the TPC command which has to be transmitted to the Memory Stick PRO is loaded in this register.

Command Register1

Second byte of the TPC command which has to be transmitted to the Memory Stick PRO is loaded in this register.
Note: Since the length of the TPC is unknown, a 16-bit register is used for this purpose. During implementation, the length of the TPC will be parameterized so that the user can define the actual length of the TPC.

Control Register

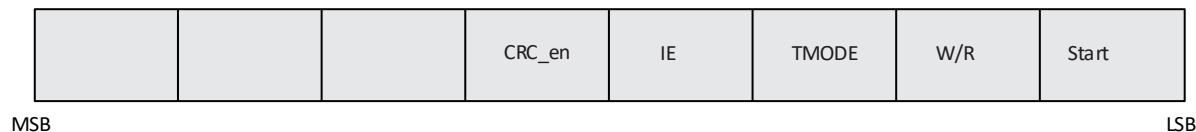


Figure 5.2. Control Register

Start	W	Set to 1 to start the transfer once the command and data registers are loaded.
W/R	W	TPC write or read operation. 0- Read 1- Write
TMODE	W	Indicates the data transmit mode 0- Serial 1- Parallel The default value is 0
IE	W	Interrupt enable bit
CRC_EN	W	Enable CRC for the data being transferred

CRC0

First byte of the CRC polynomial is loaded in this register.

CRC1

Second byte of the CRC polynomial is loaded in this register.

TLEN0

This register stores the number of bytes to be transferred. First byte of the number of bytes to be transferred is stored in this register.

TLEN1

Second byte of the number of bytes to be transferred is stored in this register.

FIFO

The Transfer FIFO is 512 bytes deep. Data to be written or read from Memory Stick PRO is loaded in this FIFO. Data loaded in first is sent out first. FIFO_EMPTY bit in the status register is set as soon as all the data is read by the Host Controller or transmitted to Memory Stick PRO. FIFO_FULL bit is set as soon as the FIFO is full.

5.2. Interfaces

The Host Controller always initiates the communication. The two interfaces used to communicate with a Memory Stick PRO are described below.

Serial Interface

Three signals, BS, SCLK and SDIO, are used during serial interface communication between the Host Controller and Memory Stick PRO. Here, the MSB (Most Significant Bit) of TPC or data will be transferred first.

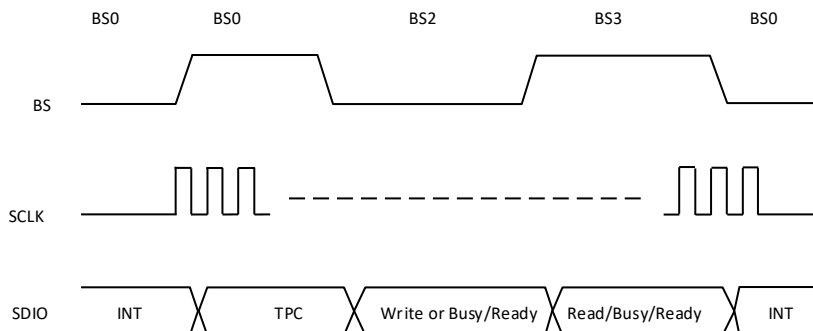


Figure 5.3. Serial Interface

Parallel Interface

Six signals, BS, SCLK and DATA [3:0], are used during serial interface communication between the Host Controller and Memory Stick PRO. The upper four bits of a byte will be transferred first followed by the lower four bits.

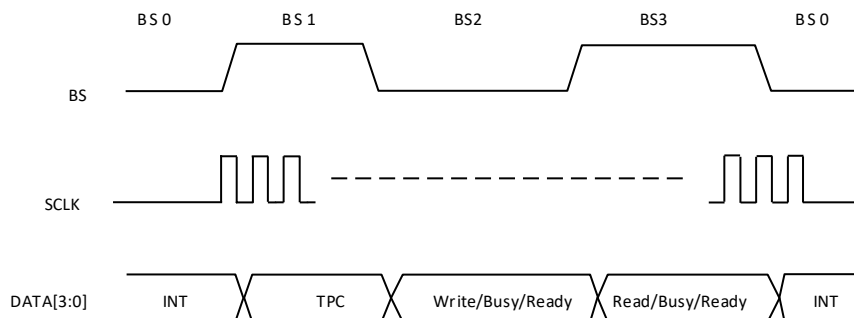


Figure 5.4. Parallel Interface

6. Bus State

The Bus State signal governs the serial/parallel communication in which it transitions from BS0 to BS3 in one cycle. Each communication must be completed within one cycle.

Table 6.1. Bus State

State	BS	Explanation
BS0	Low	Idle state. BS signal is kept low. No actual data transfer occurs.
BS1	High	TPC transfer from Host to Memory Stick PRO.
BS2	Low	BS signal is held low. Depending on the TPC, this state is classified as: Write: The data to be written into the Memory Stick PRO is transferred. Read: This is a handshake state where the Host waits for a RDY signal from the Memory Stick PRO.
BS3	High	BS signal is held high. Depending on the TPC, this state is classified as: Write: This is a handshake state where the Host waits for a RDY signal from the Memory Stick PRO. Read: Data is transferred from Memory Stick PRO to the Host Controller.

7. Operational Sequence

This sequence describes the flow followed by the Host Controller to load registers in the Host Interface module for Memory Stick PRO read or write processes.

Initialization:

1. Set the proper clock Prescale value.
2. Set the IE bit if Interrupt is used.
3. Load the CRC0 and CRC1 registers with a 16-bit CRC polynomial.

Write operation:

1. Load the TPC register.
2. Set the TLEN register.
3. Transfer the data to be written into the FIFO.
4. Set the R/W, CRC_en and Start bits of the Control register to 1.
5. Wait for interrupt and check that the status register for the Busy/Ready bit is set to 0.

Read operation:

1. Load the TPC register.
2. Set the TLEN register.
3. Set the R/W bit to 0 and the Start bit to 1. Set CRC_en to 1 to enable the CRC check.
4. Wait for the interrupt signal if IE bit is enabled or continuously poll the Status register Busy/Ready bit for 0.
5. Busy/Ready bit is set to 0 once all the bytes as set in the TLEN are read from the Memory Stick PRO.
6. Read out data in FIFO until FIFO empty.

Notes:

- Registers TPC and TLEN will be cleared after each BS cycle.
- Upon hardware reset, all the registers will be set to their default values and FIFO will be emptied.
- If Memory Stick PRO is removed (INS goes high) while a transfer is in progress all registers will be reset and FIFO will be emptied.

8. HDL Simulation and Verification

Host Interface Registers Loaded by the Host Controller to Perform a Write Operation to Memory Stick PRO

Figure 8.1. illustrates the data transfer from Host Controller to the Host Interface in order to initiate a write operation to the Memory Stick PRO. 30 bytes of data are transferred in this example.

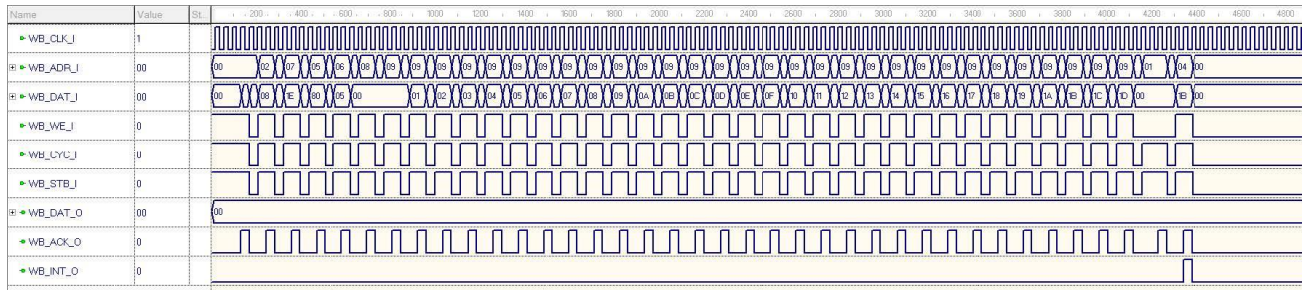


Figure 8.1. Write Operation

Host Interface Registers Loaded by the Host Controller to Perform a Read Operation from Memory Stick PRO

Figure 8.2. illustrates the data transfer from Host Controller to the Host Interface in order to initiate a read operation to the Memory Stick PRO

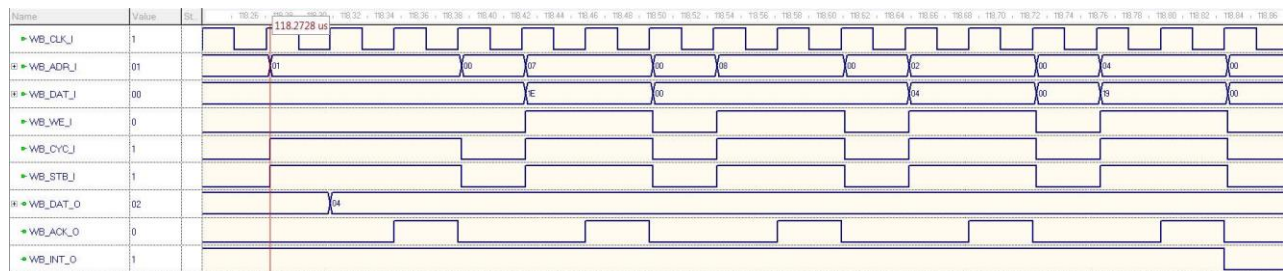


Figure 8.2. Read Operation

Data Read Back from the Host Interface by the Host Controller

30 bytes of data which were written to the Memory Stick PRO previously is read back.

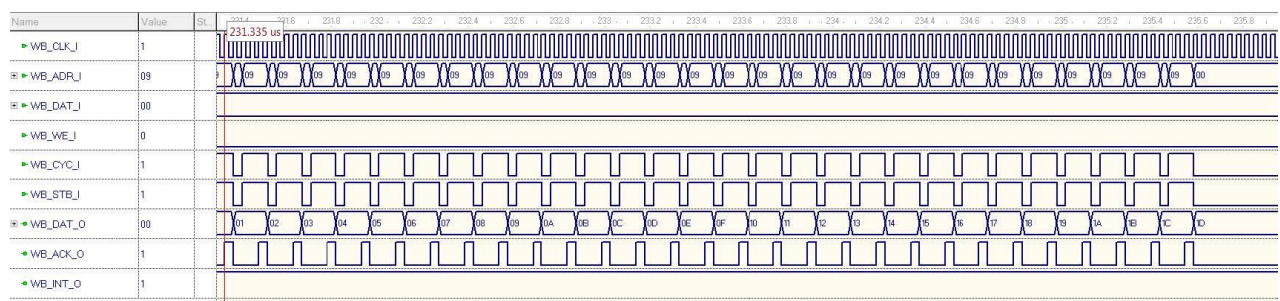


Figure 8.3. Data Read Back

9. Implementation

This design is implemented in Verilog and VHDL. When using this design in a different device, density, speed, or grade, performance and utilization may vary. Default settings are used during the fitting of the design.

Table 9.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f _{MAX} (MHz)	I/Os	Architecture Resources
MachXO2™*	Verilog	-6	458	>50	38	1 EBR

***Note:** Performance and utilization characteristics are generated using LCMXO2-640HC-6MG132C with Lattice Diamond™ 1.2 design software.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, December 2019

Section	Change Summary
All	- Changed document number from RD1109 to FPGA-RD-02094. - Updated document template.
Disclaimers	Added this section.

Revision 1.0, April 2011

Section	Change Summary
All	Initial release.



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