Sub-LVDS-to-Parallel Sensor Bridge

Reference Design

FPGA-RD-02147-1.8

January 2020

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1. Introduction

Sony introduced the IMX036 and IMX136 sensors to support resolutions up to 1080P60 and 1080p120 respectively. A traditional CMOS parallel interface could no longer handle the bandwidth requirements of these sensors. To support the higher resolutions and frame rates, Sony utilizes a parallel DDR sub-LVDS interface. This 10/12-bit parallel sub-LVDS DDR interface can operate up to 1080p60 at 148.5 Mbps on the IMX036 and 1080p120 at 297 Mbps on the IMX136. The Lattice Sub-LVDS-to-Parallel Sensor Bridge converts the low voltage sub-LVDS DDR output of the IMX036 and IMX136 to a standard CMOS parallel interface.

The IMX036 is capable of outputting a 3.27 megapixel image. The IMX136 is capable of 2.3 megapixel image. For more technical details regarding the image sensor, please contact Sony. This reference design does the following:

1. Converts parallel data from the LVDS DDR input to SDR data (LVCMOS interface) and generates the output clock (phase adjustable) at twice the frequency of the input clock with a PLL.
2. Extracts EAV and SAV from the SDR data and generates xhs and xvs. All valid and invalid SAV/EAV sync codes are detected and used to generate these active video control lines.

Figure 1.1 shows the block diagram for this design.

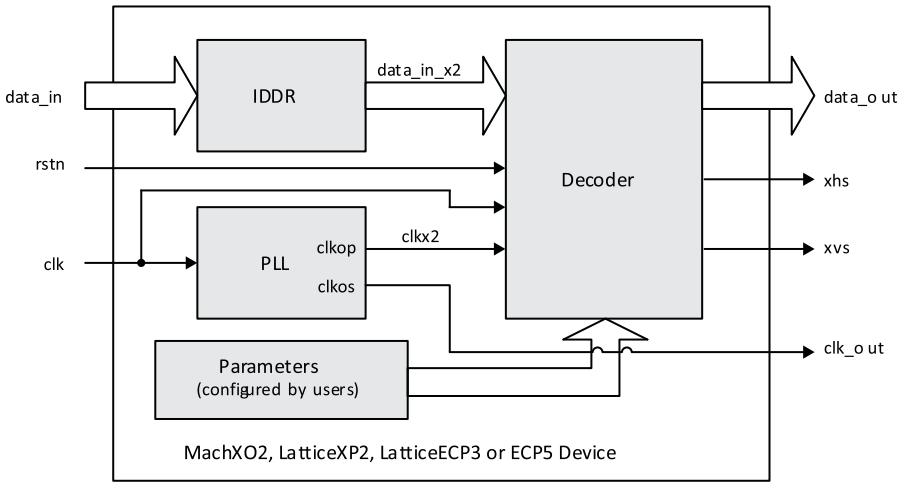

Figure 1.1. Sub-LVDS-to-Parallel Sensor Bridge Block Diagram

The decoder contains the function of the second item listed above and is compiled to the NGO. The device selected can be a MachXO2™, LatticeXP2™, LatticeECP3™, or ECP5™ device.

The phase of the output clock can be adjusted for the next device to sample the data correctly.

The width of input data can be 10 bits or 12 bits, data_in[11:2] is valid in 10-bit mode.

The drive mode can be configured to the following modes: QXGA, WUXGA, 1080p-HD, 720p-HD, 2x2 addition and 3x3 addition. This will affect the number of blank lines after the falling edge of XVS, the number of total horizontal pixels and total vertical lines (sees Table 1.1 and Table 1.2). If the parameter sim is set to '1', the number is decreased for reducing the time of simulation. Users have the option of creating additional modes with modification to the generics and source at the top level which drive the NGO.

Table 1.1. Drive Modes for the Sony IMX036

Drive Mode (2 Bits)	Analog-to-Digital Conversion	Number of Pre-blanking Lines	Frame Rate (Frame/s)	Data Rate (Mpix/s)	Number of Recording Pixels		Number of Output Vertical Lines and Horizontal Pixels	
					Horizontal	Vertical	Horizontal	Vertical
0 (QXGA)	10	12	60.18	216	2048	1536	2232	1608
	12	12	15.05	54				
1 (1080p-HD)	10	12	60.00	148.5	2048	1080	2200	1125
	12	12	30.00	74.25				
2 (2x2 addition)	10	6	60.18	54	1024	768	1116	804
3 (3x3 addition)	10	4	60.18	24	682	512	744	536

Table 1.2. Drive Modes for the Sony IMX136

Drive Mode (2 Bits)	Analog-to-Digital Conversion	Number of Pre-blanking Lines	Frame Rate (Frame/s)	Data Rate (Mpix/s)	Number of Recording Pixels		Number of Output Vertical Lines and Horizontal Pixels	
					Horizontal	Vertical	Horizontal	Vertical
4 (1080p-HD)	10/12	8	30	74.25	1920	1080	2200	1125
	10/12	8	60	148.5				
	10	8	120[1]	297[1]				
5 (WUXGA 37.125 MHz INCK)	10/12	8	27	37.125	1920	1200	2200	1250
	10/12	8	54	74.25				
	10	8	108	148.5				
6 (WUXGA 27 MHz INCK)	10/12	8	20	27	1920	1200	2160	1250
	10/12	8	40	54				
	10	8	80	108				
7 (720p-HD)	10/12	8	30	37.125	1280	720	1650	750
	10/12	8	60	74.25				
	10	8	120	148.5				

Note:

1. This may require the removal of the 24-bit to 12-bit parallel bus mux to meet Place and Route I/O timing. The result is a 24-bit parallel bus output at 148.5 MHz. Other options may be available depending on the application. Please consult Lattice Technical Support before attempting to use this mode.

Table 1.3. Sensor Bridge Port Descriptions

Name	Description	Direction
rstn	Reset, active low	Input
clk	Pixel clock	Input
data_in	LVDS DDR input data (10 or 12 bits)	Input
clk_out	Double rate of input clock with phase adjusted	Output
data_out	LVCMOS SDR output data, synchronous with clk_out	Output
xhs	Horizontal sync pulse, active low	Output
xvs	Vertical sync pulse, active low	Output

2. Implementation

Table 2.1. Performance and Resource Utilization[1]

Device Family	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)		I/Os
			clk	clkx2	
ECP5[5]	–8	246 (LSE)	>108	>216	42
	–8	247 (Syn)	>108	>216	42
LatticeECP3[2]	–6	215	>108	>216	42
LatticeXP2[3]	–5	262	>108	>216	42
	–5	267 (Syn)	>108	>216	42
MachXO2[4]	–6	268 (LSE)	>108	>180	42
	–6	268 (Syn)	>108	>180	42

Notes:

1. drive_mode = 0, ad_conv_width = 12.
2. Performance and utilization characteristics are generated using LAE3-17EA-6MG328E, with Lattice Diamond® 3.3 design software. When using this design in a different device, density, speed or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LFXP2-5E-5M132C, with Lattice Diamond 3.3 design software. When using this design in a different device, density, speed or grade, performance and utilization may vary. LSE is not supported in this device.
4. Performance and utilization characteristics are generated using LCMX02-1200HC-6MG132C, with Lattice Diamond 3.3 design software with LSE (Lattice Synthesis Engine). When using this design in a different device, density, speed or grade, performance and utilization may vary.
5. Performance and utilization characteristics are generated using LFE5UM-85F_8MG756C, with the Lattice Diamond 3.3 design software with LSE. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 2.2. I/O Timing Analysis of Sub-LVDS Parallel Input Bus[1, 2]

	Setup	Hold	Setup	Hold	Setup	Hold
ECP5	Speed Grade 6		Speed Grade 7		Speed Grade 8	
	0.169	-0.062	0.165	-0.062	0.162	-0.062
LatticeECP3	Speed Grade 7		Speed Grade 8		Speed Grade 9	
	0.480/0.359	0.351/0.457	0.379/0.480	0.463/0.379	0.405/0.487	0.432/0.351
LatticeXP2	Speed Grade 5		Speed Grade 6		Speed Grade 7	
	-0.765	0.992	-0.666	0.836	-0.566	0.679
MachXO2	Speed Grade 4		Speed Grade 5		Speed Grade 6	
	0.194/0.375	1.097/0.923	0.167/0.348	0.946/0.772	0.132/0.313	0.796/0.622

Notes:

1. Multiple setup/hold numbers indicate that not all I/O timing windows had the same delay across the sub-LVDS parallel bus. The delay primitive can be used to adjust this on a pin-by-pin basis to optimize performance, if needed.
2. I/O numbers to be re-run after pinout is added to constraint file.

Table 2.3. Pinout

Signal	MachXO2 Same Bank[1] 132-Ball csBGA	MachXO2 Multi-Bank 132-Ball csBGA	LatticeXP2 Multi-Bank 132-Ball csBGA
rstn	M1	M1	L2
clk_p	N6	N6	H1
clk_n	P6	P6	H3
Data_in_0_p	M4	B14	F1
Data_in_0_n	N4	C13	G1
Data_in_1_p	M7	G12	H2
Data_in_1_n	N8	G14	G3
Data_in_2_p	P9	K13	D1
Data_in_2_n	N9	K14	E1
Data_in_3_p	M10	M10	F3
Data_in_3_n	P11	P11	G2
Data_in_4_p	M11	N13	D2
Data_in_4_n	P12	N14	E3
Data_in_5_p	N3	E12	C2
Data_in_5_n	P4	E14	D3
Data_in_6_p	N5	N5	B1
Data_in_6_n	M5	M5	B2
Data_in_7_p	P8	P8	A1
Data_in_7_n	M8	M8	B3
Data_in_8_p	N12	N12	A2
Data_in_8_n	P13	P13	A3
Data_in_9_p	P2	P2	C5
Data_in_9_n	N2	N2	A5
Data_in_10_p	P3	N3	A6
Data_in_10_n	M3	P4	A7
Data_in_11_p	P7	F13	B6
Data_in_11_n	N7	F14	C7
clk_out	K1	K1	P2
xvs	A12	A12	P14
xhs	A13	A13	P13
data_out_0	J1	J1	N8
data_out_1	H1	H1	M6
data_out_2	F1	F1	M5
data_out_3	E1	E1	M7
data_out_4	C1	C1	N12
data_out_5	B1	B1	N7
data_out_6	A2	A2	P12
data_out_7	A3	A3	P5
data_out_8	A7	A7	P6
data_out_9	A9	A9	N2
data_out_10	A10	A10	P7
data_out_11	A11	A11	N4

Note:

1. The MachXO2 same bank pinout is preferred as this pinout has built-in termination resistors for the sub-LVDS Data_in bus.

3. Timing Specifications

The timing of the data_out and xhs is shown in Figure 3.1.

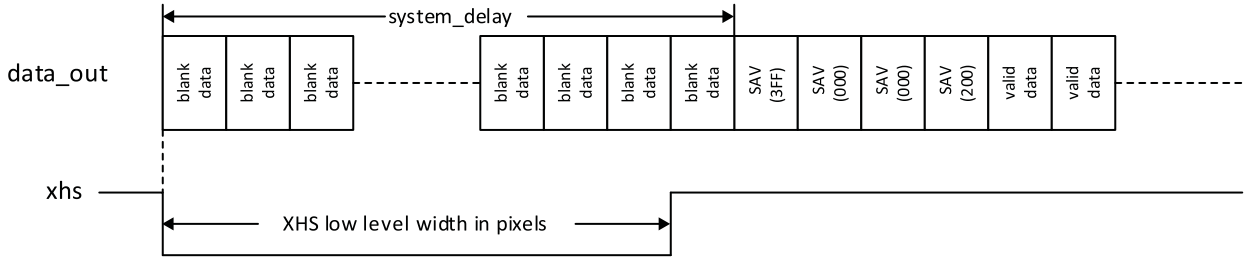

Figure 3.1. data_out and xhs Timing

The timing of xhs and xvs is shown in Figure 3.2.

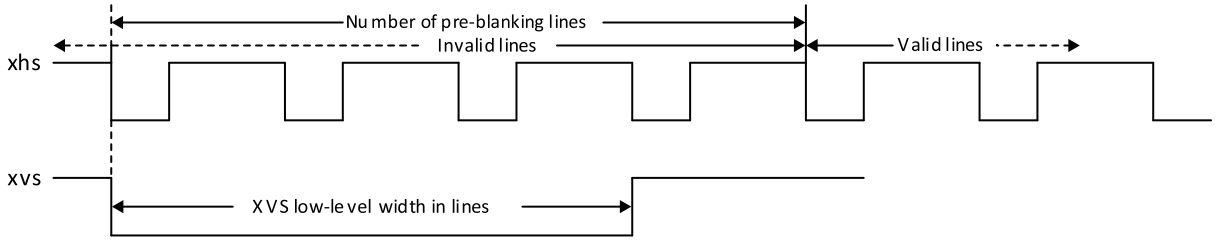

Figure 3.2. XHS and XVS Timing

The pixel number and line number can be configured with the parameters.

The simulation is supported by Active-HDL simulators. Set the working directory to the location of the .do script and then execute the .do script. The directory should also be updated on line 14 in the script file sim_active_functional_timing.do.

Figure 3.3 shows the relationship of the signal timing to each other at the horizontal blank and vertical blank.

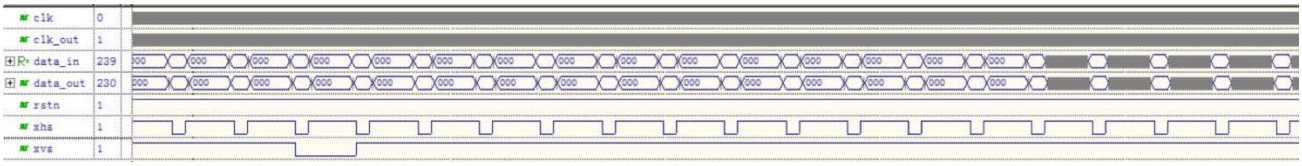

Figure 3.3. Simulation Screen Shot Showing Signal Timing

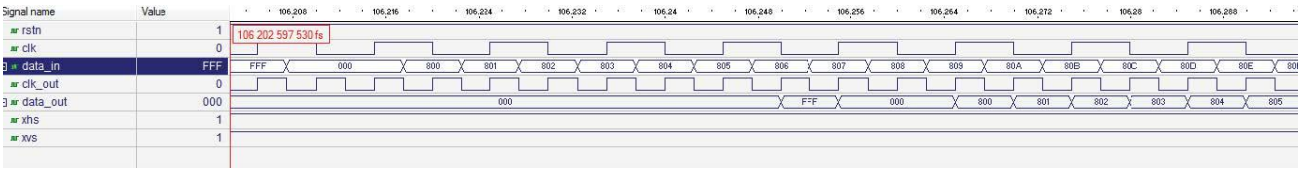

Figure 3.4. Simulation Screen Shot for drive_mode=0 and ad_conv_width=12

The waveform, as shown in Figure 3.4, is for drive_mode = 0 and ad_conv_width=12, The waveform shows that data_out follows data_in after 9 clk_out delay.

Tested Reference Design

The Sony IMX036 bridge has been utilized on the TI/Appropho Network Camera. The design utilizes the MachXO2-1200 device.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.8, January 2020

Section	Change Summary
All	• Changed document number from RD1122 to FPGA-RD-02147. • Updated document template.
Disclaimers	Added this section.

Revision 1.7, January 2015

Section	Change Summary
Implementation	Updated Implementation section. Updated Table 2.1, Performance and Resource Utilization. • Added support for Lattice Diamond 3.3 design software. • Added support for LSE and Synplify Pro.

Revision 1.6, March 2014

Section	Change Summary
Implementation	• Added support for ECP5 device family. • Updated Table 2.1, Performance and Resource Utilization. • Updated to support Lattice Diamond 3.1 design software.

Revision 1.5, October 2012

Section	Change Summary
Introduction	Updated Introduction section.

Revision 1.4, October 2012

Section	Change Summary
Implementation	Updated data in the Pinout table, LatticeXP2 Multi-Bank 132-Ball csBGA column.

Revision 1.3, August 2012

Section	Change Summary
All	Updated to include support of the built in WDR capability of the Sony IMX136/104.

Revision 1.2, March 2012

Section	Change Summary
All	• Document updated with new corporate logo. • Document updated for IMX136.

Revision 1.1, January 2012

Section	Change Summary
All	Document updated for MachXO2 device support.

Revision 1.0, May 2011

Section	Change Summary
All	Initial release.

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