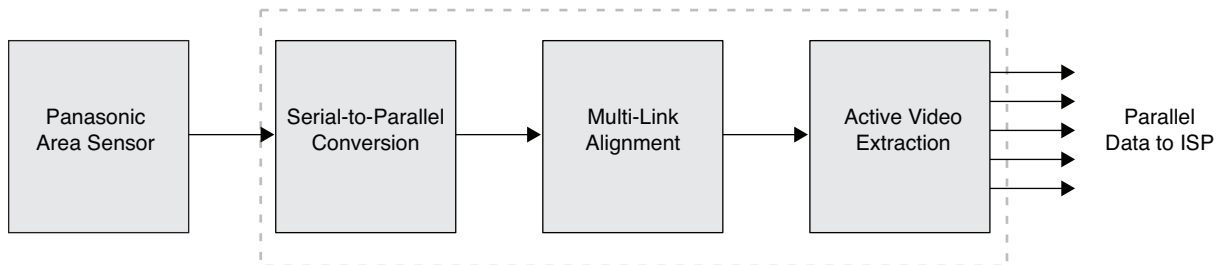


## Introduction

As image sensor resolutions have increased, Panasonic has chosen a differential high-speed serial interface instead of using a traditional CMOS parallel interface for their sensors. This was done because the resolution and frame rate of the MN34041 and MN34081 are sizable. An interface of higher bandwidth and lower noise than a standard CMOS parallel bus was required. The Panasonic MN34041 and the MN34081 are image sensors that output 2.1M pixels and 1.33M pixels, respectively. The MN34041 outputs two serial data streams up to three lanes wide. The MN34081 outputs two serial data streams up to two lanes wide. Each stream has its own clock.

The Panasonic Image Sensor Bridge reference design is configured to utilize the two data streams with two lanes. The full resolution of the Panasonic sensor is supported (MN34041: 1944x1092 at 60 fps, MN34081: 1304x1024 at 60 fps). The design output is a 12-bit parallel data bus that a standard Image Signal Processor (ISP) can read (Figure 1).

**Figure 1. Panasonic Image Sensor Bridge Block Diagram**

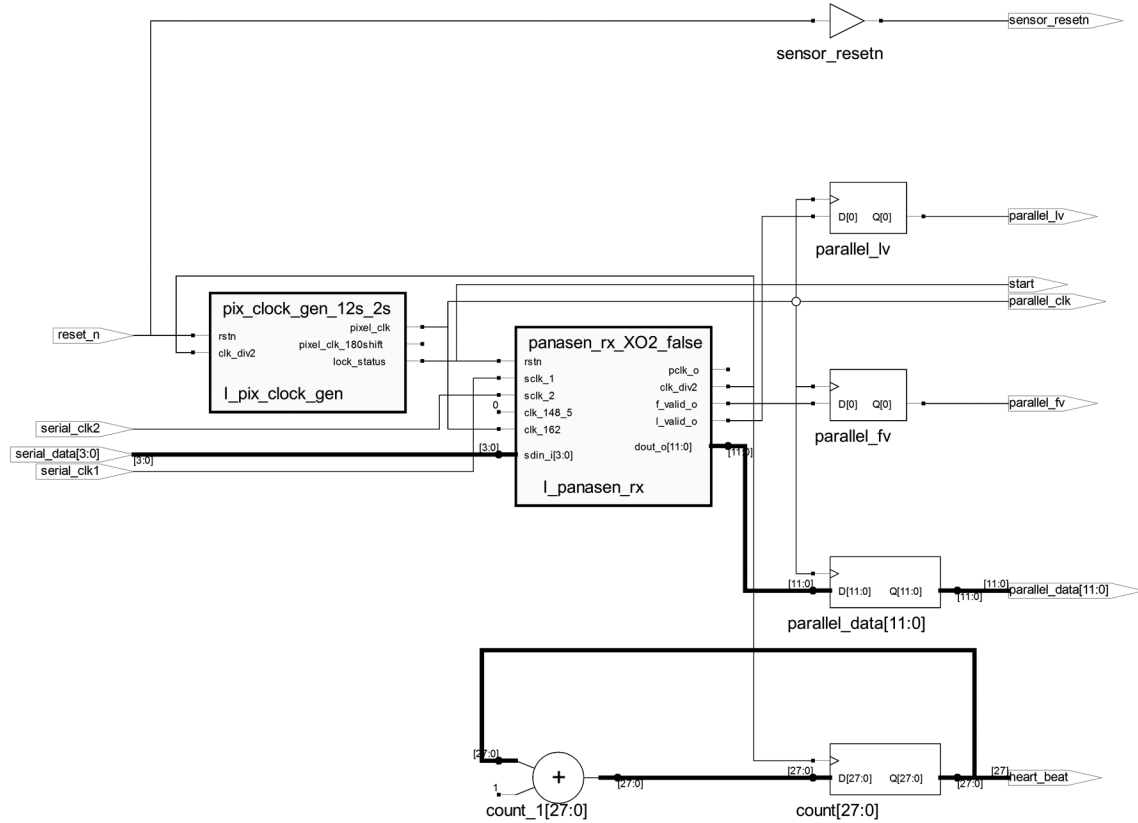


Each input port is a sub-LVDS signal and can operate up to 500 Mbps. The output signals interfacing to the ISP are single-ended LVCMOS pins and can be driven at 1.8V, 2.5V and 3.3V. For technical details regarding the image sensor, please contact Panasonic.

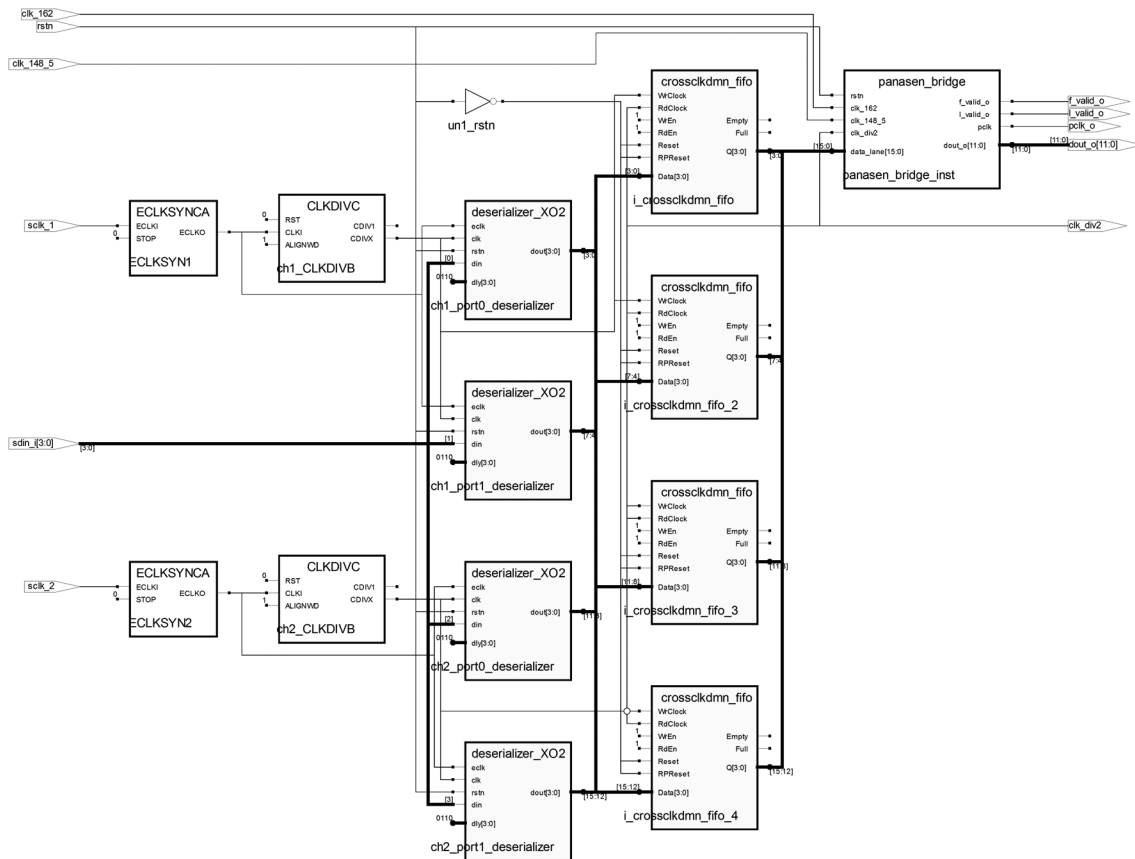
## Complete Reference Design for Panasonic to Parallel Sensor Bridge

The complete reference design includes a sensor bridge NGO and HDL wrappers for component primitives specific to the targeted device family. Reference design blocks diagram are shown in Figures 2 and 3.

**Figure 2. Reference Design Top Level Block Diagram**



**Figure 3. Reference Design NGO Wrapper Block Diagram**



**Table 1. Sensor Bridge NGO Port Definitions**

| Signal              | Definition                                                                                                                                    | Direction |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| reset_n             | Reset, active low                                                                                                                             | Input     |
| serial_clk_1        | Serial link channel 1 clock                                                                                                                   | Input     |
| serial_clk_2        | Serial link channel 2 clock                                                                                                                   | Input     |
| serial_data[3:0]    | Serial link data:<br>serial_data [0], ch1 port 0<br>serial_data [1], ch1 port 1<br>serial_data [2], ch2 port 0<br>serial_data [3], ch2 port 1 | Input     |
| start               | Indicating pixel clock is available                                                                                                           | Output    |
| parallel_clk        | $(\text{serial\_clk}/2 * 4/3)$                                                                                                                | Output    |
| parallel_data[11:0] | 12-bit parallel data                                                                                                                          | Output    |
| parallel_lv         | Indicates active video data inside a line                                                                                                     | Output    |
| parallel_fv         | Indicates active lines                                                                                                                        | Output    |

## Panasonic Sensor Bridge NGO File

The Panasonic Sensor Bridge NGO accepts the deserialized data lanes and formats them to a 12-bit parallel bus (Figure 4). First, the data on each lane is word-aligned to 12 bits. Second, the lanes are aligned to each other. Finally, the word- and lane-aligned data is parsed into the parallel bayer output.

Figure 4. Sensor Bridge NGO Block Diagram

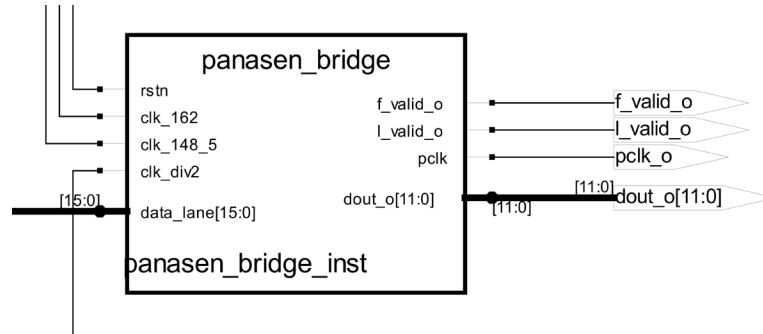
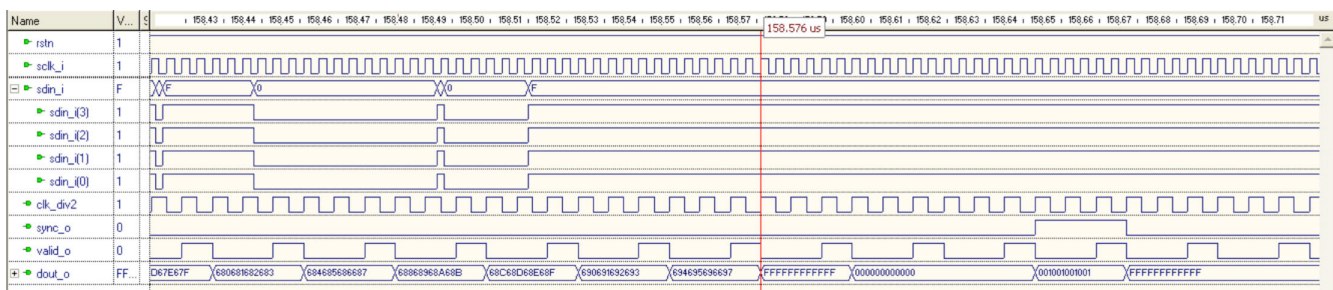


Table 2. Sensor Bridge NGO Port Definitions

| Signal          | Definition                                                                                                                                    | Direction |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| rstn            | Reset, active low                                                                                                                             | Input     |
| clk_162         | Active Video Extraction Clock:<br>(4/3 * clk_div2); clock speed can vary<br>depending on sensor oscillator and sensor<br>PLL configuration.   | Input     |
| clk_148_5       | Reserved; tie to 1'b0.                                                                                                                        | Input     |
| data_lane[15:0] | Deserialized data:<br>data_lane[3:0], ch1 port 0<br>data_lane[7:4], ch1 port 1<br>data_lane[11:8], ch2 port 0<br>data_lane[15:12], ch2 port 1 | Input     |
| f_valid_o       | frame valid, active high                                                                                                                      | Output    |
| l_valid_o       | line_valid, active high                                                                                                                       | Output    |
| dout_o[11:0]    | Parallel data Dout_o[11:0]                                                                                                                    | Output    |
| clk_div2        | Output clock, Serial clock/2                                                                                                                  | Output    |

The simulation screen shot in Figure 5 shows the time of the serial lane inputs to the output of the Multi-Link Alignment Module. Note that the dout bit order is reversed in the simulation. Also, channel 1 and channel 2 use the same serial link clock, sclck\_i. This is to simplify the test bench source code. In the actual design, the two clock signals are utilized to capture the deserialize data from each port. A FIFO on each lane is used to create a common clock domain.

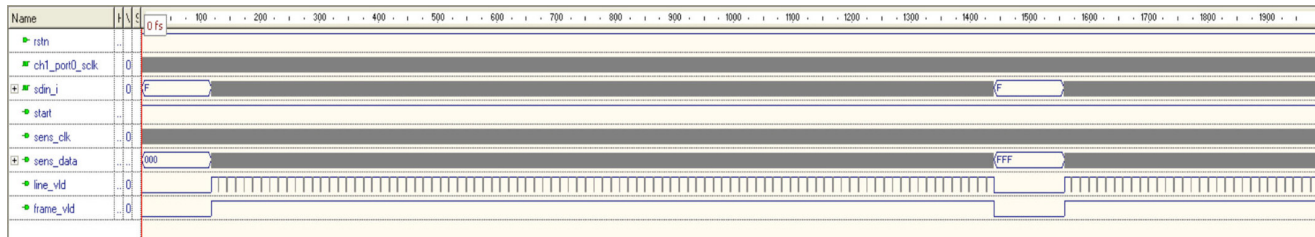
Figure 5. Sensor Bridge Simulation



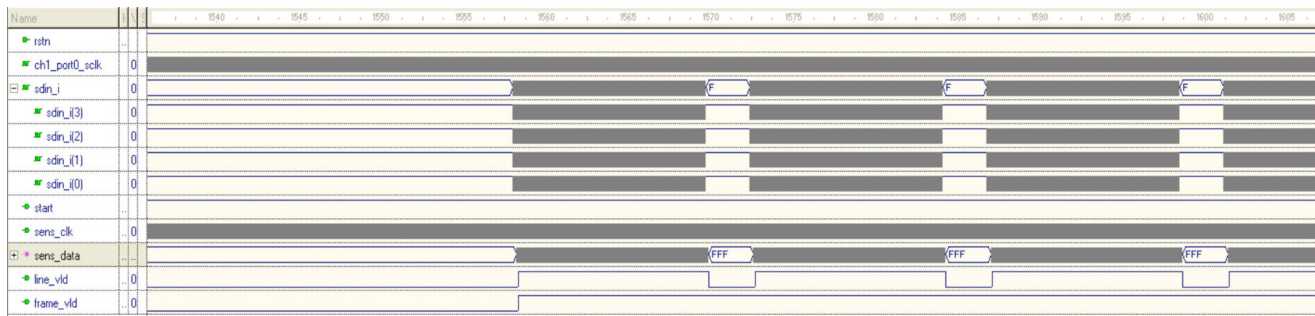
In the simulation  $dout\_o = \{ch2\ port1, ch2\ port0, ch1\ port1, ch1\ port0\}$ , each  $chx\ portx$  is 12-bit parallel pixel data. The 12-bit parallel bus output is muxed from this and synced to  $f\_valid\_o$  and  $l\_valid\_o$ .

Figures 6 and 7 show the simulation for this reference design. Figure 6 shows an entire frame being transmitted, while Figure 7 shows the start of a frame.

**Figure 6. Reference Design Simulation (Full Frame)**



**Figure 7. Reference Design Simulation (At Start of Frame)**



The following is a summary of this reference design:

1. A 2-channel, 2-port sensor bridge NGO is instantiated to implement the serial-to-parallel conversion.
2. Clock domain transfer to parallel\_clk.
3. The final parallel output is 12-bit pixel words at a clock rate of serial\_clk/2 \* 4/3 in Bayer format.
4. Line valid and frame valid signals are generated to indicate active pixels in a line and active lines in a frame.

**Table 3. Sensor Bridge Resource Utilization in a LatticeXP2 and MachXO2 Devices**

| Complete Sensor Bridge Reference Design | Registers | Slices | LUTs | EBRs |
|-----------------------------------------|-----------|--------|------|------|
| LatticeXP2                              | 596       | 468    | 443  | 0    |
| MachXO2                                 | 822       | 648    | 517  | 0    |

**Table 4. Place & Route Timing Analysis (Based on LatticeXP2-5E and MachXO2-1200HC Devices in 132-Ball csBGA Packages)**

|                     | LatticeXP2 |         |         | MachXO2 |         |         | Units |
|---------------------|------------|---------|---------|---------|---------|---------|-------|
|                     | -5         | -6      | -7      | -4      | -5      | -6      |       |
| clk_div2 (Max.)     | 150.852    | 176.243 | 189.861 | 138.485 | 143.802 | 164.231 | MHz   |
| parallel_clk (Max.) | 193.386    | 213.493 | 262.674 | 164.096 | 181.554 | 208.464 | MHz   |

1. MN34041 maximum internal operating frequency = 500 MHz (Table 1.2.6 of MN34041 data sheet). Normal operating frequency is 486 MHz. This means the maximum nominal serial clock speeds are 243 MHz respectively.
2.  $\text{clk\_div2 (Max)} = \text{serial\_clk}/2 = 250\text{MHz}/2 = 125\text{MHz}$ .  $\text{clk\_div2(nominal)} = 121.5\text{ MHz}$ . Please consider sensor operating speeds when choosing device speed grades.  $\text{parallel\_clk (max)} = 4/3 * \text{clk\_div2} = 166.67\text{MHz}$ .  $\text{parallel\_clk (nominal)} = 162\text{ MHz}$ . Please consider sensor operating speeds when choosing device speed grades.

**Table 5. Pinout for Complete Sensor Bridge in a LatticeXP2-5 or MachXO2-1200 Device**

| Bridge Signal Name | LatticeXP2-5<br>132-Ball csBGA | MachXO2-1200 <sup>1</sup><br>132-Ball csBGA |
|--------------------|--------------------------------|---------------------------------------------|
| SDOCAP             | H1                             | N6                                          |
| SDOCAN             | H3                             | P6                                          |
| SDOCBP             | L1                             | M7                                          |
| SDOCBN             | L3                             | N8                                          |
| SDODAP_0           | D2                             | M11                                         |
| SDODAN_0           | E3                             | P12                                         |
| SDODAP_1           | D1                             | P8                                          |
| SDODAN_1           | E1                             | M8                                          |
| SDODBP_0           | F3                             | M9                                          |
| SDODBN_0           | G2                             | N10                                         |
| SDODBP_1           | C2                             | N3                                          |
| SDODBN_1           | D3                             | P4                                          |
| RESET_TO_SENSOR    | B9                             | F2                                          |
| PSV                | C9                             | C3                                          |
| MSSEL              | A7                             | D1                                          |
| RESET_BAR          | F12                            | C1                                          |
| PIXCLK             | P2                             | A11                                         |
| FRAME_VALID        | P14                            | B7                                          |
| LINE_VALID         | P13                            | C4                                          |
| DOUT0              | N8                             | C6                                          |
| DOUT1              | M6                             | B3                                          |
| DOUT2              | M5                             | C11                                         |
| DOUT3              | M7                             | A12                                         |
| DOUT4              | N12                            | A7                                          |
| DOUT5              | N7                             | B5                                          |
| DOUT6              | P12                            | A9                                          |
| DOUT7              | P5                             | A10                                         |
| DOUT8              | P6                             | A2                                          |
| DOUT9              | N2                             | B12                                         |
| DOUT10             | P7                             | C12                                         |
| DOUT11             | N4                             | B13                                         |
| TCK <sup>2</sup>   | K14                            | B6                                          |
| TDI <sup>2</sup>   | L13                            | B4                                          |
| TDO <sup>2</sup>   | K13                            | A4                                          |
| TMS <sup>2</sup>   | L12                            | A6                                          |

1. When using the pins in this table for the MachXO2-1200 device, termination resistors are built in for serial\_data SDOD lines and serial\_clk SDOC lines.
2. All parallel data signals reside on Bank 0 for the MachXO2 and Banks 4 and 5 for the LatticeXP2. Voltage rails for these banks should be considered when interfacing directly to an ISP.

## Tested Designs

The Panasonic Image Sensor Bridge has been tested with the Texas Instruments IPNC DM812X and DM385. See Leopard Imaging at [www.leopardimaging.com](http://www.leopardimaging.com) for details on the Texas Instruments IP camera design.

## References

- Target Specifications – Area Sensor MN34041PL, Panasonic Corporation
- Target Specifications – Area Sensor MN34081PLJ, Panasonic Corporation

## Technical Support Assistance

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## Revision History

| Date          | Version | Change Summary                                                                       |
|---------------|---------|--------------------------------------------------------------------------------------|
| May 2011      | 01.0    | Initial release.                                                                     |
| February 2012 | 01.1    | Added data on MN34081 and the MachXO2 pinout.                                        |
| March 2012    | 01.2    | Document updated with new corporate logo.                                            |
|               |         | Place & Route Timing Analysis table – Corrected speed grade information for MachXO2. |
|               |         | Added first footnote to the Pinout table.                                            |
| March 2012    | 01.3    | Updated Pinout table.                                                                |
| March 2012    | 01.4    | Updated Pinout table footnote.                                                       |