HiSPi-to-Parallel Sensor Bridge

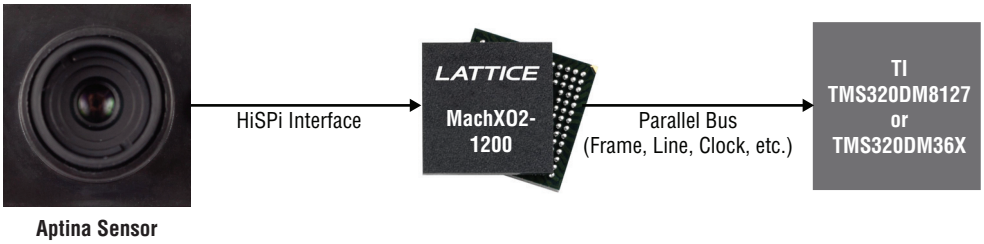
Sensor resolutions and frame rates have increased to a point where the traditional CMOS parallel interface is no longer able to handle the bandwidth requirements. To support higher bandwidth, Aptina Imaging has introduced a high-speed serial interface called HiSPi. The HiSPi interface can operate from one to four lanes of serial data, plus one clock lane. Each signal is differential and can run at speeds up to 700 Mbps.

The Need for HiSPi-to-Parallel Sensor Interface Bridging

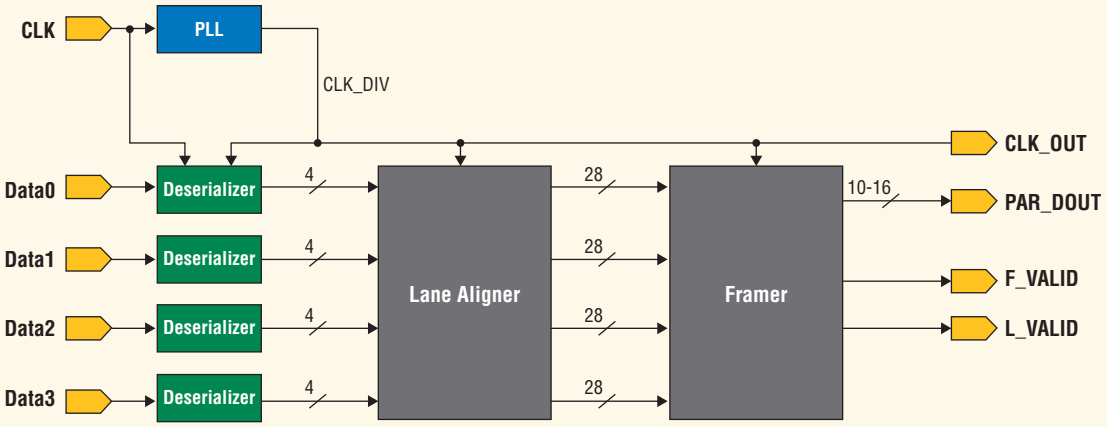
The majority of ISP (Image Signal Processing) devices support traditional CMOS parallel sensor interfaces. They usually lack interfaces that support HiSPi. Therefore, a bridge device is required to convert the HiSPi serial data to a parallel format. The MachXO2™-1200 or LatticeXP2™-5 non-volatile device provides an efficient and cost-effective solution for HiSPi-to-parallel bridging.

Key Features

- **Supports HiSPi formats Packetized-SP, Streaming-SP, Streaming-S or ActiveStart-SP8**
  - From one to four lanes, running at up to 700 Mbps
- **Emulates Parallel Sensor Output**
  - Output bus widths of 10, 12, 14 or 16 bits
- **HDR and Linear Modes Supported**
- **Bridge Device Offered in Space-saving 8x8 mm 132-Ball csBGA. TQFP Packages Also Available.**
- **Requires No External PROM**
- **Tested with Texas Instruments TMS320DM8127 & TMS320DM36X and Aptina AR0331, MT9M024 & MT9J003**
- **Parallel Interface can be Configured for 1.8V, 2.5V or 3.3V LVCMOS Levels**
- **MachXO2 and LatticeXP2 are Available in Commercial or Industrial Temperature Grades. The LatticeXP2 is Also Offered in Automotive Grade.**



HiSPi-to-Parallel Sensor Interface Bridging Block Diagram



Request your own HiSPi bridge at: www.latticesemi.com/hispibridge

Applications Support
1-800-LATTICE (528-8423)
503-268-8001
techsupport@latticesemi.com

March 2012
Order #: I0214B