

Introduction

Lattice is the inventor and the leader in the (ISP) In-System Programming PLD technology. One of the visions and ultimate goal of ISP is the live field upgrade of a mission critical system. Being a mission critical system, the field upgrade process must meet the following criteria.

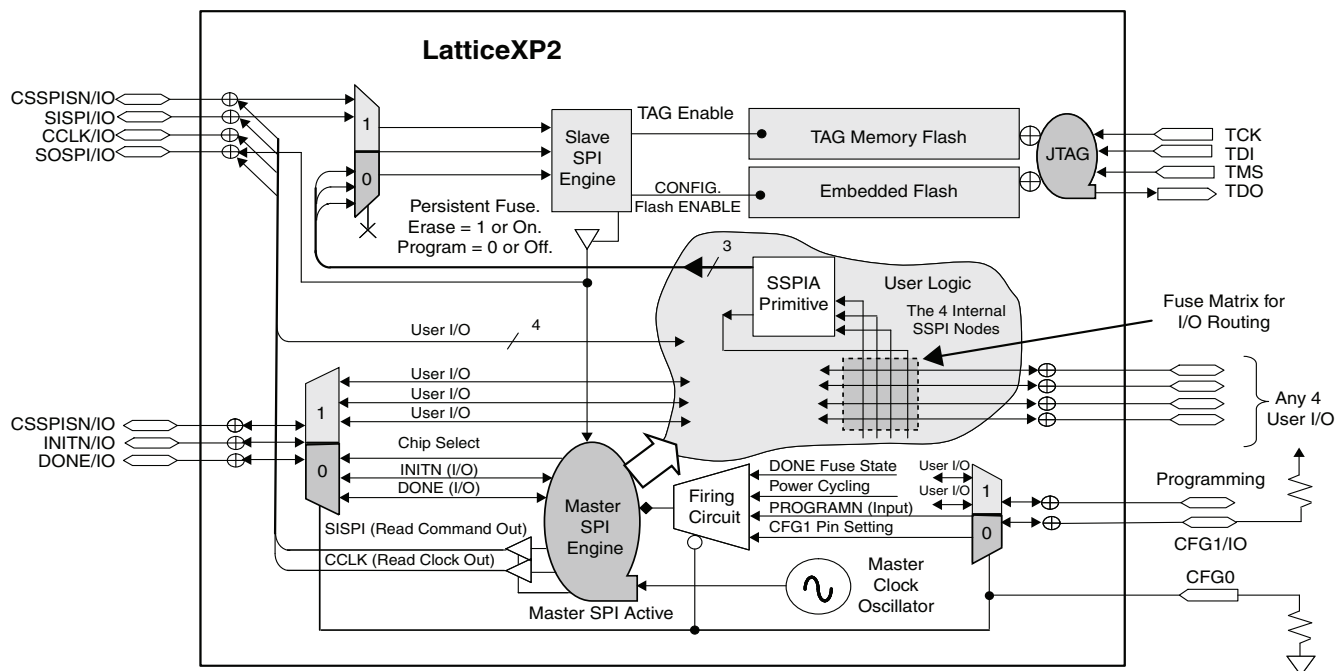
1. It must be extremely reliable as any form of programming failure is not acceptable.
2. The system must remain functional throughout as even a small interruption is not acceptable including transitioning from the current pattern to the newly updated pattern.
3. Various security features will be required to protect the IP (Intellectual Property) of the mission critical system.

With the introduction of the LatticeXP2 Flash based non-volatile FPGA family, Lattice deliver the first and only ISP products with all the critical attributes required to provide the ultimate solution of ISP, reliable and secure live field upgrade of a mission critical system. The critical attributes are:

1. Dual boot feature and Flash Protect to provide the extremely reliable system.
2. Instant-on, Background Programming, and TransFR features provide seamless live field upgrade.
3. Key Protect and Encryption to protect users' Intellectual Property.

The block diagram of the LatticeXP2 device shown in Figure 17-1 provides a bird's eye view for the unique co-existence of the Master SPI port with the Slave SPI port. The detail of the LatticeXP2 Slave SPI interface can be found in the document dedicated on the subject. TransFR, the must have feature for the mission critical field upgrade, is available only on the JTAG port. Therefore, the programming activities described in this document will focus on the JTAG port only.

Figure 17-1. LatticeXP2 Master SPI and Slave SPI Ports



Complementing its internal Flash configuration memory, the LatticeXP2™ also provides support for inexpensive SPI Flash devices. This provides the ability to use an alternate or backup bitstream, referred to as the “golden” image. The device always attempts to load the primary image from the selected source. Should any unexpected interrupts occur during configuration of the primary image, the LatticeXP2 device will automatically switch sources and configure from the golden image location.

Dual Boot Feature

One of the biggest risks in the field upgrade applications is disruption during the field grade process. Examples:

1. Power disruption.
2. Communications disruption.
3. Data file corruption.

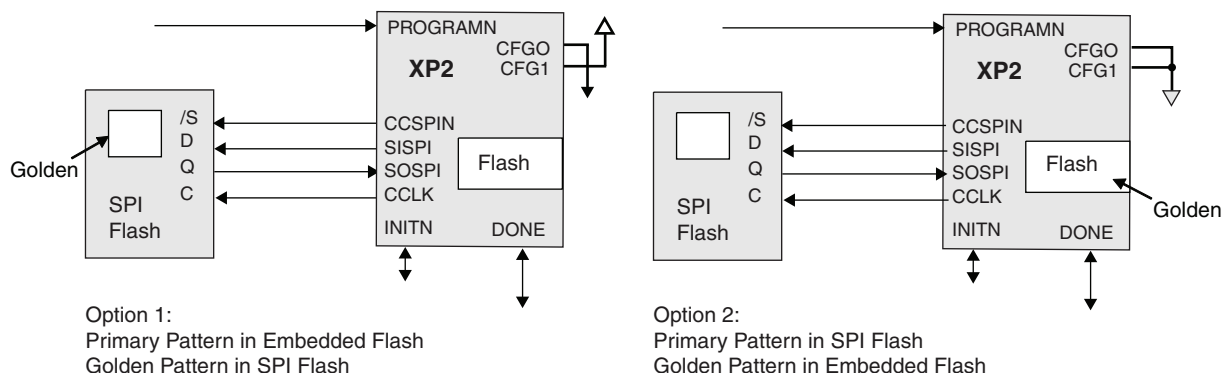
To eliminate the risk completely, the device will automatically switch to load from the second known good (Golden) pattern when the first pattern is corrupted. This is the Dual Boot feature. Thus, the main purpose of the Dual Boot feature is to enhance the reliability of a field upgradeable system.

The LatticeXP2 devices are known as non-volatile devices for the device has an embedded Flash block storing the configuration pattern. The advantage of a non-volatile device is the extremely fast instant-on time, made possible by the massive parallel loading from the embedded Flash into the SRAM block of the device.

To keep the cost as low as possible, the LatticeXP2 only has enough embedded Flash to store one pattern. To enable the dual boot feature, Lattice designed into the LatticeXP2 device family the popular SPI Flash interface found originally in the LatticeECP/2/3 family of volatile FPGA devices. The SPI Flash device can be used to store the second (Golden) pattern.

The basic connections for the two Dual Boot options are shown in Figure 17-2.

Figure 17-2. Dual Boot Options



The Dual Boot feature on the LatticeXP2 devices is designed to be simple for users by carrying out all the necessary procedures on the industry standard JTAG port. Thus, users do not need to learn a new tool or new flows. It also allows users to implement the feature incrementally.

The block diagram in Figure 17-3 shows the built-in circuitry, Lattice designed into the FPGA product families, which enable the JTAG port to access the non-JTAG SPI Flash devices. This unique capability also allows the SPI Flash devices to be live field upgradable.

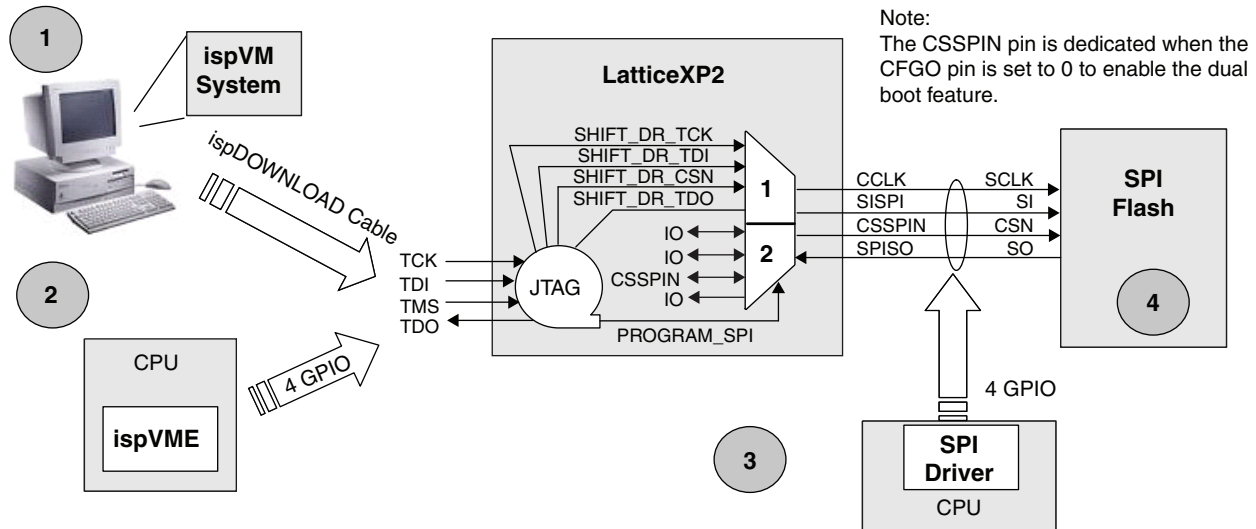
The four methods shown in Figure 17-3 are listed below.

1. Use ispVM to program the SPI Flash directly during the board development phase.
2. Use ispVME to program the SPI Flash during the board production phase.
3. Use the CPU to access the SPI Flash directly bypassing the LatticeXP2 device.

4. Use off board programming method such as the third party programmers from BPM Microsystems or System General to pre-program the SPI Flash devices and then mount them on board.

Methods 3 and 4 are of no interest as far as field upgrade is concerned. Therefore, this document will focus only on methods 1 and 2.

Figure 17-3. Four Methods for Programming the SPI Flash Device



Definitions

SPI

SPI stands for the Serial Peripheral Interface defined originally by Motorola.

Master SPI

The FPGA device boots itself by acting as the SPI host to clock bitstream data out of the external SPI Flash device.

SDM (Self Download Mode)

The FPGA device boots itself in a massive parallel fashion from the embedded Flash for instant-on.

Erase

Write into all the Flash cells state a logical one (1) (a.k.a. open fuse).

Program

Write into the selected Flash cells state a logical zero (0) (a.k.a. close fuse).

Configure

Write the pattern into the SRAM fuses of the FPGA device and wake up. It is also known as boot up.

Primary Boot

Upon power cycling, the FPGA device will load this pattern in first. Only one primary pattern is allowed.

Golden Boot

The guaranteed good pattern loaded into the FPGA device when booting failure occurs. It is also known as the root boot. Only one Golden boot pattern is allowed.

Dual Boot

The device has two patterns, namely a Primary pattern and a Golden pattern, to choose to load.

Refresh

The action loads the pattern from a non-volatile source to configure the FPGA device.

Bitstream Data File (.BIT File)

The configuration data file, for a single FPGA device, in the format that can be loaded directly into the FPGA device to configure the SRAM cells. The file is expressed in binary hex format. The file is not printable.

JEDEC File (.JED File)

The programming data file as defined by JEDEC 42.1C standard. The programming file is expressed in the ASCII 1 and 0 format. The file is printable. Third party programmers use it to support large volume production programming.

TransFR

The feature allows users to precisely control the user IO pins (high, low, or tri-state) while the embedded Flash is massively parallel loaded into the SRAM fuses.

Security

Standard security is the feature that disables the read back operation from the embedded Flash and SRAM blocks. Advanced security refers to the features providing encryption support and various Keys and Locks for protecting the Embedded Flash block.

SED CRC

Soft Error Detection (SED) by calculating the CRC value of the value of the SRAM fuses. Lattice implements the feature by using a 32-bit polynomial.

One Shot SED

After each boot from the embedded Flash, this feature enables the SED CRC feature automatically and immediately checking the integrity of the embedded Flash content.

Background Mode (User Mode)

The FPGA device shall remain fully operational as governed by the fuse pattern residing in the SRAM fuse module of the FPGA device at the time while programming activities being carried out on the FPGA device or the peripheral device (SPI Flash device) attached to it. This mode is the most critical attributes of the live field upgrade feature that can be found only on Lattice's FPGA devices.

Direct Mode (IEEE 1532 Access Modal State)

The FPGA device shall be removed from the governing of the fuse pattern residing in the SRAM fuse module, or so to say, put to sleep while programming activities being carried out on the FPGA device or on the peripheral device (SPI Flash device) attached to it. The IOs are either tri-stated or held statically while in this mode. Lack of a better term, Lattice uses it to contrast against the background mode. All PLD devices support this mode.

Purpose

It has been the ultimate goal for the In-System Programming revolution championed by Lattice since 1990 to provide a reliable and continuous live field upgradable system. The TransFR feature designed into Lattice devices since 2000 brings Lattice closer to the ultimate goal. With the introduction of the dual boot feature and the advanced security feature in 2007, the ultimate goal is achieved.

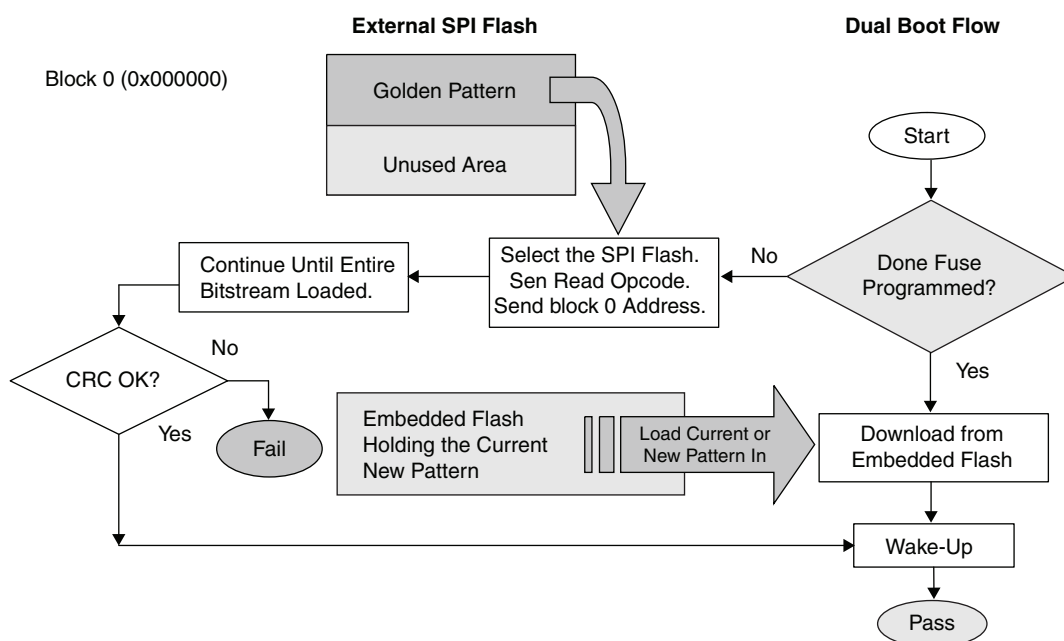
This document provides detail technical explanation of the dual boot feature in the LatticeXP2 device family. The application details for using ispVM and ispVME to support dual boot feature during the different applications is as follows:

1. Use ispVM or ispVME to program the bitstream into the SPI Flash device
2. Use ispVM or ispVME to program the JEDEC file into the LatticeXP2 device.

The application of the LatticeXP2 Advanced Security feature, TransFR feature, and Mission Critical Field Upgrade are briefly mentioned in this document. The details can be found in TN1212, [LatticeXP2 Advanced Security Programming Usage Guide](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#), respectively. Contact Lattice Applications for the other documents if required.

Note: The LatticeXP2 devices only support encrypted JEDEC files, which target the embedded Flash of the LatticeXP2 devices.

Figure 17-4. LatticeXP2 FPGA Dual Boot Feature Flow Diagram



Resource

The minimum SPI Flash density required to support the dual boot feature is listed in Table 17-1.

Table 17-1. Required SPI Flash Device Size

Device Name	Bitstream Size	Minimum SPI Flash Density
	M bits	M bits
XP2-5	1.28	2
XP2-8	1.99	2
XP2-17	3.55	4
XP2-30	5.79	8
XP2-40	8.04	16

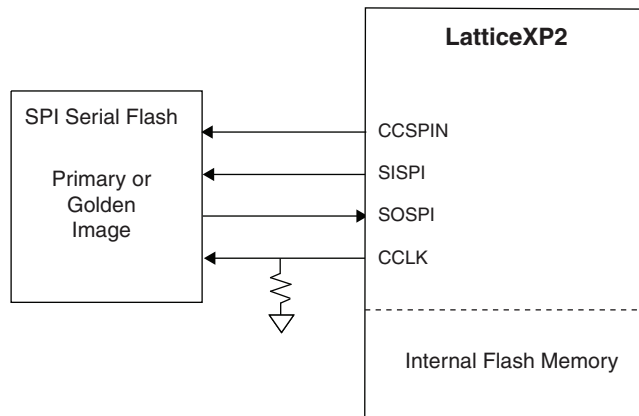
Dual Boot Mode

The LatticeXP2 Dual Boot sysCONFIG™ mode is selected using CFG pin settings. Its the sysCONFIG modes supported by the LatticeXP2 device family. Figure 17-1 illustrates the SPI Flash hardware connections.

Table 17-2. LatticeXP2 sysCONFIG Modes

CFG0	CFG1	Configuration Mode	Primary Boot Source	Secondary Boot Source
0	0	Dual Boot	External SPI Flash	Internal Flash
0	1	Dual Boot	Internal Flash	External SPI Flash
1	X	Self Download Mode (SDM)	Internal Flash	None

Figure 17-5. LatticeXP2 Hardware Connections to SPI Flash



Internal logic is used to detect a configuration failure from the primary source and provides the ability to reattempt configuration from the secondary source. This sequence is used when the LatticeXP2 is set to dual boot mode and configuration is initiated.

Configuration initiates in dual boot mode when any of the following events occur:

- The device is powered-up with all supplies reaching their required minimum values.
- The PROGRAMN pin is toggled.
- The REFRESH command is issued via the ispJTAG™ port.

Should configuration from both primary and golden images in dual boot mode fail, the INITN pin will be driven low and the configuration process will halt.

Lattice strongly recommends using the embedded Flash as the first (Primary) boot to take full advantage of the features only embedded Flash can offer, for example fast instant-on time, standard or advance security, and TransFR. The dual boot flow described in this document focus only on setting CFG[0:1] to [01], respectively, to select the embedded Flash as the first boot.

This flow is triggered either by power cycling or toggle the PROGRAMN pin.

A. When the dual boot mode is selected by setting the CFG0 to low (0), the device checks the CFG1 pin first to decide the source of the first boot. If the CFG1 pin is high (1), the device will check the Flash done fuse immediately.

1. Done Fuse Programmed

If the Done fuse is programmed, then the embedded Flash must have been programmed with a valid pat-

tern. The device will boot from the embedded Flash. If it is desirable to check if the boot from the embedded Flash is error free, the One Shot SED feature can be used to confirm.

Note: The devices carry out the one shot SED by reading the SRAM fuses and calculate the CRC value in Background mode.

2. Done Fuse Not Programmed (aka Erased)

If the Done fuse is erased, then the embedded Flash must have an invalid pattern. The device will activate the Master SPI engine to load the data from the external SPI Flash device. The standard protocol of the Master SPI engine is to ignore the first 128 bits of data from the SPI Flash device, and then begins looking for the preamble code 0xBDB3.

There are two possible failures.

- a. The preamble code is not detected within ~16K clocks. This will happen if the SPI Flash device is blank. This is known as a time out failure.
- b. The CRC value calculated by the Master SPI engine of the device does not match with the one embedded in the bitstream. This means the bitstream is corrupted.

If there is a failure, the device drives the INITN pin low to indicate a failure. Otherwise, the device wakes up and functions.

Note: The INITN pin is functional only when the Master SPI engine is active. Otherwise, it has no function.

- B. If the CFG1 pin is set to low (0), then the device will activate the Master SPI engine to boot the first pattern in. If failure occurs, as described above in 2a or 2b, the device will drive the INITN pin low and then high, and then check if the Flash-Done fuse is programmed. If the Done fuse is programmed, the device will perform the SDM, drive the DONE pin high, and the device wakes up. If the Done fuse is not programmed, then the device stops configuring and leaves the DONE pin low to indicate configuration did not complete.

From the dual boot flow described above, it should become obvious why the Done fuse is always the very first fuse to be erased when performing an erase operation. Also, it is the last Flash fuse to be programmed when programming embedded Flash in LatticeXP2 devices.

Critical Points

1. Check the maximum read frequency supported by the SPI Flash devices. Do not set the CCLK frequency in the bitstream beyond the maximum as specified on the data sheet of the SPI Flash devices.

Reason: All SPI Flash devices support Slow Read command (0x03) and Fast Read command (0x0B). The LatticeXP2 family only supports the Slow Read command.

When the device is powered up, the CCLK frequency is the silicon default, which is approximately 3.1 MHz. After the LatticeXP2 starts loading the bitstream, the CCLK frequency is updated to user's selected frequency. If the selected CCLK frequency exceeds maximum frequency supported by the SPI Flash device, the LatticeXP2 may not configure.

Work-around Solution: When using the ispUFW to convert the JEDEC file into a bitstream file, select a CCLK frequency setting that meets the specifications of the target SPI Flash.

2. If the JTAG port has been used, do not toggle the PROGRAMN pin to reboot unless the board has been power cycled. (Note 2 of the Signal Descriptions Table of DS1009, [LatticeXP2 Family Data Sheet](#), shown in Figure 18, describes this restriction.)

Figure 18. LatticeXP2 Datasheet Note

Lattice Semiconductor

Pinout Information
LatticeXP2 Family Data Sheet

Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN ¹	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI ²	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI ²	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN ²	O	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V _{CC} is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10kΩ is recommended.

2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

Reason: The JTAG port is designed to be all powerful so that even the PROGRAMN pin is disabled to prevent the pin from interrupting the JTAG port operations.

Work-around Solution: Use the JTAG Refresh instruction to reboot instead of toggling the PROGRAMN pin.

- When the standard security fuse is set, use Background Mode to reprogram the LatticeXP2 device will fail verification.

Reason: The function of the standard security fuse is for disabling the read back operation. Whenever powering up the LatticeXP2 device, the security latch latches in the security fuse state to protect the fuse pattern residing in it. The Background Mode programming by design can not alter or corrupt the current pattern residing in the SRAM fuse module including the security latches. In other word, the security latch can't be cleared by Background operations. As a consequence, the security latch will block all subsequent Background read back operation.

Work-around Solutions:

- Skip verification on Background Mode programming.
- Use Encryption Background Programming.

Programming Procedures

Part 1: Program the Golden Pattern into the SPI Flash Devices

The SPI Flash device stores the Golden Pattern for the LatticeXP2 device. The Master SPI port requires the Golden Pattern to be in a bitstream format. The bitstream format is exactly the same as the LatticeECP/2/3 FPGA family of devices. The bitstream format can be found in the reference section at the end of this document.

For LatticeXP2 FPGA products, Lattice's design software, ispLEVER®, only generates a JEDEC file. The Universal File Writer (ispUFW®) utility shipped with the ispVM® System can be used to convert the LatticeXP2 JEDEC file into the bitstream file for the Master SPI port. The procedure is shown in Figure 17-1 and Table 17-3.

Figure 17-1. Using the ispUFW to Convert a JEDEC File to a Bitstream

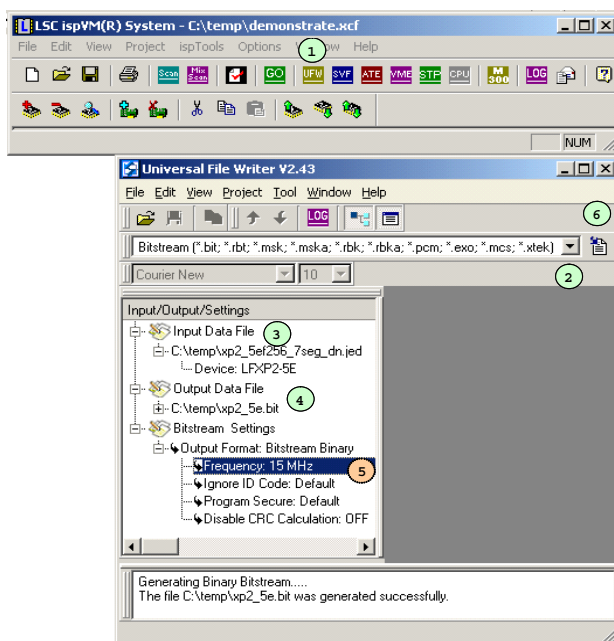


Table 17-3. Procedure for Converting a JEDEC File to a Bitstream using the ispUFW

Steps	Description
1	Launch the UFW on ispVM.
2	Select the bitstream file as the output format.
3	Browse for the JEDEC input file name. The device name will be extracted from the JEDEC file.
4	Browse or enter the output file name.

Table 17-3. Procedure for Converting a JEDEC File to a Bitstream using the ispUFW (Continued)

Steps	Description
5	This is optional. The default is 2.5 MHz. The maximum frequency recommended is 15 MHz due to the +/- 30% variance of the clock oscillator of the LatticeXP2 devices and the typical slow read (opcode = 0x03) frequency is 20 MHz maximum of the SPI Flash devices. The other settings following the Frequency shall be left to default to as shown. Just for completeness, the purpose of the other settings are described below: Ignore ID Code = Insert the LatticeXP2 device 32-bit Device ID checking into the bitstream. Default = do not check IDCODE. Program Secure = Insert the program security fuse command into the bitstream. Default = per the JEDEC file G field setting. Disable CRC Calculation = Remove CRC checking in the bitstream. OFF = the bitstream has CRC checking. (Note: The LatticeXP2 devices use the CRC value to check against bitstream corruption for configuration pass/fail decision. User must not change this setting when generating the final customer ready bitstream. These features are provided to aid board development and debugging.)
6	Click the file generation button to generate the bitstream.

Once the bitstream is generated, follow the procedures shown in Figure 17-2 and Table 17-4 to program the bitstream into the SPI Flash device on ispVM System. ispVM System supports quite many useful SPI Flash operations. Most operations are intuitively understood by users thus do not require detail description in this document.

After the SPI Flash is programmed with a valid bitstream, and if the LatticeXP2 device is not yet programmed, using JTAG refresh or power cycling the LatticeXP2 device will activate the Master SPI port to boot from the SPI Flash device. The PROGRAMN pin will work as long as the JTAG port has not been used. If the JTAG port has been used, power cycle the LatticeXP2 device will re-enable the PROGRAMN pin. Please refer to Critical Point 2 above for more details.

The mechanical detail on the JTAG port in the LatticeXP2 device serving as a SPI host to access the external SPI Flash devices can be found in the reference section at the end of this document.

Figure 17-2. Using ispVM to Program a Bitstream into the SPI Flash Device

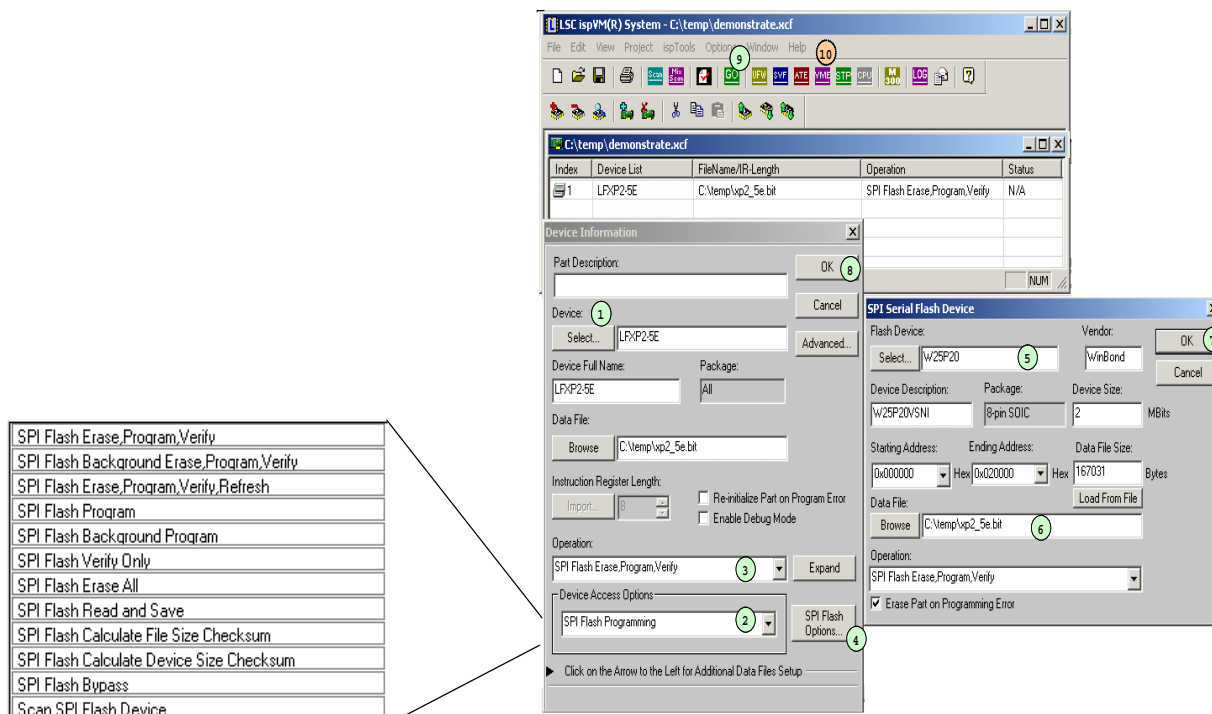


Table 17-4. Procedure for Program a Bitstream into the SPI Flash Device using ispVM

Steps	Description	
1	Scan or select the LatticeXP2 device.	
2	Select the SPI Flash Programming under the Device Access Options.	
3	Select the SPI Flash operation from the operation list: (Note: Due to the operations describe here are all carried out on the JTAG port, as previously noted, the PROGRAMN pin function is disabled by any activities on the JTAG port, power cycling the LatticeXP2 device is the only way to re-enable the PROGRAMN pin.)	
	SPI Flash Operation	Comments
	Erase, Program, Verify	This is a Direct Mode operation. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and while programming the SPI Flash device. The purpose is to set the persistent fuse to be on to gain unconditional access to the SPI Flash device through the JTAG port.
	Background Erase, Program, Verify	This is a Background Mode operation. The LatticeXP2 device can remain functional while programming the SPI Flash device. However, the persistent fuse in the LatticeXP2 device must be set to on first to use this operation. If the persistent fuse is not set to be on or the LatticeXP2 device is not blank, this operation will fail ID check. In that case, must use the operation above instead.
	Erase, Program, Verify, Refresh	This Direct Mode operation is provided as a work around for the PROGRAMN pin disabled by the JTAG port activities. Must use this operation if need to boot the bitstream into the LatticeXP2 device immediately after completing the SPI Flash programming. Refresh = the JTAG refresh instruction which has the effect as toggling the PROGRAMN pin.
	Program (Erase, Program)	This Direct Mode operation will erase and program the SPI Flash device in without verification in Direct Mode. The VME file size of this operation is half that of with verification. User might have no choice but use this operation when the EPROM size storing the VME file is too small to include verification.
	Background Program (Background Erase, Program)	Same as above except it is conducted in Background Mode. The persistent fuse in the LatticeXP2 device must be on for this operation to work.
	Calculate File Size Checksum	This Direct Mode operation will calculate the fuse checksum in the SPI Flash device per the starting address and ending address after browsing in the bitstream file at step 6 below. Example: The XP2-5E bitstream occupy sector 0, 1, and 2, or three sectors total. The checksum is calculated by reading the fuse data out from those three occupied sectors.
	Calculate Device Size Checksum	This Direct Mode operation will calculate the fuse checksum of the entire SPI Flash device. Example: The 2Mb SPI Flash device has four sectors total. The checksum is calculated by reading out fuse data from all four sectors
	Scan SPI Flash Device	This Direct Mode operation will scan SPI Flash device against the Lattice SPI Flash device database. If there is a match, then it shows what the device is on the message window for user to enter on step 6. If it is not in the database, then it returns an unknown device. User will need to find out the SPI Flash device name manually then select accordingly at step 6.
4	Launch the SPI Flash device menu.	
5	Select the SPI Flash device.	
6	Browse for the bitstream file. Note: Do not change the starting address from sector 0. The LatticeXP2 device will boot from sector 0.	
7	Click OK to close the SPI Flash device menu.	
8	Click OK to close the device selection menu.	
9	Click GO to program the SPI Flash device. For embedded programming, skip this step. Go to step 10 to generate the VME file instead.	
10	This is optional. For embedded programming, use the VME file generator to generate the VME file first then run the VME file to program the SPI Flash device then port the ispVME driver onto the embedded system.	

Part 2: Program the Primary Pattern into LatticeXP2 Embedded Flash

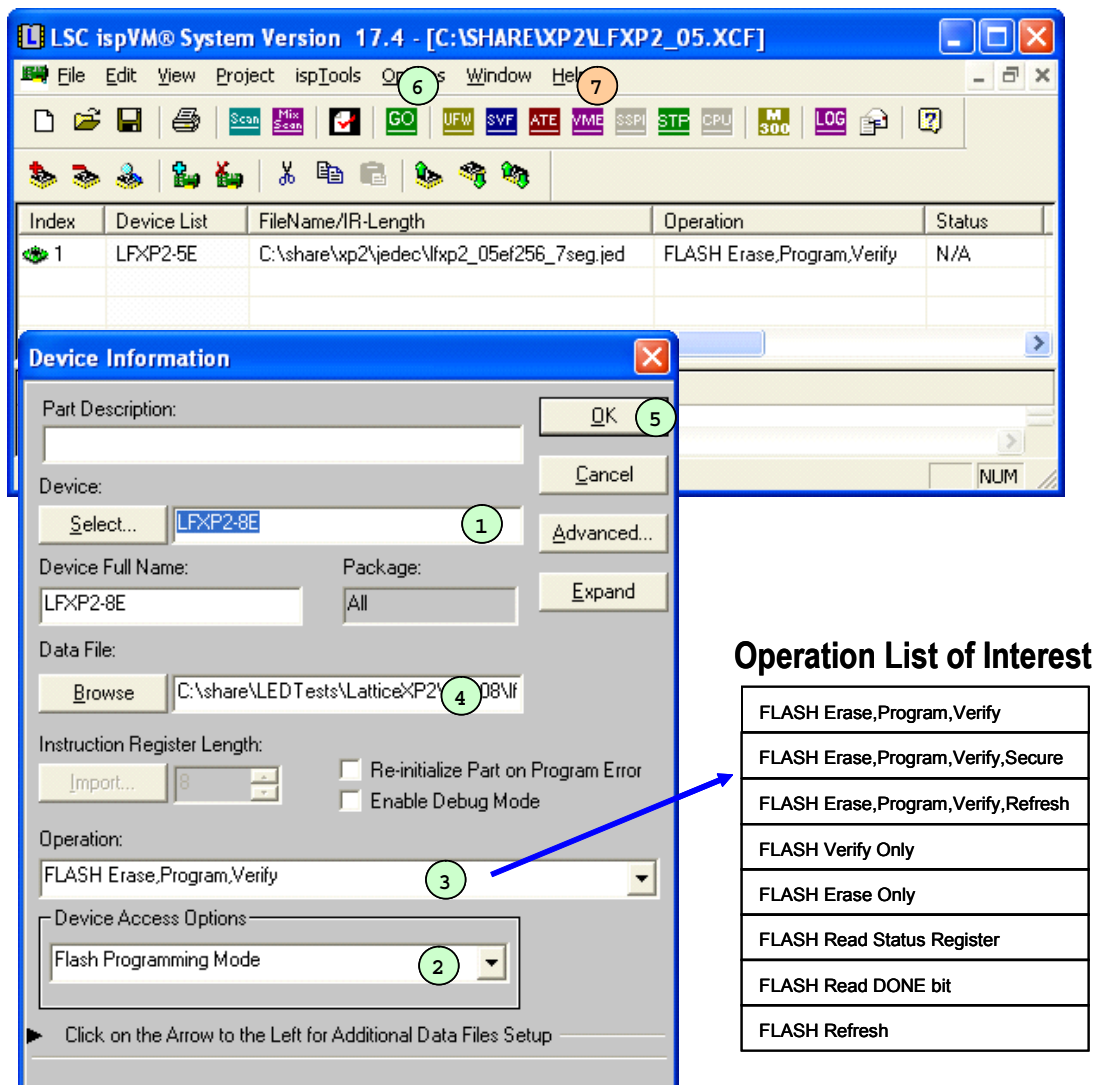
Follow the procedures shown in Figure 17-3 and Table 17-5 to program the JEDEC file into the LatticeXP2 embedded Flash using the ispVM System. There is absolutely no difference between programming the LatticeXP2 device for standard single boot and dual boot applications.

For live field upgrade of a mission critical application, Background Mode programming is strongly recommended.

Once the embedded Flash and Done fuse is programmed, it can be difficult to configure the LatticeXP2 device from the external SPI Flash device. There are two methods that can be used to test the dual boot feature does work.

1. Drive the CFG1 pin to 0. This will cause the bitstream in the SPI Flash to be the Primary pattern.
2. Use the ERASE_DONE command to erase only the Done fuse of the LatticeXP2 Embedded Flash. The only draw back of this approach is that entire LatticeXP2 Embedded Flash will need to be re-programmed. Simply programming the Done fuse will not work.

Figure 17-3. Using ispVM to Program a JEDEC into the Embedded Flash



The screenshot shows the LSC ispVM System Version 17.4 interface. The main window displays a table with columns: Index, Device List, FileName/IR-Length, Operation, and Status. A row is visible with Index 1, Device List LFXP2-5E, and FileName C:\share\xp2\jedec\lfxp2_05ef256_7seg.jed. The Operation column shows 'FLASH Erase,Program,Verify' and the Status is 'N/A'.

The 'Device Information' dialog box is open, showing the following fields:

- Part Description: (empty)
- Device: LFXP2-8E (selected from a dropdown)
- Device Full Name: LFXP2-8E
- Package: All
- Data File: C:\share\LED Tests\LatticeXP2\08\lf (selected from a dropdown)
- Instruction Register Length: 8 (selected from a dropdown)
- Re-initialize Part on Program Error: (unchecked)
- Enable Debug Mode: (unchecked)
- Operation: FLASH Erase,Program,Verify (selected from a dropdown)
- Device Access Options: Flash Programming Mode (selected from a dropdown)

The 'Operation List of Interest' table is shown to the right of the dialog box:

Operation List of Interest
FLASH Erase,Program,Verify
FLASH Erase,Program,Verify,Secure
FLASH Erase,Program,Verify,Refresh
FLASH Verify Only
FLASH Erase Only
FLASH Read Status Register
FLASH Read DONE bit
FLASH Refresh

Table 17-5. Procedure for Program a JEDEC File into the LatticeXP2 using ispVM

Steps	Description	
1	Scan or select the LatticeXP2 device.	
2	Select the Flash Programming Mode under the Device Access Options.	
3	Select the Flash Programming operation from the operation list: (Note: Due to the operations describe here are all carried out on the JTAG port, as previously noted, the PROGRAMN pin function is disabled by any activities on the JTAG port, power cycling the LatticeXP2 device is the only way to re-enable the PROGRAMN pin.)	
	Flash Background Operation	Comments
	FLASH Erase,Program,Verify	This is a Direct Mode operation. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and while programming the embedded Flash. A post programming verification of the Flash fuses is performed. If all of the Flash fuses match the data in the JEDEC file, the Flash Done fuse is programmed. The pattern from embedded Flash device into the SRAM fuses using the JTAG ISC_DISABLE instructions at the end of the operation.
	FLASH Erase,Program,Verify,Secure	This is a Direct Mode operation. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and while programming the embedded Flash. A post programming verification of the Flash fuses is performed. If all of the Flash fuses match the data in the JEDEC file, the Flash Security and Done fuses are programmed. The pattern from embedded Flash device into the SRAM fuses using the JTAG ISC_DISABLE instructions at the end of the operation.
	FLASH Erase,Program,Verify,Refresh	This is a Direct Mode operation. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and while programming the embedded Flash. A post programming verification of the Flash fuses is performed. If all of the Flash fuses match the data in the JEDEC file, the Flash Done fuse is programmed. This operation loads the pattern from embedded Flash device into the SRAM fuses using the JTAG Refresh instruction.
	FLASH Verify Only	This is a Direct Mode operation. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and while programming the embedded Flash. A verification of the Flash fuses is performed. If all of the Flash fuses match the data in the JEDEC file, the Flash Done fuse is programmed. The pattern from embedded Flash device into the SRAM fuses using the JTAG ISC_DISABLE instructions at the end of the operation.
	FLASH Erase Only	This is a Direct Mode operation. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and while erasing the embedded Flash. Since the Flash Done bit is erased, the Flash to SRAM transfer does not happen, and the device remains in the unprogrammed mode. If dual boot configuration mode is selected, and the golden is located in the external SPI Flash, the device will configure from the golden pattern contained in the external SPI Flash device.
	FLASH Read Status Register	This is a Direct Mode operation. The LatticeXP2 device will enter programming mode while the device Status Register is read and displayed.
	FLASH Read DONE bit	This is a Direct Mode operation. The LatticeXP2 device will enter programming mode while the Flash Done Bit is read and displayed.
	FLASH Refresh	This is a Direct Mode operation. This operation loads the pattern from embedded Flash device into the SRAM fuses using the JTAG Refresh instruction. The LatticeXP2 device will be forced into an erased state, by clearing (erase) the SRAM fuses, before and during the Flash to SRAM transfer.

Table 17-5. Procedure for Program a JEDEC File into the LatticeXP2 using ispVM (Continued)

Steps	Description
4	Browse for the JEDEC file.
5	Click OK to close the device selection menu.
6	Click GO to program the LatticeXP2 embedded Flash. For embedded programming, skip this step. Go to step 7 to generate the VME file instead.
7	This is optional. For embedded programming, use the VME file generator to generate the VME file first then run the VME file to program the LatticeXP2 embedded Flash device then port the ispVME driver onto the embedded system.

Reference Material

LatticeXP2 Bitstream File Format

Table 17-6 shows the format of a LatticeXP2 bitstream. The bitstream consists of a comment field, a header, the preamble, and the configuration setup, and data.

Table 17-6. LatticeXP2 Bitstream File Format

Frame	Contents	Description
Comments	(Comment String)	ASCII Comment (Argument) String and Terminator
Header	1111...1111	16 Dummy bits
	1011110110110011	16-bit Standard Bitstream Preamble (0xBDB3)
Verify ID		64 bits of command and data
Control Register 0		64 bits of command and data
Reset Address		32 bits of command and data
Write Increment		32 bits of command and data
Data 0		Data, 16-bit CRC, and Stop bits
Data 1		Data, 16-bit CRC, and Stop bits
...	...	...
Data n-1		Data, 16-bit CRC, and Stop bits
End	1111...1111	Terminator bits and 16-bit CRC
Usercode		64 bits of command and data
SED CRC		64 bits of command and data
Program Security		32 bits of command and data
Program Done		32 bits of command and data, 16-bit CRC
NOOP	1111...1111	64 bits of NOOP data
End	1111...1111	32-bit Terminator (all ones)

Note: The data in this table is intended for reference only.

Implement SPI Flash Programming on ispVM System

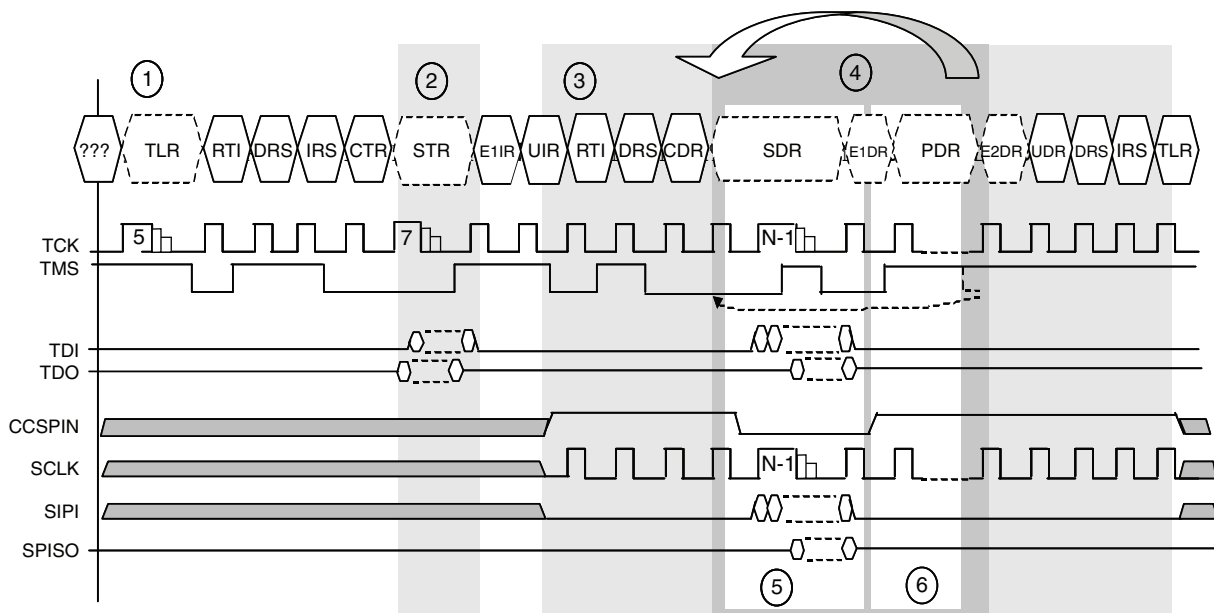
The LatticeECP2/3 and LatticeXP2 families of FPGA devices are designed to support a JTAG instruction, PROGRAM_SPI, which when executed, will effectively connect the four SPI interface signals of SPI Flash devices to four JTAG port signals.

ispVM System and ispVME takes care of the detail to program the SPI Flash devices via the JTAG port. The detail task is shown in the waveform diagram on on

Table 17-7. Description of the Hare-wired JTAG SPI Flash Programming IP

Block #	Title	Description
1	Reset JTAG Port	The standard method to set the JTAG state machine to a known state.
2	Send Instruction	Shift in the PROGRAM_SPI instruction (OPCODE = 0x0X⇌). ⇌ Indicate bit 0 first shifting direction.
3	Connect	The 4-pin JTAG port is connected to the 4-pin SPI interface. SLCK following TCK indicate connection is made.
4	Repeat	Loop around to erase by sectors and programming by pages.
5	Shift Data	Send in the command to erase a sector or shift in one page of programming data. The FPGA respond by driving the CCSPIN pin to low to gate on SCLK, SPID0, and SISPI.
6	Burn Time Delay	Drive the CCSPIN to high to command the SPI Flash device to start the erase or programming action. Wait for the required erase or programming delay time then poll the complete status. Consult the SPI Flash datasheet for the polling method required.

Figure 17-4. Waveform Diagram of the Hare-wired JTAG SPI Flash Programming IP



References

- Lattice Technical Note TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- Lattice Technical Note TN1141, [LatticeXP2 sysCONFIG Usage Guide](#)
- Lattice Technical Note TN1142, [LatticeXP2 Configuration Encryption and Security Usage Guide](#)

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Revision History

Date	Version	Change Summary
November 2010	01.0	Initial release.
August 2012	01.1	Removed references to the <i>LatticeXP2 Mission Critical Field Upgrade Usage Guide</i> .