LED/OLED Driver

March 2014 Reference Design RD1103

Introduction

A Light Emitting Diode (LED) is a semiconductor light source mainly used in signalling and lighting applications. A LED consists of anode and cathode nodes. When current is applied in a forward direction, the LED emits light. The Organic LED (OLED) is the latest development in the field of LED technology. It is a special type of LED which has a layer of organic compound. The advantage of the LED is its efficiency. It occupies a small area, consumes less power and lasts for a long duration.

In recent years there has been a surge in demand for LEDs and this translates into a rise in demand for LED controllers. PLDs and FPGAs offer an ideal solution for LED controllers as they can be easily programmed and reprogrammed for different functions. Thus a PLD and FPGA implementation for a LED controller helps designers make efficient use of LEDs.

The WISHBONE Bus interface is a free, open-source standard that is gaining popularity in digital systems that require the use of IP cores. This bus interface encourages IP reuse by defining a common interface among IP cores. That, in turn, provides portability for the system, speeds time to market, and reduces the cost of the end product.

This reference design is targeted for a LED controller to drive a GM1WA55311A LED device from Sharp Electronics. A typical application of this design includes the interface between a WISHBONE-compliant, on-board microcontroller and a LED device. This design can also be used as a reference to control other LEDs or OLEDs for similar functions.

Features

The LED/OLED Driver reference design provides a bridge between the microcontroller and the LED device via a WISHBONE bus. The microcontroller programs the duty cycle for the red, green and blue LEDs. Below is a summary of the functionalities.

- Supports red, green and blue LEDs
- Programmable duty cycle range of 0-100%
- WISHBONE Classic Interface Revision B compliant
- A non-WISHBONE compatible signal, rst_i, is an asynchronous reset signal provided for PLD or FPGA implementations

Functional Description

This design consists of three programmable registers for programming the duty cycle for the three LEDs (RGB). These registers are programmed by the microcontroller using a WISHBONE interface.

Table 1 lists the I/O ports of the design. The signals ending in “_i” indicate an input and those ending in “_o” indicate an output for WISHBONE interface.

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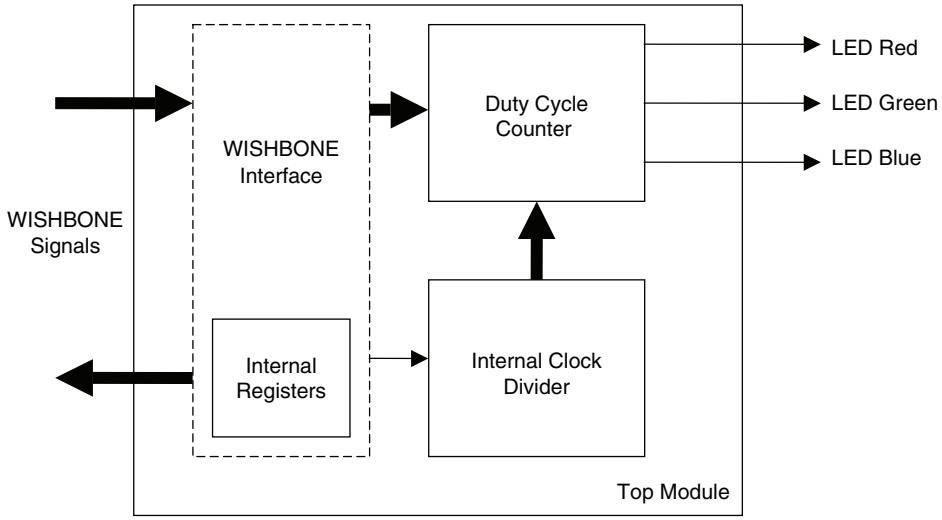
Table 1. Pin Descriptions

Signal	Width	Type	Description
WISHBONE Interface			
clk_i	1	Input	Master clock
rst_i	1	Input	Master reset (active high)
wb_dat_i	7	Input	Input data
wb_stb_i	1	Input	Strobe signal
wb_we_i	1	Input	Write enable
wb_cyc_i	1	Input	Valid bus cycle
wb_add_i	2	Input	Address
wb_ack_o	1	Output	Bus cycle acknowledgement
LED Interface			
led_red	1	Output	Enable for red LED
led_blue	1	Output	Enable for blue LED
led_green	1	Output	Enable for green LED

Design Module Description

The design has a single module as shown in Figure 1. This module includes logic for the WISHBONE interface, internal registers, the clock divider and duty cycle counter.

Figure 1. Top-Level Module



The WISHBONE interface is used to program the internal registers of the design. The internal clock generator uses either a WISHBONE interface clock or the on-chip oscillator for generating a clock for the LEDs. This generated clock is used as a duty cycle counter to drive LED outputs.

Table 2 list the internal registers of the design. These registers are used to program the duty cycle for the red, green and blue LEDs. These registers are WRITE-only registers.

Table 2. Internal Registers

Internal Register	Address	Width	Access	Description
duty_val_red	0x0	7	Write	Duty cycle for red LED
duty_val_green	0x1	7	Write	Duty cycle for green LED
duty_val_blue	0x2	7	Write	Duty cycle for blue LED

Table 3 lists descriptions of the internal register bits.

Table 3. Internal Register Bits

Internal Register	Bit#	Access	Description
duty_val_red	6:0	Write	Duty cycle for the red LED. 0 = Always OFF 100 = Always ON >0 and <100 = Partial Dimming Setting
duty_val_green	6:0	Write	Duty cycle for the green LED. 0 = Always OFF 100 = Always ON >0 and <100 = Partial Dimming Setting
duty_val_blue	6:0	Write	Duty cycle for the blue LED. 0 = Always OFF 100 = Always ON >0 and <100 = Partial Dimming Setting

Other Features

The on-chip oscillator can be used instead of the master clock to drive LED output. The on-chip oscillator clock can be used by enabling the macro OSC_CLOCK.

Common Operation Sequence

The sequence to operate the design is quite simple. Using the WISHBONE interface, program the three internal registers of the design. The design will start to drive the LED output. The internally-generated clock, which is also the clock to drive LED output, can be driven from the on-chip oscillator if the WISHBONE interface is not used.

HDL Simulation and Verification

The LED/OLED Driver reference design is simulated using a WISHBONE interface model. The model programs the internal register of the design. This model contains a write task for programming the duty cycle for the LEDs.

The following timing diagrams show the major timing milestones in the simulation.

Figure 2. Programming the Duty Val Red Register

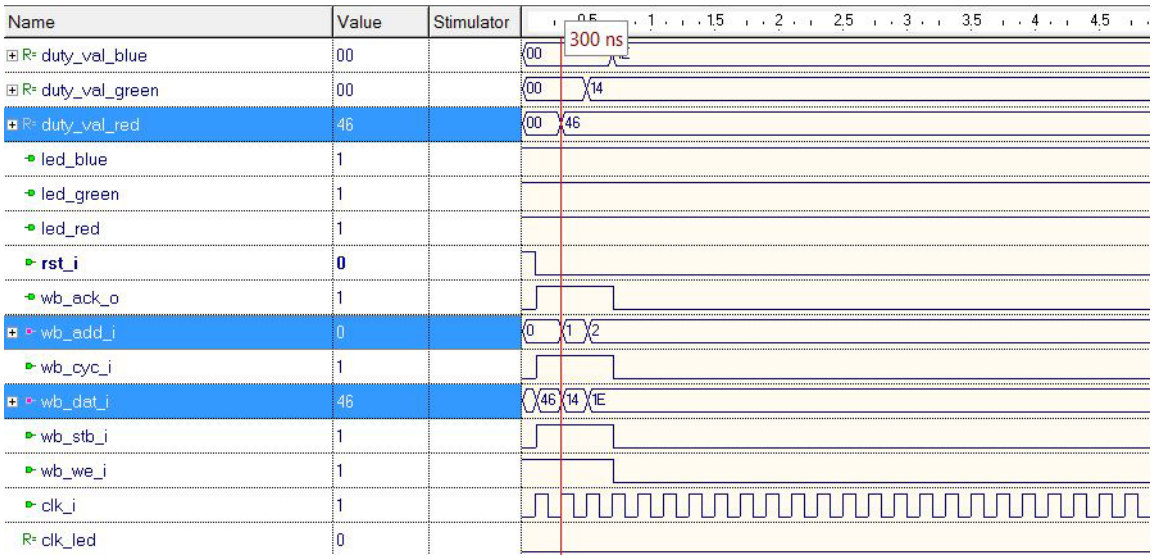


Figure 3. Programming the Duty Val Green Register

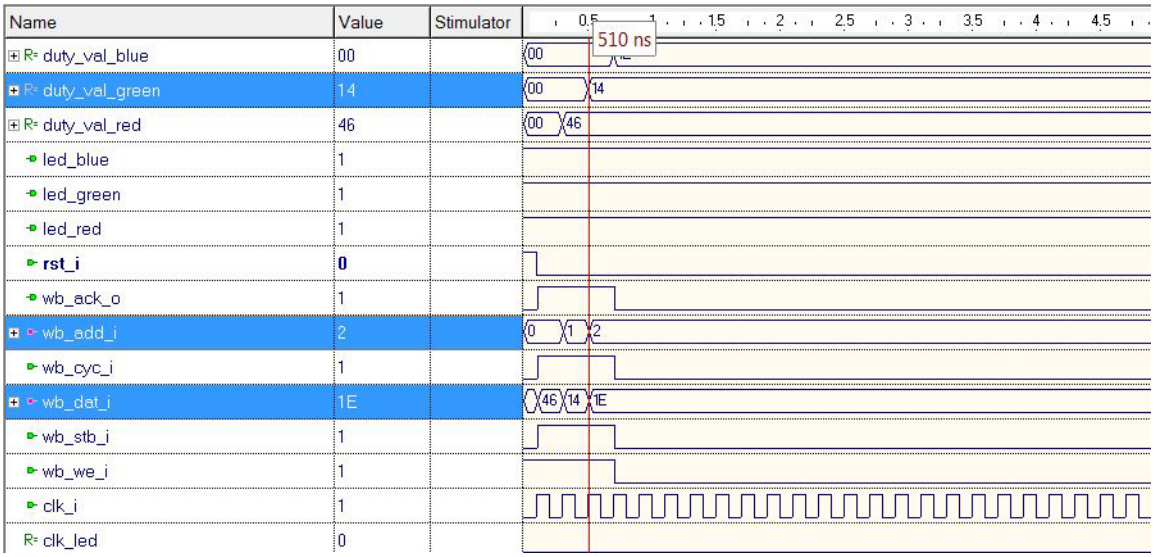


Figure 4. Programming the Duty Val Blue Register

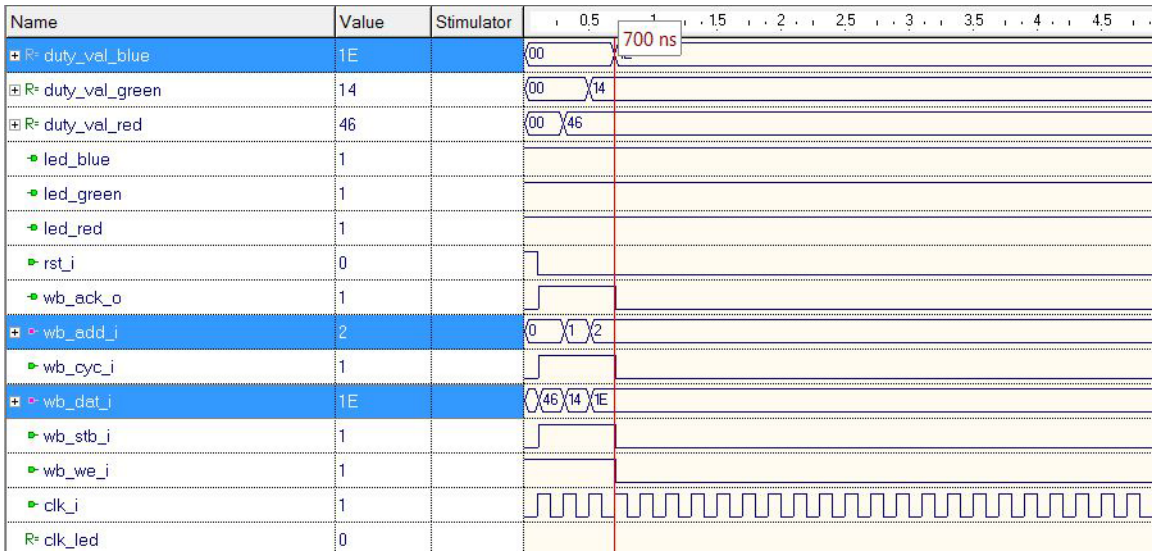
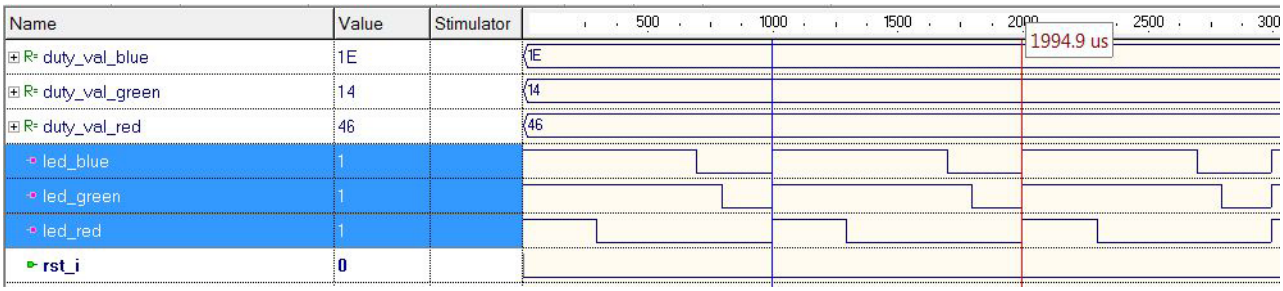


Figure 5. Output with Varying Duty Cycles



Implementation

Table 4. Performance and Resource Utilization

Family	Language	Speed Grade	Utilization	f_{MAX} (MHZ)	I/Os	Architecture Resources
MachXO3L[4]	Verilog-LSE	-6	60 LUTs	>50	18	N/A
	Verilog-Syn	-6	58 LUTs	>50	18	N/A
MachXO2™ [1]	Verilog	-4	59 LUTs	>50	18	N/A
MachXO™ [2]	Verilog	-3	54 LUTs	>50	18	N/A
ispMACH® 4000ZE[3]	Verilog	-7.5 (ns)	44 Macrocells	>50	18	N/A

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-4TG100CES, with Lattice Diamond® 1.1 and isp-LEVER® 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO-256C-3T100C, with Lattice Diamond 1.1 and ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LC4064ZE-7TN48, with ispLEVER Classic 1.4 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
4. Performance and utilization characteristics are generated using LCMXO3L-4300C-6BG256C with Lattice Diamond 3.1 design software with LSE (Lattice Synthesis Engine) and Synplify Pro®.

References

- Light Emitting Diode (GM1WA55133A) Specification from Sharp Electronics Corporation

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2010	01.0	Initial release.
March 2014	01.1	Updated Table 4, Performance and Utilization.
		Added support for MachXO3L device family.
		Updated corporate logo.
		Updated Technical Support Assistance information.