USING LOW COST, NON-VOLATILE PLDs IN SYSTEM APPLICATIONS

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Introduction

The system market is comprised of applications in telecom infrastructure, computing, high end industrial and high end medical. Power supply sequencing, voltage and current monitoring, bus bridging, voltage level translation, interface control, and temperature measurement are typical board functions found in these applications. System designers are faced with continual pressure to meet their development schedules, and need to implement designs with minimal effort and risk while maintaining maximum flexibility. By using a programmable-based approach instead of several discrete devices or Application Specific Standard Products (ASSPs), designers can accelerate their time-to-market, address system cost and space reduction, and ensure a high level of product differentiation.

PLD Usage in Typical System Application

Figure 1 shows a typical system application using a PLD performing functions such as memory interface control, power sequencing and reset, and serial interface control.

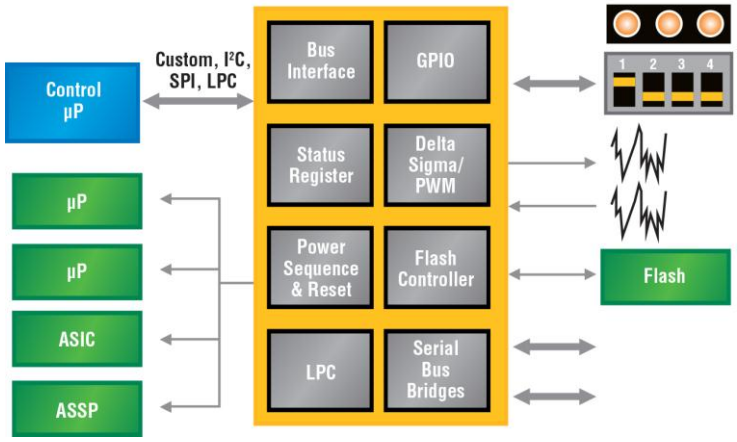

Figure 1- Typical System Application Using a PLD

In this application the PLD communicates with the microcontroller, ASIC, ASSP, LEDs and flash Memory at different voltage levels. The microcontroller monitors the status of the system through the register banks of the PLD via I^2C, SPI, or LPC interfaces. The PLD provides status indication via the LEDs and controls the interfaces to the Flash memory. The PLD manages the power-up sequence and reset for several ICs, and

provides the interface to the analog signals. Furthermore, it communicates via serial bus bridges to the other components on the board.

System Application Challenges

Typical system application challenges include:

Interfacing with Multiple Devices

As the number of devices on a board continues to increase, the number of I/Os required to interface between these devices also increases. PLDs can be used to monitor and control many signals to multiple devices. In addition, they can be used in conjunction with a microcontroller or ASSP to increase the number of available user I/O. Through the use of advanced process technology nodes, there has been a significant reduction in the size of the logic, memory, PLLs and other core functions within a PLD; however the I/O structure remains much the same as it requires special circuitry such as ESD that does not benefit as much from shrinking process geometries. This results in pad limited designs.

Reliable Operation Within a Noisy Environment

One of the primary requirements in system applications is to efficiently manage the power up and power down sequencing of devices on a board. This drives several unique requirements including instant-on, support for input hysteresis, 3.3V single power supply and single chip solution.

Instant-On

Bus bridging and control logic functions have to operate before other devices power-up within a system. This includes the ability to control the power sequencing of other devices in a particular sequence to ensure that they operate correctly.

Input Hysteresis

Low slew rate signals are frequently generated in system applications due to heavy utilization of board-level routing resources. Devices with input hysteresis provide noise immunity for slow rising inputs, improving the overall reliability of the system.

3.3V Power Supply

In system applications, typically the PLD operates from the auxiliary power supply as this is the first to be powered-on and the last to be powered off during a power cycle. For many systems the auxiliary rail is 3.3-volts. The ability to operate directly from this rail avoids the expense and increased component count of an additional regulator.

Single Chip

Programmable devices that do not require an additional PROM or configuration device contribute to the reliability of the system by operating independently and minimizing the component count.

Board Area Reduction Through Functional Integration

In order to satisfy customer demand for changing features and standards, designers are often faced with the challenge of supporting a high level of functionality with differentiating features while at the same time trying to reduce the total system cost. Discrete devices and ASSPs do not provide the required differentiation, and increase the bill of materials (BOM) and occupy a large amount of board area. Application Specific Integrated Circuits (ASICs) provide customization and functional integration, but will adversely affect the delivery schedules and development cost due to their expensive mask sets. Solutions that can provide functional integration and product differentiation while saving board space and reducing costs are gaining traction in the system market.

Implementing System Functions Using MachXO2 PLDs

Lattice's MachXO2 PLD family is an ideal fit for functions used in the system applications described above. Combining optimized lookup table (LUT) architecture with 65-nm embedded Flash process technology, MachXO2 devices provide a flexible "do-it-all" solution for system designs.

MachXO2 devices enable system designers to interface with a large number of low cost I/O at different voltage levels, improve overall system robustness and provide increased functional integration, all in a single device.

The following describes the features and benefits of the MachXO2 family that address the challenges of system designs.

Large Number of Low Cost I/O

MachXO2 devices provide up to 335 user I/O in a broad range of package options. Pre engineered source synchronous I/Os in addition to a comprehensive support of I/O standards and several features such as default pull down, hot socketing and input hysteresis enable flexible implementation of designs.

Triple Staggered I/O Pads

MachXO2 devices are designed to be pad limited. The I/O pads are laid out in double or triple staggered I/O rings depending on device density thereby, the die size for a given number of I/Os. This is particularly attractive for system functions such as voltage translation, bus bridging and interface control which require a higher ratio of I/Os compared to the logic.

Asymmetrical Banking Scheme

System applications typically use 3.3V LVCMOS I/O with a limited number of other I/O voltages and standards. With symmetrical I/O banks, designers often find themselves underutilizing I/O banks for lower voltages. MachXO2 devices provide asymmetrical I/O banking that enables designers to maximize I/O usage. This is beneficial for voltage level translation and bridging functions where a limited number of I/Os require a different supply voltage offering flexibility and maximizing I/O usage.

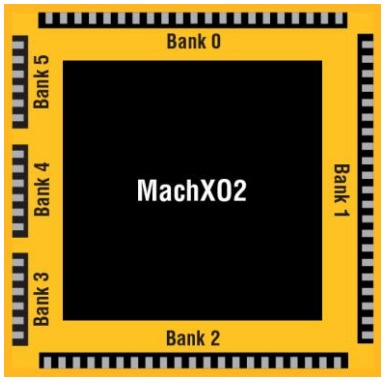

Figure 2- Asymmetrical I/O Banks in MachXO2-2000, 4000 and 7000 Devices

Low cost BGA packages

The MachXO2 family offers a broad range of low cost package options to save space, cost per I/O, and manufacturing expense. Electrical simulations were used to identify the lowest cost substrate design features that would enable the packages to support the device performance targets. These packages are designed such that all the I/O and power supply connections break out in two to four layers of PCB routing. This avoids use of higher cost manufacturing techniques such as buried or blind vias and laser drilled vias. I/O assignment on MachXO2 packages was done to enable density migration within the same package, eliminating the cost and lead time required for a new board spin in the event of a design change.

Robust Design

Several features of the MachXO2 family contribute to the robustness of the design and its ability to function in noisy environments such as:

Sub 1ms Instant-on

The combination of Flash and SRAM within the same device provides significant advantages for remote field upgrades as well as instant-on non-volatile operation. Upon power-up, the configuration bits (From a Non-Volatile FLASH) are loaded into SRAM of the device, enabling instant-on operation in less than 1ms after power-up.

Input Hysteresis

Inherent parasitic capacitance, resistance and inductance in the input path and input buffer cause an input signal to have an infinite amount of rise or fall time. As shown in Figure 3, if an input signal becomes too slow the noise around the device's input voltage threshold can cause multiple state changes.

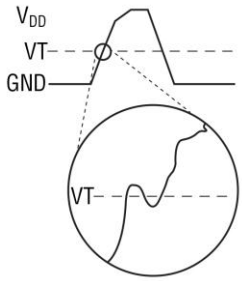

Figure 3- Noise Around the Input Voltage Threshold

The MachXO2 devices' Schmitt-trigger buffers enable conversion of a slow or noisy signal into a clean one before passing it to the core of the PLD, providing reliable operation in a noisy environment. Schmitt-trigger buffers have transfer functions with hysteresis as shown in Figure 4 below.

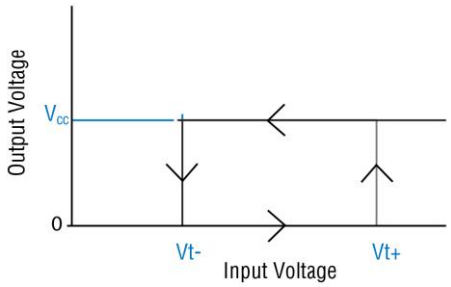

Figure 4- Hysteresis Curve

As the input voltage rises from 0V towards the lower threshold, the output will remain at 0 volts. Only when the input exceeds the higher threshold will the output jump up to Vcc. At this point, reducing the input voltage will not cause the output to drop to zero immediately. This only happens when the input voltage is reduced to the lower threshold voltage. Applying the hysteresis theory to the noisy signal shown in Figure 5, will result in an almost perfect output to be recovered from a slow and very noisy input.

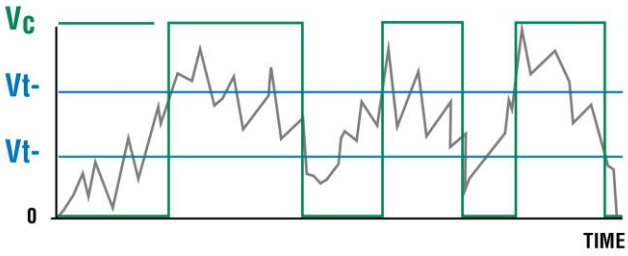

Figure 5- Applying Hysteresis to a Noisy Signal

Input Buffers with Default Pull-down

The default state of I/O termination for MachXO2 devices is pull-down. This provides protection against problems caused by default pull-up (shark-fin behavior) in the event that the connected devices on the board reset or trigger from an active high signal.

Ability to Operate from Single Power Supply

MachXO2 devices require only one voltage supply. They can operate directly from one rail avoiding the need for an additional regulator, which reduces the component count and increases system reliability.

Single Chip

MachXO2 devices combine SRAM and Flash configuration memory within the same device, eliminating the need for a PROM and/or additional memory for device configuration.

High Level of Functional Integration

MachXO2 devices enable a high level of system integration due to their architectural attributes such as on-chip User Flash Memory (UFM), oscillator, PLLs and hardened I^2C, SPI and timer/counter functions, resulting in reduced board area, component count, and total system cost.

Figure 6 shows the integration of discrete logic such as an I/O expander, voltage level and bus bridging translators, voltage regulator, clock sources and configuration devices; all in a single MachXO2 device.

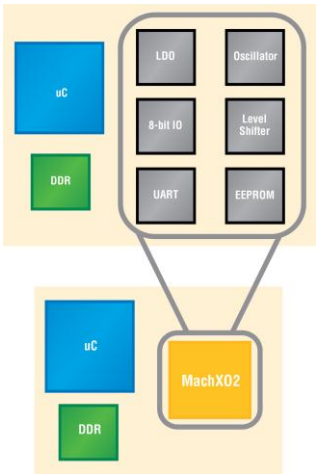

Figure 6- MachXO2 functional integration

Integrate External Non-volatile Memory

MachXO2 devices include up to 256Kbits of embedded Flash memory. This on-chip User Flash Memory (UFM) enables the MachXO2 devices to integrate the external non-volatile memory, and can be used for a variety of applications, including storing a portion of the configuration image, storing PROM data or as a general purpose User Flash Memory.

Reduce Number of Oscillators

MachXO2 devices have an internal oscillator with a nominal accuracy of +/- 5% that can be used as a clock source in a design, eliminating the need for an external oscillator.

Hardened SPI, I^2C, Timer/Counter

SPI and I^2C controllers and timer/counters are among the most commonly implemented functions in system designs. Designers often implement SPI or I^2C bus expansion in PLDs. Timer/Counters are also frequently used to generate status signals. All MachXO2 devices include hardened implementations of these commonly used functions. With hardened I^2C, SPI and timer/counter functions, designers can save up to 600 LUTs for additional logic implementation in their designs. Table 1 shows the savings in logic requirements that can be realized by hardening commonly used control functions.

Function	Typical LUTs required in PLDs	Typical LUTs required in MachXO2 Devices
SPI Master	115	0
I2C Master	234	0
Timer/Counter	50-80	0

Table 1- Typical LUT Saving by Using Hardened I^2C, SPI and Timer/Counter

Free Design Tools to Accelerate Development Time

Designers can start designing with MachXO2 devices using the Lattice Diamond v1.1 software, which can be downloaded for free from the Lattice website. Alternatively, designers can also use the free ispLEVER® v8.1 SP1 Starter software with an installed control pack that can be downloaded from the Lattice website.

A comprehensive suite of reference designs, optimized for system applications can be downloaded for free from the Lattice Website.

Table 2 shows MachXO2 reference designs optimized for system designs.

System Management	Processors and Peripherals
Control Link Serial Interface	Lattice Mico8 Microcontroller
Delta Sigma ADC	LCD Controller (WISHBONE Compatible)
PWM Fan Control	I^2C Bus Controller for EEPROM
I^2S Controller	SPI Controller (WISHBONE Compatible
PMBUS Controller	I^2C Master (WISHBONE Compatible)
Single Wire Temperature Sensor Interface	UART WISHBONE Compatible
SMBUS Controller	LED/OLED Driver

Memory Controllers
Compact Flash
Fast Page Mode SDRAM
NOR Flash
SD Controller with SD Bus
NAND Flash
SDR DRAM
Flash Controller with Wear Leveling

Table 2- Reference Designs for MachXO2 Devices

Conclusion

MachXO2 PLDs are ideal for implementing system functions commonly found in telecom infrastructure, computing, high end industrial and high end medical applications. They provide several key system benefits that help reduce total system cost. The free design tools and reference designs provide designers a comprehensive and convenient solution to accelerate their system designs quickly and efficiently.