I^2S Controller with WISHBONE Interface

March 2014 | Reference Design RD1101

Introduction

The I^2S bus (Inter-IC Sound bus) is a 3-wire, half-duplex serial link for connecting digital audio devices in an electronic system. The bus handles audio data and clocks separately to minimize jitter that may cause data distortion in the digital analog system. Invented by Philips Semiconductor, the I^2S bus is widely used by equipment and IC manufacturers.

This reference design implements an I^2S transmit master or I^2S receive master with a WISHBONE interface.

Features

The following are some key characteristics of this design:

- Configurable as an I^2S transmit master or I^2S receive master
- WISHBONE interface
- Configurable sample data resolution from 16 to 32 bits
- Configurable data width from 16 to 32 bits
- Configurable data buffer from 16 to 256 words deep
- Active high interrupt output

Functional Description

This design is configurable via the parameter IS_RECEIVER. When IS_RECEIVER is set to '1', it is configured as an I^2S transmit master; otherwise, it is configured as an I^2S receive master. Figure 1 shows the design used as an I^2S transmit master in an I^2S system. Figure 2 shows the design used as an I^2S receive master in an I^2S system.

Figure 1. I^2S Transmit Master Connecting to Peripherals

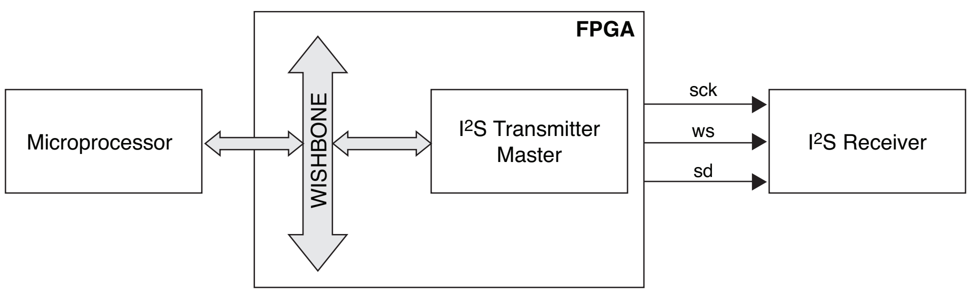
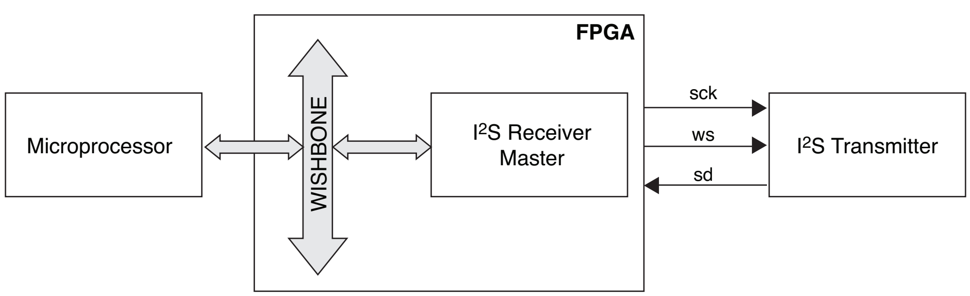


Figure 2. I^2S Receive Master Connecting to Peripherals



The timing of the I²S signals is shown as Figure 3. The timing relationship among the signals is applicable for both transmit or receive modes.

Figure 3. I²S Signal Timing

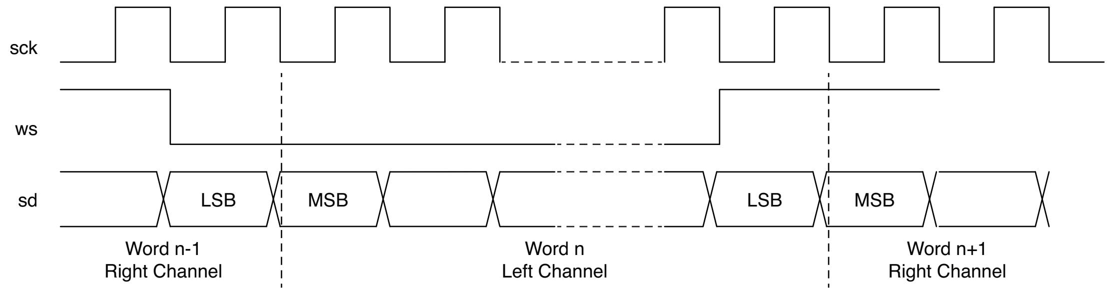


Table 1. I²S Transmit or Receive Master I/O Interface Descriptions

Signal	Direction	Width	Active State	Description
WISHBONE Interface				
wb_clk_i	Input	1	N/A	WISHBONE clock signal
wb_rst_i	Input	1	High	WISHBONE reset signal
wb_sel_i	Input	1	High	WISHBONE select signal
wb_stb_i	Input	1	High	WISHBONE strobe signal
wb_we_i	Input	1	1 = Write 0 = Read	WISHBONE write or read signal
wb_cyc_i	Input	1	High	WISHBONE cycle signal
wb_bte_i	Input	2	N/A	WISHBONE burst type signal. This design only supports linear burst (‘00’). Other values treated as classic cycle.
wb_cti_i	Input	3	N/A	WISHBONE cycle type identifier signal. This design only supports the cycle type defined as ‘000’, ‘010’ and ‘111’. Other values treated as classic cycle.
wb_adr_i	Input	5-9	N/A	WISHBONE address signal
wb_dat_i	Input	16-32	N/A	WISHBONE data input signal
wb_ack_o	Output	1	High	WISHBONE acknowledge signal
wb_dat_o	Output	16-32	N/A	WISHBONE data output signal
I²S Interface				
i2s_sd_i	Input	1	N/A	I²S data input signal. When the design used as a transmitter, this signal is ignored.
i2s_sd_o	Output	1	N/A	I²S data output signal. When the design used as a receiver, this signal is ignored.
i2s_sck_o	Output	1	N/A	I²S bit clock signal
i2s_ws_o	Output	1	N/A	I²S word select signal
Interrupt				
rx_int_o	Output	1	High	Interrupt signal when the design is used as a receiver. When the design is used as a transmitter, this signal is ignored.
tx_int_o	Output	1	High	Interrupt signal when the design is used as a transmitter. When the design used as a receiver, this signal is ignored.

Design Modules

WISHBONE Interface

Whether this design is used as an I²S transmit master or an I²S receive master, this design has a standard WISHBONE slave bus, which connects the I²S with a microprocessor as shown in Figures 1 and 2. From the WISHBONE bus, the I^2S appears as a set of addressable registers or buffers that can be read or written. From these registers, the processor can transmit and receive data and control the operation of the I^2S.

The WISHBONE slave bus supports WISHBONE Classic bus cycles as well as Feedback bus cycles. When the WISHBONE master launches Feedback bus cycles, this design only supports the Cycle Type Identifier (signal wb_cyc_o) defined as ‘000’, ‘010’ and ‘111’; other values are treated as Classic Cycle. This design only supports burst types defined as Linear burst (signal wb_bte_o is defined as ‘00’); other values are treated as Classic Cycle.

The width of the WISHBONE address and data are defined by the parameters ADDR_WIDTH and DATA_WIDTH in the source code file. The value of ADDR _WIDTH ranges from 5 to 9 bits and the value of DATA _WIDTH ranges from 16 to 32 bits. Table 2 describes the parameters used in this design.

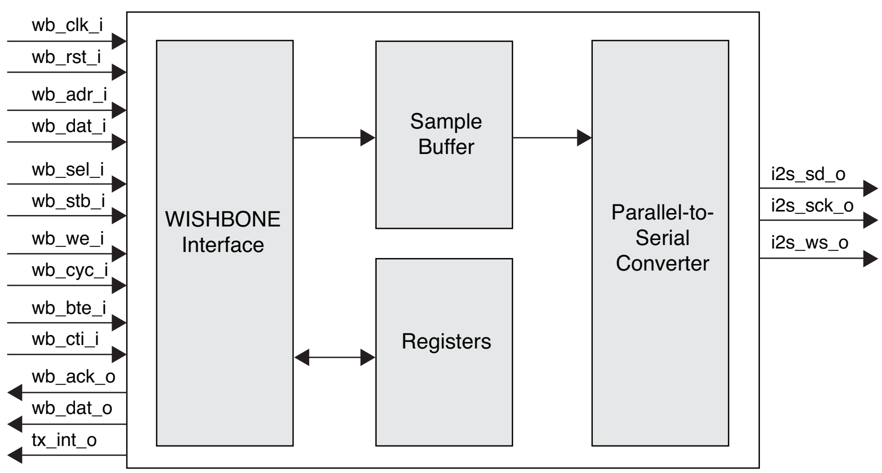
Table 2. Parameter Descriptions

Parameter	Description	Value
IS_RECEIVER	Specifies whether this design is used as an I^2S transmitter or receiver	1 = I^2S receive master 0 = I^2S transmit master
ADDR_WIDTH	Specifies the WISHBONE bus address width	5-9
DATA _WIDTH	Specifies the WISHBONE bus data width	16-32

I^2S Transmit Master

The functional block diagram of the design used as an I^2S transmit master is shown in Figure 4.

Figure 4. I^2S Transmit Master Functional Block Diagram



Register Descriptions

Two registers are used to interact with the WISHBONE bus and I^2S when this design is used as an I^2S transmit master. A description of each of these registers is shown in Table 3. Further information about these registers can be found in Tables 4 and 5.

Table 3. Register Descriptions for I^2S Transmit Master

Register	Width	WISHBONE Access	WISHBONE Address	Description
REG_TXCONFIG	16	R/W	0x0	Configuration Register. This register controls the operation of the I^2S transmit.
REG_TXINTSTAT	16	R/W	0x1	Interrupt Register. This register controls the generation of the interrupt.

Table 4. Configuration Register Bit Definitions for I^{2}S Transmit Master

Bit Name	Bit	WISHBONE Access	Description
TXEN	0	R/W	0: Transmit master is disabled 1: Transmit master is enabled
TINTEN	1	R/W	0: Interrupt output is disabled 1: Interrupt output is enabled
TSWAP	2	R/W	0: Left channel is stored on even addresses of the sample buffer 1: Left channel is stored on odd addresses of the sample buffer
MLSBF	3	R/W	Mask lower sample buffer empty interrupt
MHSBF	4	R/W	Mask higher sample buffer empty interrupt
RES	10:5	R/W	Sample data resolution. Number of bits that are transmitted from each word in the sample buffer. Valid range is 16 to 32 bits.
RATIO	15:11	R/W	Clock divider for the transmit frequency. The WISHBONE bus clock is divided by a factor of (1+RATIO) to generate the serial transmit clock, sck.

The TXEN bit disables or enables the I2S transmitter. When this bit is set to '1', the Parallel-to-Serial converter (shown in Figure 4) is enabled; otherwise the I2S transmitter does not transmit and the output is (high or low?, or the last value?).

The TINTEN, MLSBF and MHSBF bits control the generation of the interrupt output (signal tx_int_o).

- When the TINTEN bit is set to '0', the signal tx_int_o is inactive.
- When the TINTEN bit is set to '1' and the MHSBF and MLSBF bits are set to '0', the signal tx_int_o is inactive.
- When the TINTEN and MLSBF bits are set to '1', the signal tx_int_o is active if the data in the lower half of the sample buffer has been transmitted by the I2S transmit master.
- When the TINTEN and MHSBF bits are set to '1', the signal tx_int_o is active if the data in the higher half of the sample buffer has been transmitted by the I2S transmit master.

When the TSWAP bit is set to '0', the data stored in the even addresses of the sample buffer is transferred when the I2S word select signal, i2s_ws_o, is low. Under the same condition, data stored in the odd addresses of the sample buffer is transmitted when i2s_ws_o is high.

When the TSWAP bit is set to '1', the polarity of the I2S word select signal, i2s_ws_o, has a different effect on the transmit data. When i2s_ws_o is high, data stored in the even addresses of the sample buffer is transferred. Otherwise, data stored in the odd addresses of the sample buffer is transmitted.

The RES bits control the number of bits that are transmitted from each item of data in the sample buffer. For example, if RES is equal to 18 and the parameter DATA _WIDTH is equal to 24, then only the lower 18 bits of data stored in the sample buffer are transmitted and the higher six bits of data are ignored. The valid range of RES is 16 to 32 bits and must be less than or equal to the value of the parameter DATA _WIDTH. If the value of RES is less than 16 or more than 32 bits, RES is set to the default value of 16.

The RATIO bits control the frequency of the I^{2}S bit clock, i2s_sck_o.

$$\text{Frequency of i2s\_sck\_o} = \frac{\text{Frequency of wb\_clk\_i}}{2 * (\text{RATIO} + 2)}$$

Table 5. Bit Descriptions of the Interrupt Register for I²S Transmit

Bit Name	Bit	WISHBONE Access	Description
LSBF	0	R/W	Lower part of sample buffer empty
HSBF	1	R/W	Higher part of sample buffer empty
—	15:2		Unused

The LSBF bit is set to '1' when the data stored in the lower part of the sample buffer has been transmitted by the I2S transmitter. If the MLSBF and TINTEN bits are set to '1', the signal tx_int_o is active. The LSBF is set to '0' when a '1' is written to this bit.

The HSBF bit is set to '1' when the data stored in the higher part of the sample buffer has been transmitted by the I2S transmitter. If the MHSBF and TINTEN bits are set to '1', the signal tx_int_o is active. The HSBF is set to '0' when a '1' is written to this bit.

The interrupt signal becomes inactive when the LSBF and HSBF bits are both cleared.

Transmit Sample Buffer

The sample buffer is divided into two equal parts, the lower and higher parts. The addresses of the lower part are from 0 to 2**(ADDR_WIDTH-2) -1; and the addresses of the higher part are from 2**(ADDR_WIDTH-2) to 2**(ADDR_WIDTH-1) -1.

When this design is used as an I²S transmit master, the WISHBONE master can only write data to the sample buffer. When the WISHBONE master writes data to the sample buffer, the most significant bit of the signal wb_adr_i must be set to '1'. This indicates the WISHBONE access configuration register or interrupt register if the most significant bit of signal wb_adr_i is set to '0'.

Parallel-to-Serial Converter

If the TXEN bit is set to '1', the parallel-to-serial converter generates the signals i2s_sck_o and i2s_ws_o based on the setting of the configuration register. Meanwhile it reads data from the sample buffer and transmits serial data on the i2s_sd_o line.

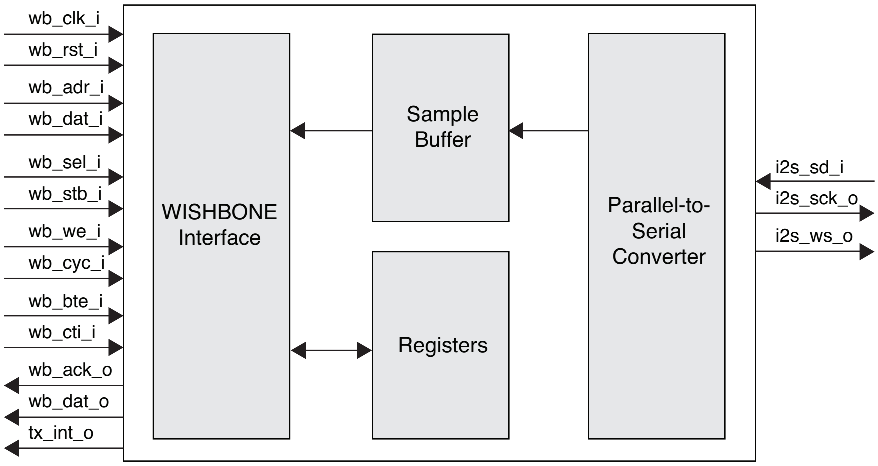
Operation sequence when this design is used as an I²S transmit master:

1. Set parameter IS_RECEIVER to 0.
2. Set parameters ADDR_WIDTH and DATA _WIDTH to the appropriate values.
3. Write data to the sample buffer (the most significant bit of signal wb_adr_i must be set to '1').
4. Set the configuration register to the appropriate value. Enable interrupt output and last enable I²S transmit master.
5. If the signal tx_int_o is active, read interrupt register. If the LSBF bit is '1', this indicates the data in the lower part of the sample buffer has been transmitted and can be filled with new data. Write a '1' to the LSBF bit to clear the interrupt. Conversely, if the bit HSBF is '1', this indicates the data in the higher part of the sample buffer has been transmitted and can be filled with new data. Write a '1' to the HSBF bit to clear the interrupt.
6. If all data has been transmitted, set TXEN to '0' to disable the I²S transmit master.

I²S Receive Master

If the parameter IS_RECEIVER is set to '1', this design is used as an I²S receive master. The functional block diagram of the I²S receive master is shown in Figure 5.

Figure 5. I^2S Receive Master Functional Block Diagram



Register Descriptions

Two registers are used to interact with the WISHBONE bus and the I^2S when this design works as an I^2S receive master. A description of each of these registers is shown in Table 6. Further information about the two registers can be found in Tables 7 and 8.

Table 6. I^2S Receive Master Register Descriptions

Register	Width	WISHBONE Access	WISHBONE Address	Description
REG_TXCONFIG	16	R/W	0x0	Configuration Register. This register controls the operation of the I^2S receive.
REG_TXINTSTAT	16	R/W	0x1	Interrupt Register. This register control the generation of the interrupt.

Table 7. I^2S Receive Configuration Register Bit Descriptions

Bit	Width (Bits)	WISHBONE Access	Description
RXEN	0	R/W	0: Receive master is disabled 1: Receive master is enabled
RINTEN	1	R/W	0: Interrupt output is disabled 1: Interrupt output is enabled
RSWAP	2	R/W	0: Left channel is stored on the even addresses of the sample buffer 1: Left channel is stored on the odd addresses of the sample buffer
MLSBF	3	R/W	Mask lower sample buffer full interrupt
MHSBF	4	R/W	Mask higher sample buffer full interrupt
RES	10:5	R/W	Sample data resolution. Number of bits that are stored in each word in the sample buffer. Valid range is 16 to 32 bits.
RATIO	15:11	R/W	Clock divider for the transmit frequency. The WISHBONE bus clock is divided by a factor of (1+RATIO) to generate the serial transmit clock, sck.

The RXEN bit disables or enables the I2S receive. When this bit is set to ‘1’, the serial-to-parallel converter (shown in Figure 5) is enabled; when this bit is set to ‘0’, the serial-to-parallel converter is disabled.

The RINTEN, MLSBF and MHSBF bits control the generation of interrupt output (signal rx_int_o).

- When the RINTEN bit is set to ‘0’, the signal rx_int_o is inactive.

- When the RINTEN bit is set to '1' and the MHSBF and MLSBF bits are set to '0', the signal rx _int_o is inactive.
- When the RINTEN and MLSBF bits are set to '1', the signal rx_int_o is active if the data in the lower half of the sample buffer is full.
- When the RINTEN and MHSBF bits are set to '1', the signal rx_int_o is active if the data in the higher half of the sample buffer is full.

When the RSWAP bit is set to '0', the data received when the I2S word select signal, i2s_ws_o, is low are stored in the even addresses of the sample buffer. Likewise, the data received when i2s_ws_o is high are stored in the odd addresses of the sample buffer.

When the RSWAP bit is set to '1', the data received when i2s_ws_o is high are stored in the even addresses of the sample buffer. The data received when i2s_ws_o is low are stored in the odd addresses of the sample buffer.

The RES bits control the number of bits that are received from the i2s_sd_i line of each I2S data. For example, if RES is equal to 18 and the parameter DATA _WIDTH is equal to 24, then the lower 18 bits of data stored in the sample buffer are filled with data received from the i2s_sd_i port and the higher six bits are filled with zero. The valid range of RES is 16 to 32 bits and must be less than or equal to the value of the parameter DATA _WIDTH. If the value of RES is less than 16 or more than 32 bits, the RES is set to the default value of 16.

The RATIO bits control the frequency of the I^2S bit clock, i2s_sck_o.

$$\text{Frequency of i2s\_sck\_o} = \frac{\text{Frequency of wb\_clk\_i}}{2 * (\text{RATIO} + 2)}$$

Table 8. Interrupt Register Bit Descriptions for the I^2S Receive Master

Bit Name	Bit	WISHBONE Access	Description
LSBF	0	R/W	Lower part of sample buffer full
HSBF	1	R/W	Higher part of sample buffer full
—	15:2		Unused

The LSBF bit is set to '1' when the lower part of the sample buffer has been filled with received data. If the MLSBF and RINTEN bits are set to '1', the signal rx_int_o is activated. The LSBF is set to '0' when a '1' is written to this bit.

The HSBF bit is set to '1' when the higher part of the sample buffer has been filled with received data. If the MHSBF and RINTEN bits are set to '1', the signal rx_int_o becomes active. The HSBF is set to '0' when a '1' is written to this bit.

The interrupt signal goes inactive when the LSBF and HSBF bit are both cleared.

Receive Sample Buffers

The sample buffer is divided into two equal parts, the lower and higher parts. The addresses of the lower part are from 0 to 2**(ADDR_WIDTH-2) -1; and the addresses of the higher part are from 2**(ADDR_WIDTH-2) to 2**(ADDR_WIDTH-1) -1.

When this design is used as an I^2S receive master, the WISHBONE master can only read data from the sample buffer. When the WISHBONE master readw data from the sample buffer, the most significant bit of the signal wb_adr_i must be set to '1'.

Serial-to-Parallel Converter

If the RXEN bit is set to '1', the serial-to-parallel converter generates the signals i2s_sck_o and i2s_ws_o based on the setting of the configuration register. It reads data from the signal i2s_sd_i and stores parallel data in the sample buffer.

The operation sequence when this design is used as I²S receive master is as follows:

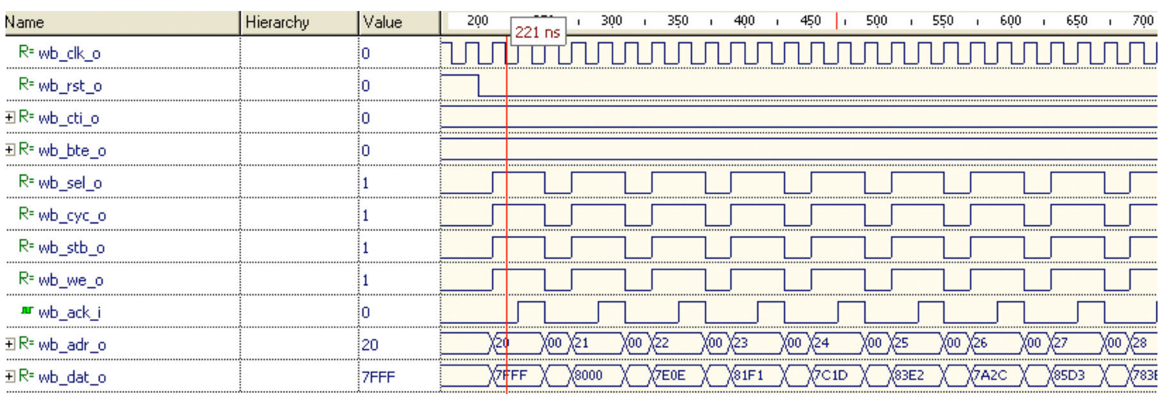
1. Set the parameter IS_RECEIVER to 1.
2. Set the parameters ADDR_WIDTH and DATA _WIDTH to the appropriate values.
3. Set the configuration register to the appropriate value, enable the interrupt output and the I²S receive master.
4. If the signal rx_int_o is active, read the interrupt register. If the LSBF bit is ‘1’, this indicates that the data in the lower part of the sample buffer is full and can be read by the WISHBONE master. Write a ‘1’ to the LSBF bit to clear the interrupt. However, if the bit HSBF is a ‘1’, this indicates that the data in the higher part of the sample buffer is full and can be read by the WISHBONE master. Write a ‘1’ to the HSBF bit to clear the interrupt.
5. If all data have been received, set RXEN to ‘0’ to disable the I²S receive master.

Test Bench Description

The test bench simulates the design as an I²S transmit master or an I²S receive master. In both cases, the parameter ADDR_WIDTH is set to 6 and DATA _WIDTH is set to 16 for the following simulation results.

For the I²S transmit master, the test bench first writes data to the sample buffer after reset with the WISHBONE classic cycle.

Figure 6. Writing Data to the Sample Buffer



The processor writes 0x3a1b to the configuration register through the WISHBONE bus and waits for the signal tx_int_o be active.

Figure 7. Writing 0x3a1b to the Configuration Register

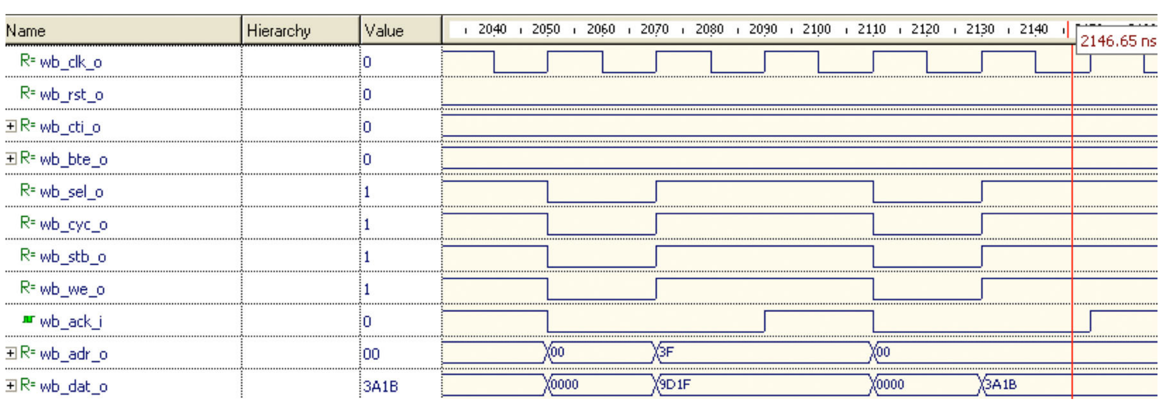
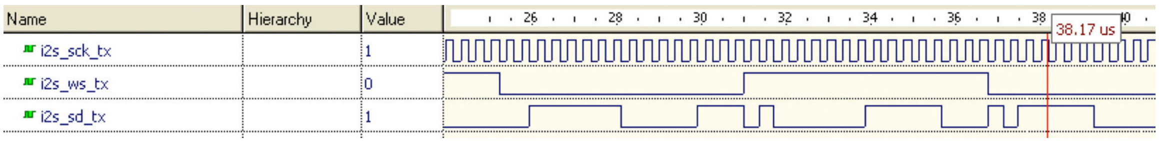


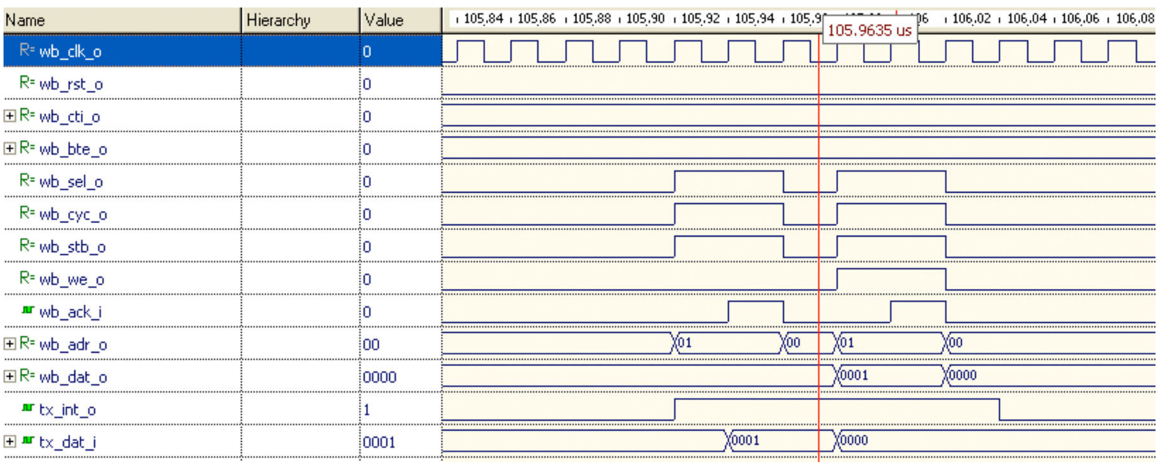
Figure 8 shows the timing relationship of the I²S signals when the TXEN bit is set to ‘1’.

Figure 8. I²S Signal Timing



When the signal tx_int_o is active, the processor reads the interrupt register and then writes a ‘1’ to the corresponding bit to clear the interrupt.

Figure 9. I²S Read and Write Interrupt Register



For the I²S receive master, the test bench first writes 0x3a1f to the configuration register.

Figure 10. Writing 0x3a1f to the Configuration Register

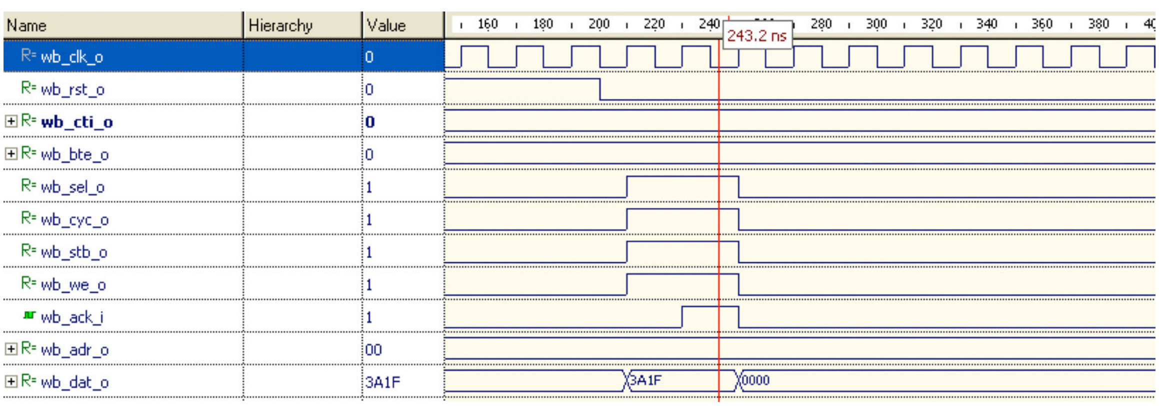
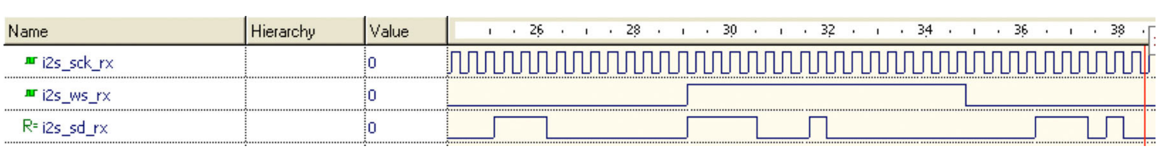


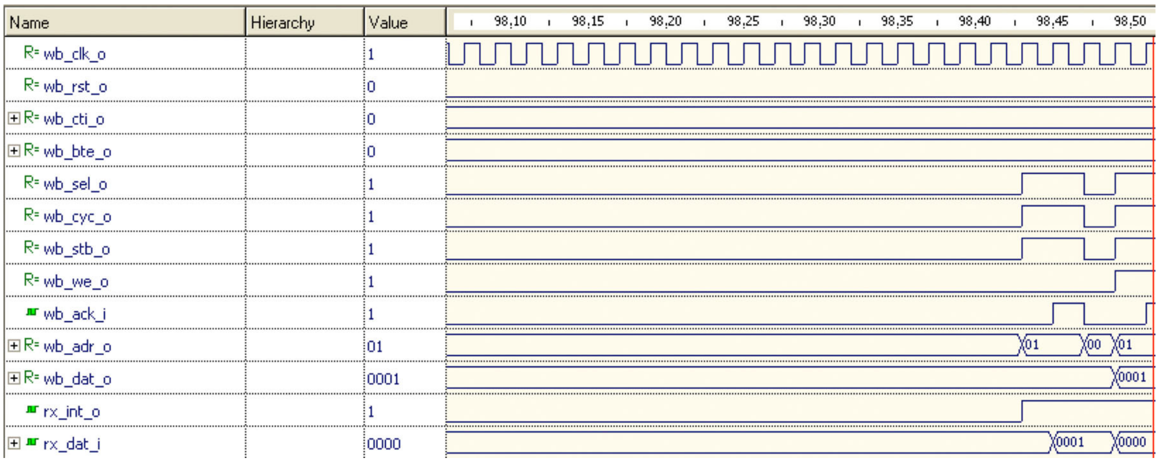
Figure 11 shows the timing relationship of I²S signals when the RXEN bit is set to ‘1’.

Figure 11. I²S Signal Timing



When the signal rx_int_o is active, the processor reads the interrupt register and then writes a ‘1’ to the corresponding bit to clear the interrupt.

Figure 12. I^2S Read and Write Interrupt Register



Implementation

Table 9 lists the implementation results when the design is configured as an I^2S transmit master with parameter ADDR_WIDTH set to 6 and DATA _WIDTH set to 16. The implementation results may vary depending on the parameter values.

Table 9. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
MachXO3L[4]	Verilog-LSE	-6	225	>50	56	N/A
	Verilog-Syn	-6	289	>50	56	N/A
	VHDL-LSE	-6	227	>50	56	N/A
	VHDL-Syn	-6	255	>50	56	N/A
MachXO2™ [1]	Verilog	-4	241	>50	55	N/A
	VHDL	-4	232	>50	55	N/A
MachXO™ [2]	Verilog	-3	245	>50	55	N/A
	VHDL	-3	236	>50	55	N/A

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-4TG100CES, with Lattice Diamond® 1.1 or ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO1200C-3T100C, with Lattice Diamond 1.1 or ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LCMXO3L-4300C-6BG256C with Lattice Diamond 3.1 using Synplify Pro® and LSE (Lattice Synthesis Engine). When using this design in a different device, density, speed, or grade, performance and utilization may vary.

Table 10 lists the implementation results when the design is configured as an I^2S receive master with the parameter ADDR_WIDTH set to 6 and DATA _WIDTH set to 16. The implementation results may vary depending on the parameter values.

Table 10. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
MachXO3L[3]	Verilog-LSE	-6	202	>50	55	N/A
	Verilog-Syn	-6	229	>50	55	N/A
	VHDL-LSE	-6	194	>50	55	N/A
	VHDL-Syn	-6	208	>50	55	N/A
MachXO2[1]	Verilog	-4	298	>50	55	N/A
	VHDL	-4	272	>50	55	N/A
MachXO[2]	Verilog	-3	305	>50	55	N/A
	VHDL	-3	280	>50	55	N/A

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-4TG100CES, with Lattice Diamond 1.1 or ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO1200C-3T100C, with Lattice Diamond 1.1 or ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LCMXO3L-4300C-6BG256C with Lattice Diamond 3.1 design software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

References

- I^{2}S Bus Specification, Philips Semiconductor
- WISHBONE System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores, Revision B.3
- I^{2}S Interface Specification Revision 1.0, OpenCores, Author: Geir Drange

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2010	01.0	Initial release.
March 2014	01.1	Updated Table 9, Performance and Utilization (design is configured as an I^{2}S transmit master) and Table 10, Performance and Utilization (design is configured as an I^{2}S receive master). - Added support for MachXO3L device family. - Added support for Lattice Diamond 3.1 design software.
		Updated corporate logo.
		Updated Technical Support Assistance information.