SMBus Controller

Reference Design

FPGA-RD-02100-1.1

December 2019

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1. Introduction

The System Management Bus (SMBus) is a two-wire interface through which simple system and power management devices can communicate with the rest of the system. The protocol is compatible with the I^2C bus protocol and is often found in monitoring power conditions, temperature, and other sensors on a board. This reference design provides a bridge between the SMBus master and the WISHBONE bus. A typical application of this design includes the interface between a WISHBONE-compliant, on-board microcontroller and multiple SMBus peripheral components.

While SMBus is derived from I^2C, there are several major differences existing between the specifications of the two buses. The most significant differences between the two are the timeout and the minimum clock speed requirements. SMBus defines a clock-low timeout limit of 25 ms for master, 35 ms for slave, and a minimum clock speed of 10 KHz. I^2C does not have such a requirement and the master or the slave can hold the bus low indefinitely. In addition, SMBus specifies a data hold time of 300 ns while the I2C hold time is 0. In terms of performance, SMBus operates up to 100 KHz, while I^2C's fast-mode supports up to 400 KHz. Other minor differences include voltage level and rise/fall time. The details can be found in the SMBus Specification and I^2C Specification.

This design is based on Lattice reference design I^2C Master with WISHBONE Interface (FPGA-RD-02072). It is available in both Verilog and VHDL languages.

2. Features

- Compatible with SMBus Specification
  - Multi-master operation
  - Software-programmable SDL clock frequency from 10 KHz to 100 KHz
  - Clock stretching and wait state generation
  - Timeout monitor for the master
  - Interrupt flag generation
  - Arbitration lost interrupt, with automatic transfer cancellation
  - Bus busy detection
  - Supports 7-bit addressing modes
- Compliant with WISHBONE specification
  - Revision B.3 compliant WISHBONE Classic interface
  - All output signals are registered
  - Two-cycle access time
  - A non-WISHBONE compatible signal, arst_i, is an asynchronous reset signal provided for FPGA implementations

3. Functional Description

The SMBus master core supports the critical features described in the SMBus Specification and is suitable for most applications involving SMBus slave control. Two optional wires, SMBSUS# and SMBALERT#, as described in the SMBus Specification, are not included in this design. They can be easily added into the design by the user. The design responds to the read/write cycles initiated by the microcontroller through the WISHBONE interface. It provides the correct sequences of commands and data to the SMBus slave device and then transfers the required data from the SMBus slave device through the two open-drain wires. The SMBus master with WISHBONE interface administrates many details of the SMBus commands and operation sequences, freeing the microcontroller from these tasks.

Table 3.1. lists the I/O ports of the design. The signals ending in "_i" indicate an input and those ending in "_o" indicate an output. All signals on the WISHBONE side are synchronous to the master clock. The two SMBus wires, SCL and SDA, must be open-drain signals and are externally pulled up to Vcc through resistors.

Table 3.1. Pin Descriptions

Signal	Width	Type	Description
WISHBONE Interface			
wb_clk_i	1	Input	Master clock
wb_rst_i	1	Input	Synchronous reset, active high
arst_i	1	Input	Asynchronous reset
wb_adr_i	3	Input	Lower address bits
wb_dat_i	8	Input	Data towards the core
wb_dat_o	8	Output	Data from the core
wb_we_i	1	Input	Write enable input
wb_stb_i	1	Input	Strobe signal/core select input
wb_cyc_i	1	Input	Valid bus cycle input
wb_ack_o	1	Output	Bus cycle acknowledge output
wb_inta_o	1	Output	Interrupt signal output
SMBus Interface			
scl	1	Bi-directional	Serial clock line
sda	1	Bi-directional	Serial data line

4. Design Module Description

The design has four main modules as shown in Figure 4.1. These include one top-level module and three lower-level modules which include the register module, byte command module and bit command module.

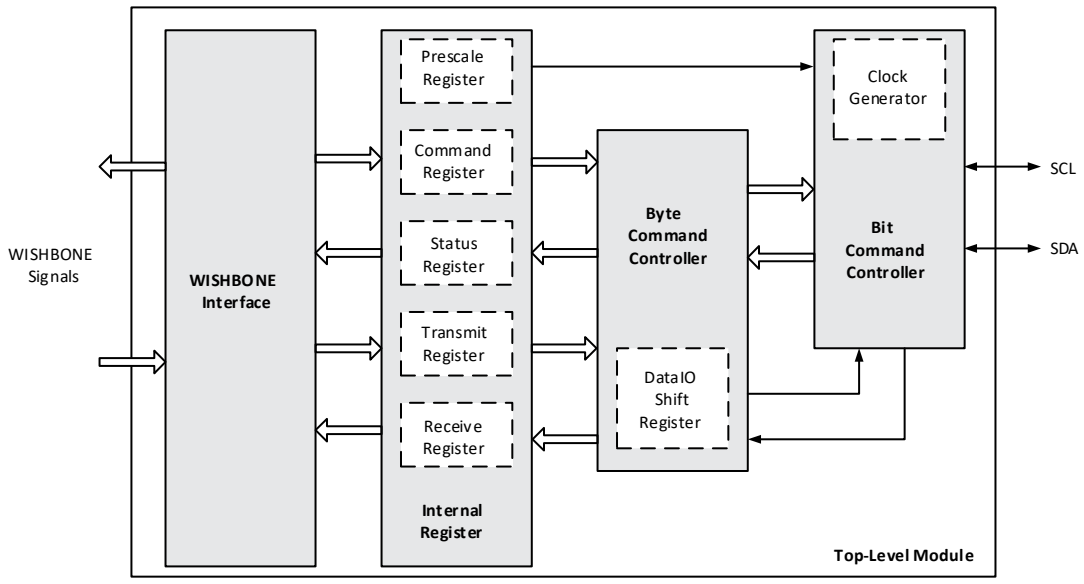

Figure 4.1. Design Modules

4.1. Top-level Module (SMBus_master_top.v)

In addition to connecting all the functional blocks, this module generates generates byte-wide data, plus acknowledgement and interrupt signals for the WISHBONE interface. Depending on the parameter ARST_LVL, the reset polarity is determined and distributed to all the modules.

4.2. Internal Registers Module (SMBus_master_registers.v)

A 2-bit by 8-bit register space constitutes the internal register structure of the SMBus core. The space houses the six 8-bit registers listed in Table 4.1. The addresses not used are reserved for future expansion of the core.

Table 4.1. Internal Register List

Name	Address	Width	Access	Description
PRERlo	0x00	8	RW	Clock prescale register lo-byte
PRERhi	0x01	8	RW	Clock prescale register hi-byte
CTR	0x02	8	RW	Control register
TXR	0x03	8	W	Transmit register
RXR	0x03	8	R	Receive register
CR	0x04	8	W	Command register
SR	0x04	8	R	Status register

The prescale register (address = 0x00 and 0x01) is used to prescale the SCL clock line based on the master clock. This design uses an internal clock, clk_en, to generate the SCL clock frequency. The frequency of clk_en is calculated by the equation [wb_clk_i Frequency / Prescale Register + 1] and this frequency is 5 times SCL frequency. The contents of the prescale register can only be modified when the core is not enabled.

Only two bits of the control register (address = 0x01) are used for this design. The MSB of this register is the most critical one because it enables or disables the entire SMBus core. The core will not respond to any command unless this bit is set.

The transmit register and the receive register share the same address (address = 0x30) depending on the direction of data transfer. The data to be transmitted via SMBus will be stored in the transmit register, while the byte received via SMBus is available in the receive register.

The status register and the command register share the same address (address = 0x04). The status register allows the monitoring of the SMBus operations, while the command register stores the next command for the next SMBus operation. Unlike the rest of the registers, the bits in the command register are cleared automatically after each operation. Therefore, this register must be written for each start, write, read, or stop of the SMBus operation. Table 4.2. provides a detailed description of each bit in the internal registers.

Table 4.2. Description of Internal Register Bits

Internal Register	Bit #	Access	Description
Control Register (0x02)	7	RW	EN – SMBus core enable bit. 1 = Core is enabled 0 = Core is disabled
	6	RW	IEN – SMBus core interrupt enable bit. 1 = Interrupt is enabled 0 = Interrupt is disabled
	5:0	RW	Reserved
Transmit Register (0x30)	7:1	W	Next byte to be transmitted via SMBus
	0	W	a) This bit represents the data's LSB. b) This bit represents the RW bit during slave address transfer 1 = Reading from slave 0 = Writing to slave

Table 4.3. Description of Internal Register Bits (Continued)

Internal Register	Bit #	Access	Description
Receive Register (0x30)	7:0	R	Last byte received via the SMBus
Status Register (0x04)	7	R	RxACK – Received acknowledge from slave. This flag represents acknowledge from the addressed slave. 1 = No acknowledge received, 0 = Acknowledge received
	6	R	Busy – Indicates that the SMBus bus is busy 1 = START signal is detected 0 = STOP signal is detected
	5	R	AL – Arbitration lost. This bit is set when the core loses arbitration. Arbitration is lost when: A STOP signal is detected, but not requested The master drives SDA high, but SDA is low
	4	R	Reserved
	3	R	Timeout 1 = SCL and SDA line have been high for 50ms
	2	R	Timeout 1 = SCL line has been low for 25ms
	1	R	TIP – Transfer in Progress. 1 = Transferring data 0 = Transfer is complete
	0	R	IF – Interrupt Flag. This bit is set when an interrupt is pending, which will cause a processor interrupt request if the IEN bit is set. The Interrupt Flag is set when: One byte transfer has been completed Arbitration is lost
Command Register (0x04)	7	W	STA – Generate (repeated) start condition
	6	W	STO – Generate stop condition
	5	W	RD – Read from slave
	4	W	WR – Write to slave
	3	W	ACK, when a receiver, sent ACK (ACK = 0) or NACK (ACK = 1)
	2	W	When set, clears the timeout status
	1	W	Reserved
	0	W	IACK – Interrupt acknowledge. When set, clears a pending interrupt.

4.3. Byte Command Controller Module (SMBus_master_byte_ctrl.v)

The microcontroller issues commands and data through the WISHBONE interface in byte format. The information is fed into the Byte Command Controller module and is translated into SMBus sequences required for a byte transfer. This module includes a state machine, as shown in Figure 4.2., to handle normal SMBus transfer sequences. The module then breaks up a single command into multiple clock cycles for the Bit Command Controller to work on bitlevel SMBus operations. This module also contains a shift register which is used for both READ and WRITE cycles. During a READ cycle, the input to the shift register comes from the SDA line. After eight SCL cycles, the shifted-in data is copied into the Receive Register. During a WRITE cycle, the input to the shift register comes from the WISHBONE data bus. The data in the shift register is shifted out to the SDA line during a WRITE.

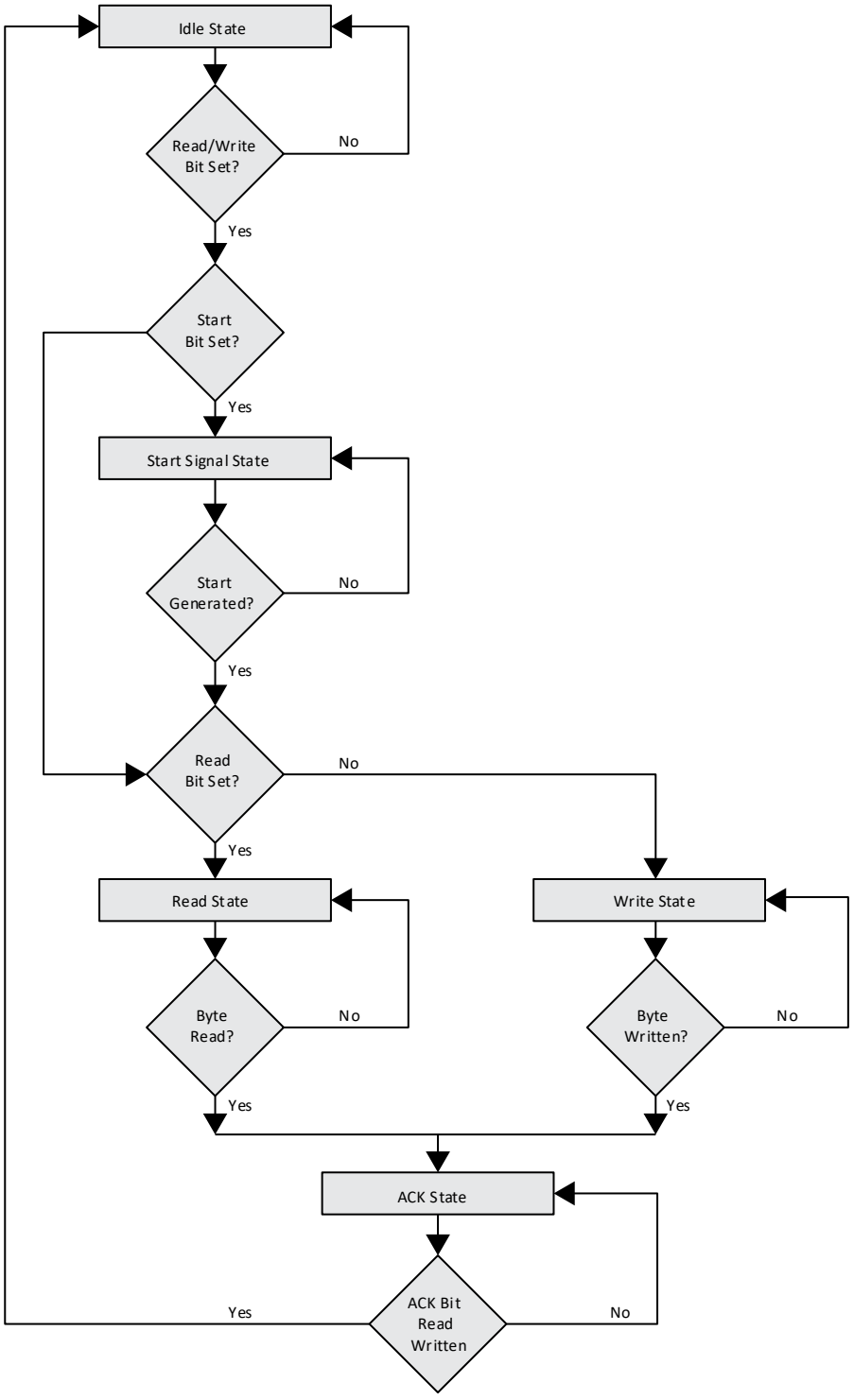

Figure 4.2. SMBus Byte Command State Machine Flow Diagram

4.4. Bit Command Controller Module (SMBus_master_bit_ctrl.v)

This module controls the SMBus, SCL and SDA lines, by generating the correct sequences for START, STOP, Repeated START, READ, and WRITE commands. Each bit operation is divided into five (5x SCL frequency) clock (clk_en) cycles (idle, A, B, C, and D), except for the START command that has six clock cycles. This ensures that the logical relationship between the SCL and SDA lines meets the SMBus requirement for these critical commands. The internal clock (clk_en) running at 5 x SCL frequency is used for the registers in this module (Figure 4.3., Table 4.4.). The designer can calculate the appropriate frequency of the internal clock clk_en to meet the SMBus timing specification by setting an appropriate value to the prescale register.

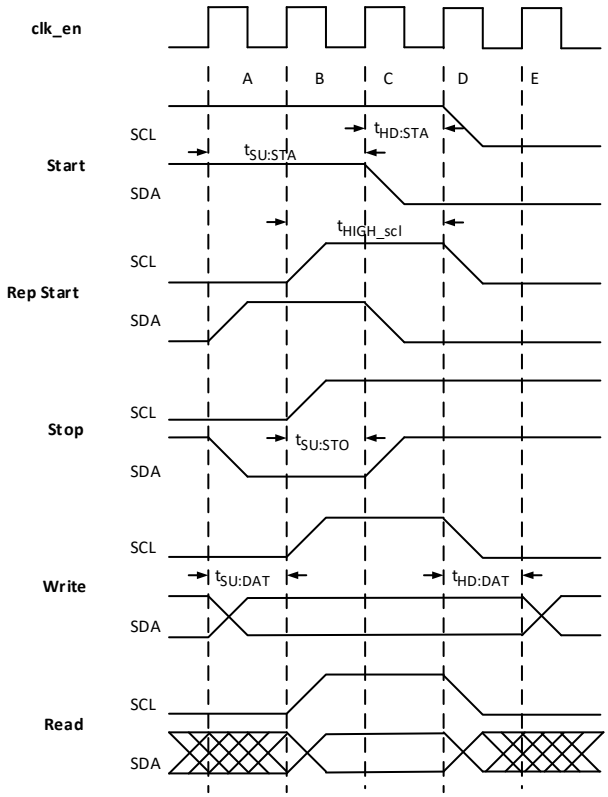

Figure 4.3. SMBus Bit Command Waveform

Table 4.4. SMBus Timing Specification

Symbol	Parameter	Value
$t_{HD:STA}$	Hold time after START condition	1 clk_en cycle
$t_{SU:STA}$	Start condition setup time	1 clk_en cycle
$t_{SU:DAT}$	Data setup time	1 clk_en cycle
$t_{HD:DAT}$	Data hold time	1 clk_en cycle
t_{HIGH_scl}	SCL high period	2 clk_en cycles
$t_{LOW:scl}$	SCL low period	3 clk_en cycles
$t_{SU:STO}$	Stop condition setup time	1 clk_en cycle

4.5. Miscellaneous Features

By nature of the open-drain signal, the SMBus provides clock synchronization through a wired-AND connection on the SCL line. This clock synchronization capability can be used as a handshake between the slave and master SMBus devices. By holding the SCL line low, the slave device tells the master to slow down the data transfer until the slave device is ready. This design detects the SCL line to determine if the line is being held.

This design supports multiple masters and thus incorporates the arbitration lost detection. The master that loses the arbitration reports the status in Status Register bit 5. The arbitration is lost when the master detects a STOP condition which is not requested, or when the master drives the SDA line high but the SDA line is pulled low. The arbitration lost resets the bits in the Command Register to clear the current command for the master to start over again.

This design monitors the SCL and SDA bus values to determine if either of two timing conditions have been violated:

- **The SMBus specification requires that when SCL has been low for 25 ms, the SMBus master must generate a stop condition within or after the current data byte in the transaction**. This design generates a stop condition after the current data byte in the transaction when the master detects this condition and reports the status in Status Register bit 2. An appropriate value can be set for the parameter SCL_LOW_TIMEOUT in the source code to meet the 25 ms requirement according to the clock wb_clk_i frequency.
- **The SMBus specification also requires that when SCL and SDA have been high for 50 ms, the SMBus is considered free.** This design reports the status in Status Register bit 3 when such a condition is detected. An appropriate value can be set in the parameter SCL_SDA_HIGH_TIMEOUT in the source code to meet the 50 ms requirement according to the clock wb_clk_i frequency.

These features are described in detail in the SMBus Specification.

4.6. SMBus Controller Operation Sequence

To write data to the SMBus slave:

1. Write the appropriate data to the **prescale register** based on the frequency of SCL through the WISHBONE bus.
2. Write 0x01 to the **control register** to enable the SMBus Controller through the WISHBONE bus.
3. Write the SMBus slave address and write bit to the **transmit register** through the WISHBONE bus.
4. Write 0x90 to the **control register** through the WISHBONE bus to start the SMBus write operation.
5. Read the status register through the WISHBONE bus until bit 1 of the **status register** is set.
6. Write the byte which is sent to the SMBus slave to the **transmit register** through the WISHBONE bus.
7. Write 0x10 to the **control register** through the WISHBONE bus to set SMBus write operation.
8. Read the **status register** through the WISHBONE bus until bit 1 of the status register is set.
9. When all the bytes have been sent, write 0x40 to the **control register** through the WISHBONE bus to stop the SMBus write operation.
10. Read the **status register** through the WISHBONE bus until bit 1 of the status register is set.

To read data from the SMBus slave:

1. Write the appropriate data to the **prescale register** based on the frequency of SCL through the WISHBONE bus.
2. Write 0x01 to the **control register** to enable the SMBus Controller through the WISHBONE bus.
3. Write the SMBus slave address and the read bit to the **transmit register** through the WISHBONE bus.
4. Write 0x90 to the **control register** through the WISHBONE bus to start the SMBus read operation.
5. Read the **status register** through the WISHBONE bus until bit 1 of the status register is set.
6. Write 0x20 to the **control register** through the WISHBONE bus to read data from the slave.
7. Read the **status register** through the WISHBONE bus until bit 1 of the status register is set.
8. Read data from the **receive register** through the WISHBONE bus.
9. When the read operation is finished, write 0x40 to the control register through the WISHBONE bus to stop the SMBus read operation.
10. Read the status register through the WISHBONE bus until bit 1 of the status register is set.

5. HDL Simulation and Verification

The SMBus master with WISHBONE interface design is simulated using an SMBus slave model (SMBus_slave_model.v) and a WISHBONE master model (wb_master_model.v). The slave model emulates the responses of an SMBus slave device by sending an ACK signal when the address is matching and when the WRITE operation is completed. The master model contains several tasks to emulate the WISHBONE READ, WRITE, and COMPARE commands normally issued by the microcontroller. The top-level test bench (tst_bench_top.v) controls the flow of the SMBus operation. The START, WRITE, REPEATED START, READ, consecutive READ, ACK/NACK, STOP, and clock stretching operations are simulated with this test bench.

The following timing diagrams shows the major timing milestones in the simulation.

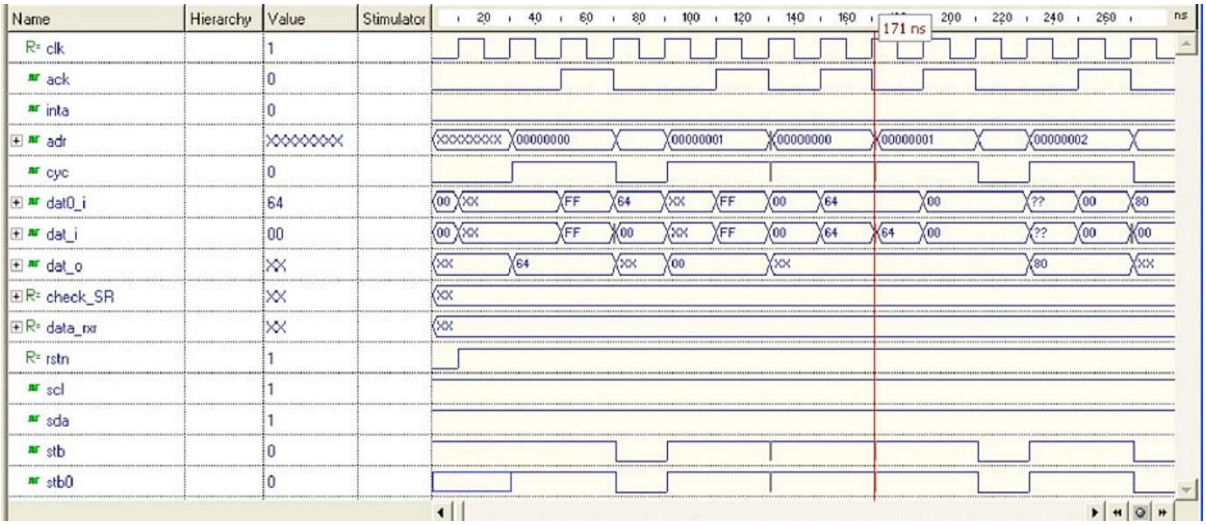

Figure 5.1. Writing Prescale Register with 0x64 and 0x00 at Addresses 0x00 and 0x01 Respectively

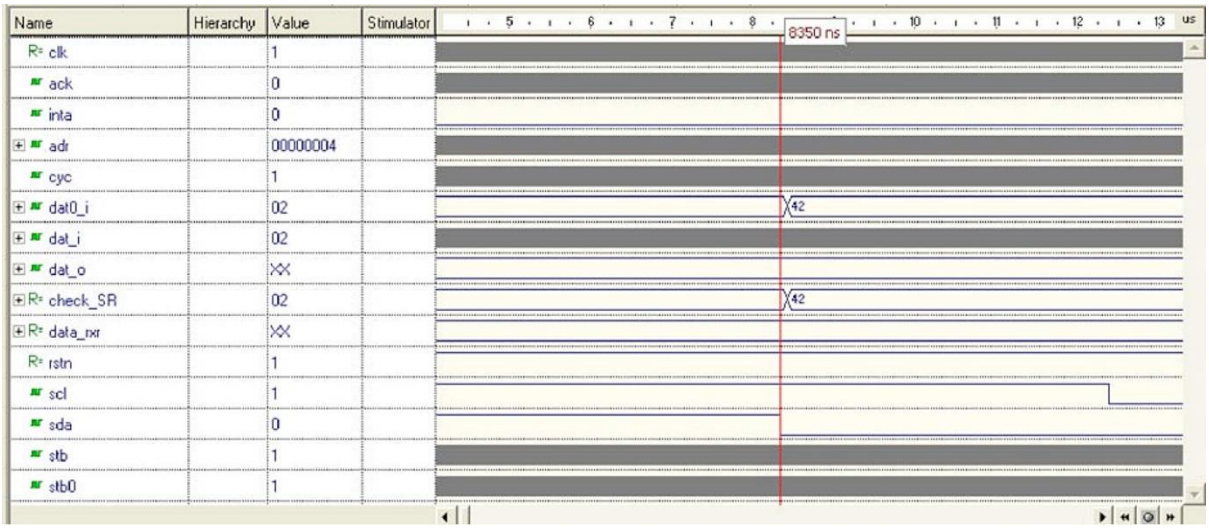

Figure 5.2. Initiate a START, SR[1] (Transfer in Progress) and SR[6] (Busy) Are Set

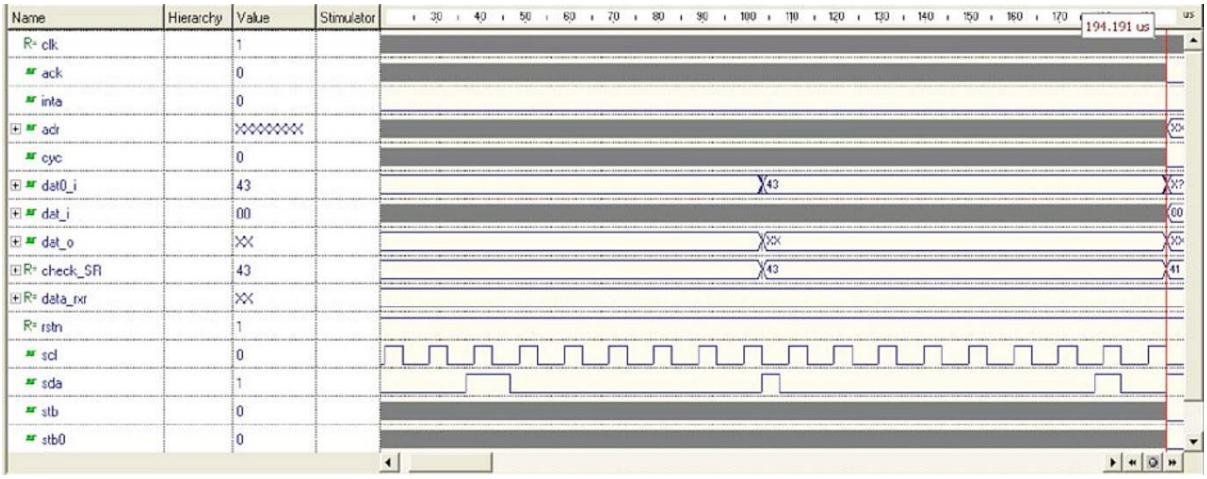

Figure 5.3. Transfer Slave Address + WR, Receive ACK from Slave, Transfer Slave Memory Address 0x01, Receive ACK from Slave, Release SR[1] (Transfer in Progress)

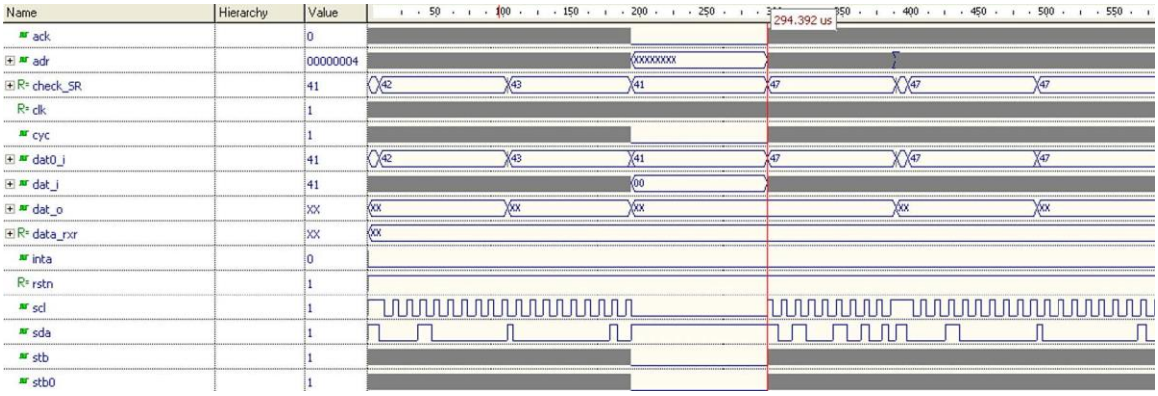

Figure 5.4. Clock Stretching by Slave, SCL Line Held Low for 25 ms, Master Generate the Stop Condition

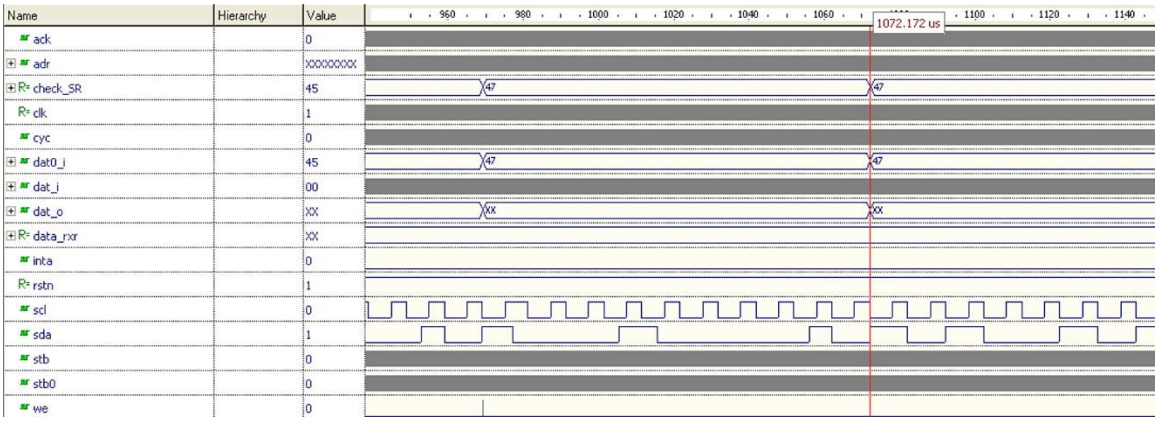

Figure 5.5. Repeated START with Slave Address + RD Command

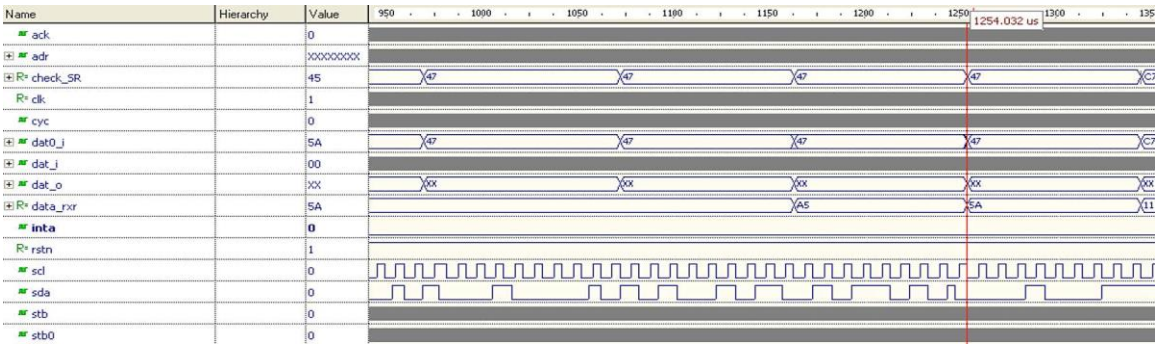

Figure 5.6. Consecutive READ from the Slave, Data Read are 0xA5, 0x5A, and 0x11

6. Implementation

Table 6.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
MachXO™ [1]	Verilog	-3	294	>50	29	N/A
	VHDL	-3	285	>50	29	N/A
MachXO2™ [2]	Verilog	-4	299	>50	29	N/A
	VHDL	-4	290	>50	29	N/A

Notes:

1. Performance and utilization characteristics are generated using LCMXO1200C-3T100C, with Lattice ispLEVER® 8.1 SP1 and Lattice Diamond™ 1.1 design software When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO2-2000HC-4TG100CES, with Lattice ispLEVER 8.1 SP1 and Lattice Diamond 1.1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

References

- SMBus Specification, Version 2.0
- I^2C Master with WISHBONE Interface (FPGA-RD-02072)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, December 2019

Section	Change Summary
All	• Changed document number from RD1098 to FPGA-RD-02100. • Updated document template.
Disclaimers	Added this section.

Revision 1.0, November 2010

Section	Change Summary
All	Initial release.

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