LatticeECP3 AMC Evaluation Board – Revision B

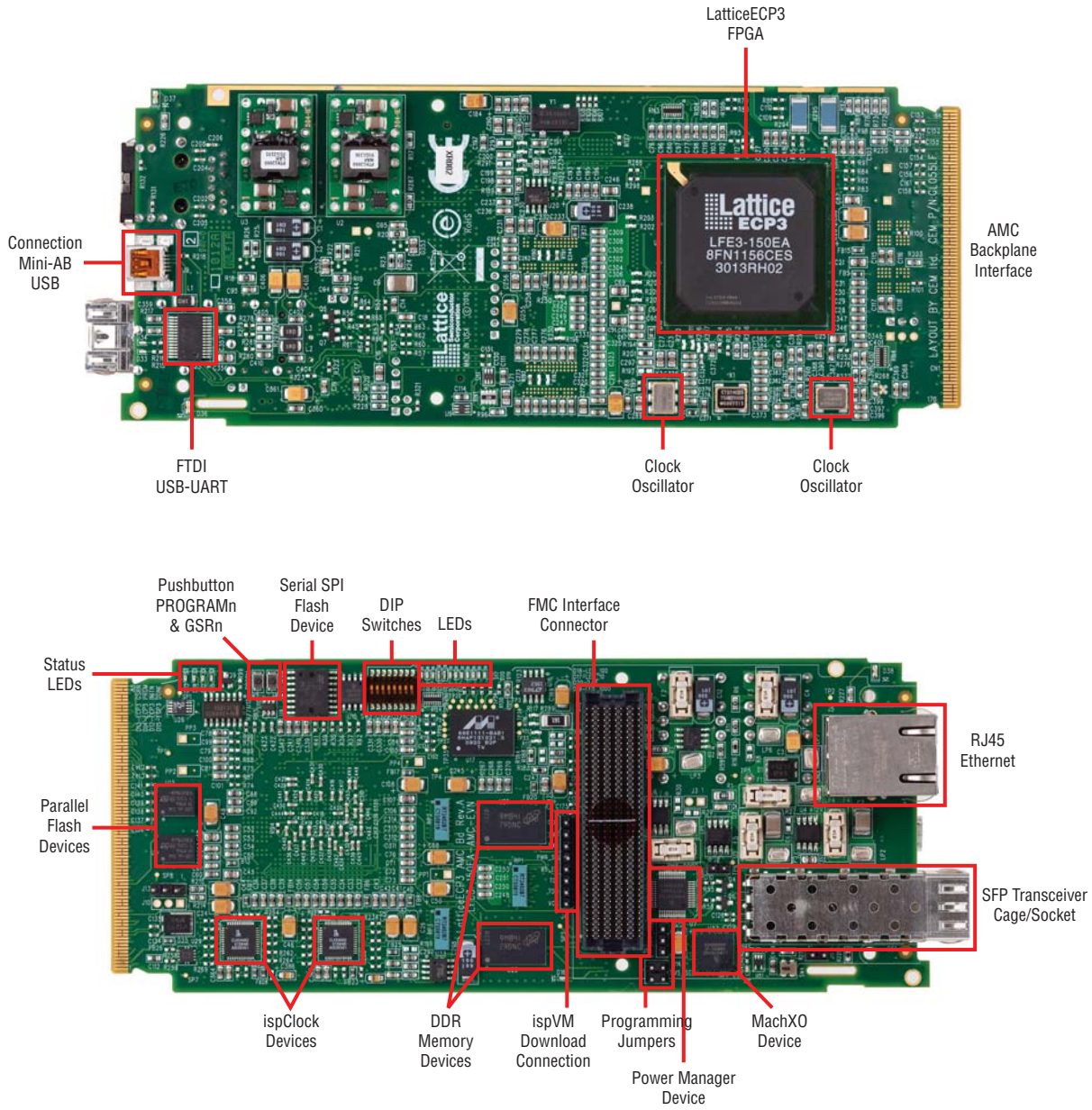
User's Guide

August 2012
Revision: EB56_01.1

Introduction

The LatticeECP3™ AMC Evaluation Board allows designers to investigate and experiment with the features of the LatticeECP3 high-speed SERDES transceivers in an AMC system environment. The features of the LatticeECP3 AMC Evaluation Board assist engineers with rapid prototyping and testing of their designs. The board follows portions of the PICMG AMC R2.0 AMC form-factor specification that allows users the capability to use the board in live system evaluations. This user's guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP3 FPGA.

Figure 1. LatticeECP3 AMC Evaluation Board Details



Features

- Single module AMC PCB card edge interface
  - Allows demonstration of AMC Fat Pipes
  - Common options interface
- Allows control of SERDES PCS registers using the Serial Client Interface (ORCAstra)
- DMC (FPGA Mezzanine Card) expansion connector
- USB-B connection to UART for run-time control
- RJ45 interface to 10/100/1000 Ethernet to SGMII
- SFP transceiver module cage and connection
- On-board Boot Flash
  - 64M Serial SPI Flash
- DDR2 memory components (256MB x 32 bits)
- 32-bit parallel, non-volatile memory that can be read, erased and reprogrammed
- Switches, LEDs and displays for demonstration purposes
- ispVM™ System software programming support
- On-board reference clock sources

The board can be used as provided with a front-panel SFP cage that accepts industry standard transceiver modules. It also includes a RJ45 network jack for Ethernet communication. However, by removing the SFP and RJ45 the board can be used with a standard VITA 57.1 FPGA Mezzanine Card. This permits user-specific FMCs to be used with the LatticeECP3 AMC Evaluation Board.

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics (Appendix D) and bill of materials (Appendix B).

LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V core supply. It can accommodate all pin-compatible LatticeECP3 devices in the 1156-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP3 Family Data Sheet.

Note: The connections referenced in this document refer to the LFE3-95EA-FF1156 device. However, the LFE150EA-FF1156 has been used but provides full device migration pinouts. This device permits additional transceiver connections to the board. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeECP3 AMC Evaluation Board is ready to power on. The board can be supplied with power from the uTCA backplane or chassis. For evaluations outside a telecom equipment environment Lattice provides the Lattice AMC Interface Card that provides power. See Appendix A for further information on the Lattice AMC Interface Card.

All input power sources and on-board power supplies are fused with the surface mounted fuses noted below.

Table 1. Board Power Supply Fuses (see Appendix D, Figure 27)

Fuse Designator	Description
F1	12V Input Supply Fuse
F2	3.3V Fuse
F3	1.2V Core Fuse
F4	1.8VFuse
F5	1.2V Analog Supply
F6	2.5V Fuse

The above-mentioned supplies can be isolated from the on-board regulators by removal of the associated fuse. Surface-mounted test-loops are provided to apply alternative power sources to these supplies as required for testing purposes.

Table 2. Power Supply Test Connections

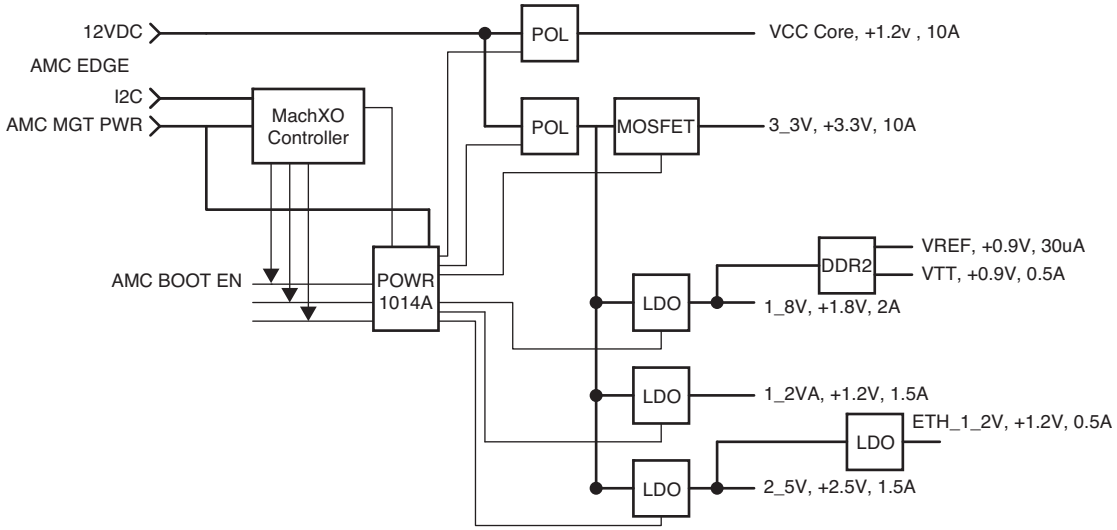
Test Point Designator	Supply
LP1	2.5V
LP2	1.8V
LP3	3.3V
LP4	12V
LP5	1.2V VCCA
LP6	1.2V VCC Core
LP7	Ground

Power Management

The board includes an ispPAC®-POWR1014A programmable power management IC (U7). This device controls the power sequence and monitors designated board supplies. The POWER GOOD indicator LED D10 is controlled via this device. This LED indicates all supplies are on and at proper operating levels.

The power management device is factory-programmed to control and monitor the power supplies. The block diagram of the power management is shown in Figure 2.

Figure 2. Power Management Scheme (see Appendix D, Figure 28)

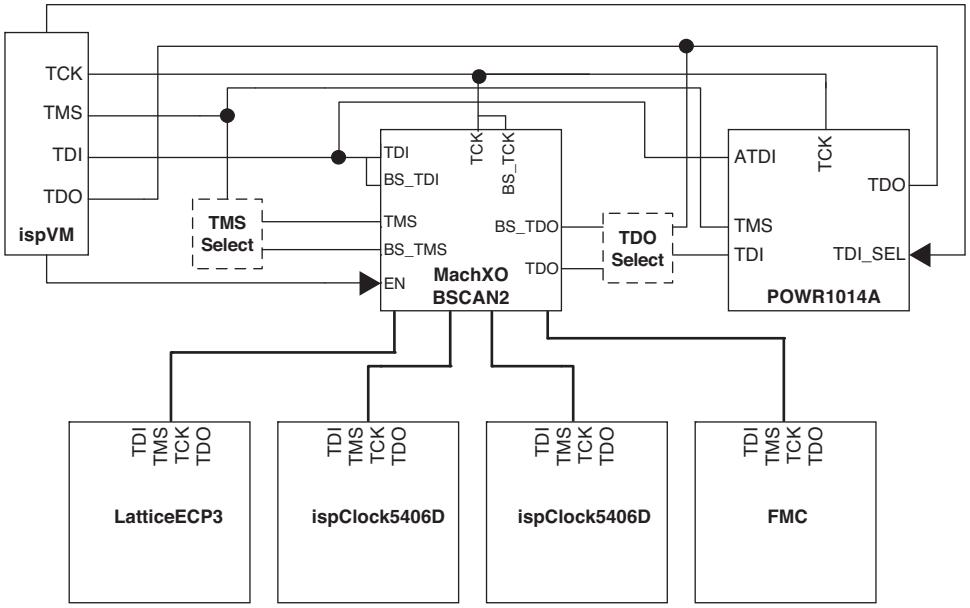


Programming/FPGA Configuration

A programming header is provided on the evaluation board that provides access to all on-board Lattice devices including the LatticeECP3 JTAG port. The on-board JTAG scheme utilizes a MachXO™ CPLD to serve as a controller for the JTAG when programmed with the BSCAN2 logic. The BSCAN2 controller is factory-programmed within the MachXO640C device.

The JTAG chain includes the POWR1014A power manager device that is available in the JTAG chain and through the alternative chain that is controlled via the ispVM cable selection. The user can alter any design within the FPGA or either of the two ispClock™5406D devices. However, users should not alter the MachXO640C or POWR1014A devices without consulting Lattice.

Figure 3. AMC JTAG Chain (see Appendix D, Figure 30)



ispVM Requirements

Note: An ispDOWNLOAD™ Cable is included with each ispLEVER®-Base or ispLEVER-Advanced design tool shipment. Cables may also be purchased separately from Lattice.

After initial board setup, use the following procedure to program the evaluation board. Instructions assume ispVM software has been installed on a local PC.

Requirements:

- PC with ispVM System v.19.0 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

ispVM Download Interface

J4 is an 8-pin JTAG connector used in conjunction with the ispVM USB download cable to program and control the device.

Figure 4. Standard ispVM Programming Cable Configuration

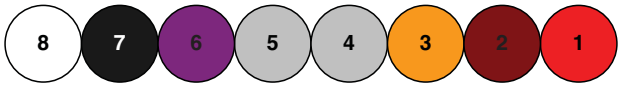
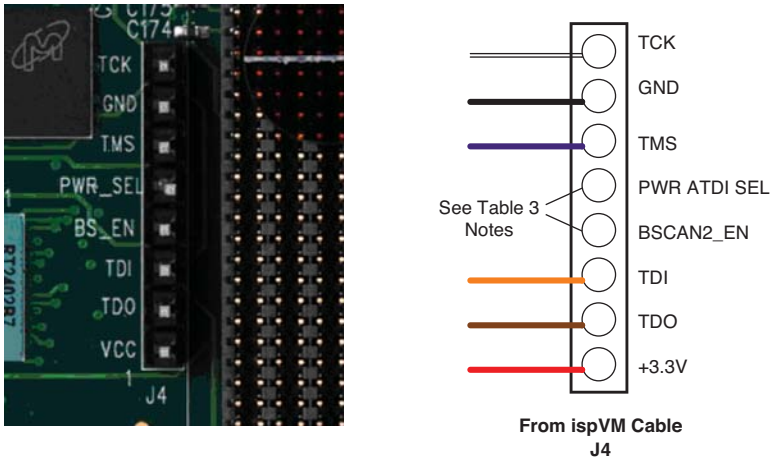


Table 3. ispVM JTAG Connector (see Appendix D, Figure 30)

Pin	Function	Color
1	PWR	Red
2	TDO	Brown
3	TDI	Orange
4	BS_Enable	Note 1
5	PWR_SEL	Note 2
6	TMS	Purple
7	GND	Black
8	TCK	White

1. Only connected to enable BSCAN2 logic within the MachXO640 CPLD. Connect TRST (green lead) to this pin.
2. Only connected for alternate programming of POWR1014A power manager device. Connect ISPEN (yellow lead) to this pin.

Figure 5. ispVM Download Connection (J4)



Board Programming

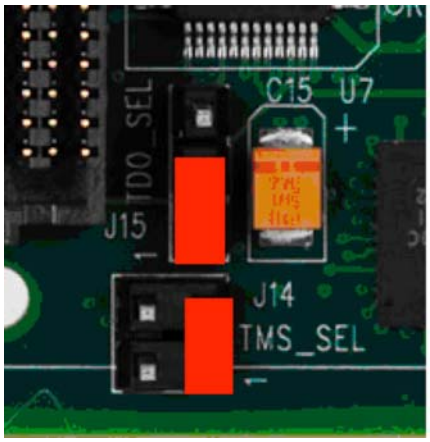
To program or reprogram the Lattice devices on the board, the user must understand the board JTAG topology. As shown in Figure 3, the board allows several different programming variations. These are user-controlled by the ispVM connections (J4) and jumper selections (J14- TMS SEL and J15- TDO SEL).

An alternative chain can be used when it is desired to only communicate with the POWR1014A device. This alternative method utilizes the ispVM to drive the TDISEL input. A logic "1 "driven on the TDISEL of the POWR1014A will enable the ATDI input, ignoring the TDI data of the board JTAG chain and receiving TDI data directly from the ispVM input.

Programming the POWR1014A Device

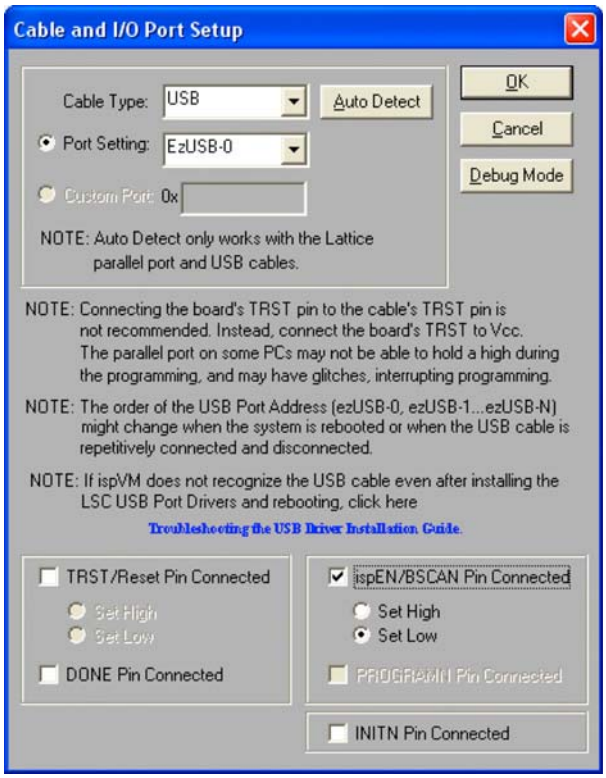
1. Connect the ispVM colored leads to J4 with the yellow lead connected to Pin 5 (PWR_SEL).
2. Add jumpers to J14 and J15 as shown in Figure 6.

Figure 6. Jumpers for Programming the POWR1014A Device (see Appendix D, Figure 39)



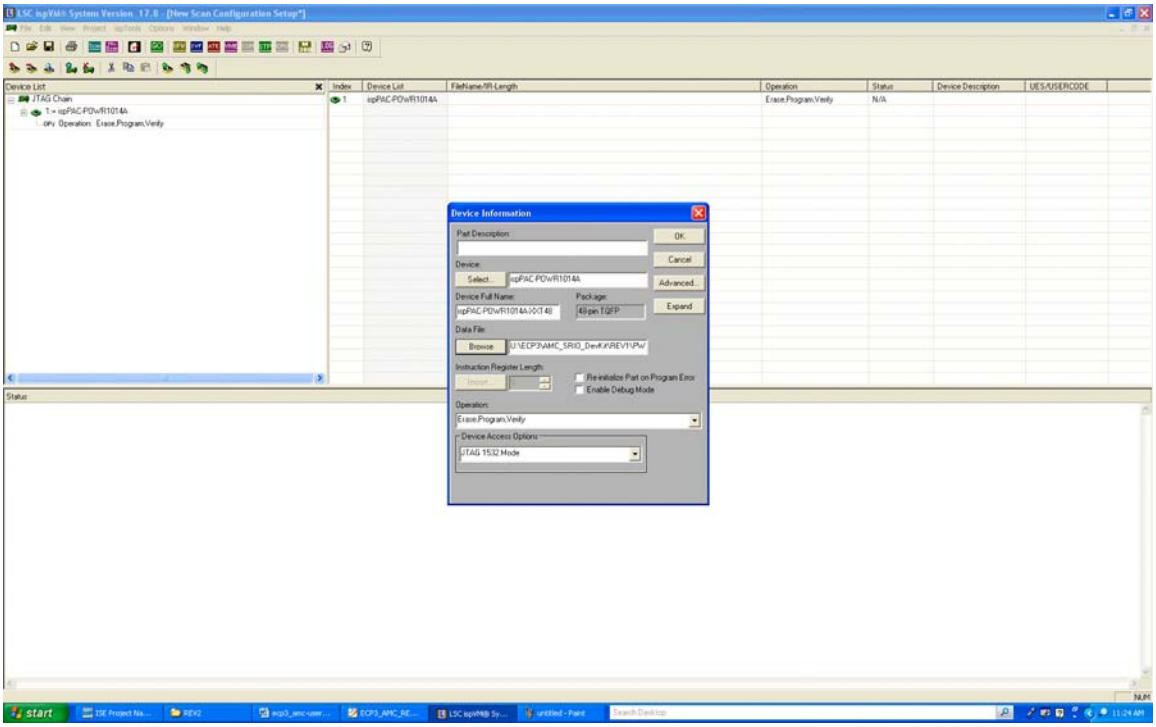
3. Open an ispVM session.
4. Go to **Options > Cable and IO Port Setup > ispEN Connected**, and set **LOW > OK**.

Figure 7. Set ispEN =LOW



5. Click **Scan** on the top toolbar.
6. Browse to the programming file and select **Go** from the top toolbar to program device.

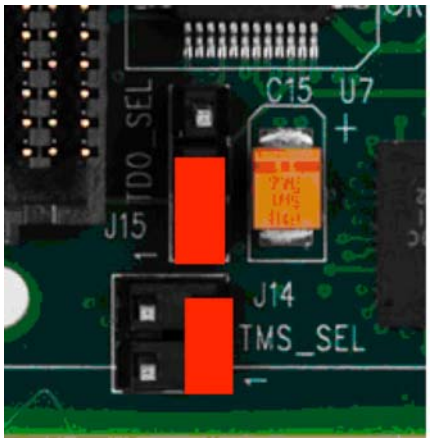
Figure 8. ispVM Session Window for POWR1014A Programming



Programming the MachXO640C Device

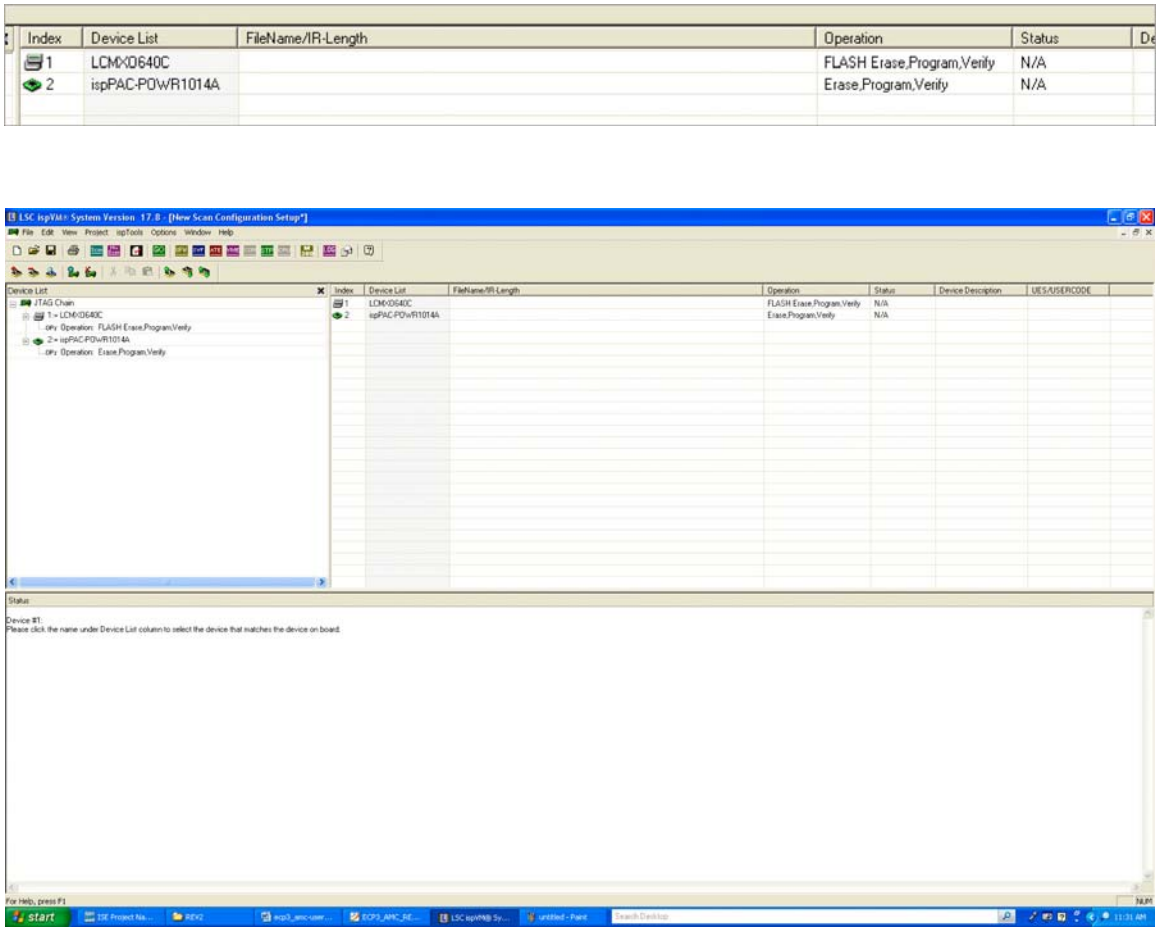
1. Connect the ispVM colored leads to J4 with the yellow and green leads left unconnected.
2. Add jumpers to J14 and J15 as shown in Figure 9.

Figure 9. Jumpers to Program the MachXO640C Device (see Appendix D, Figure 39)



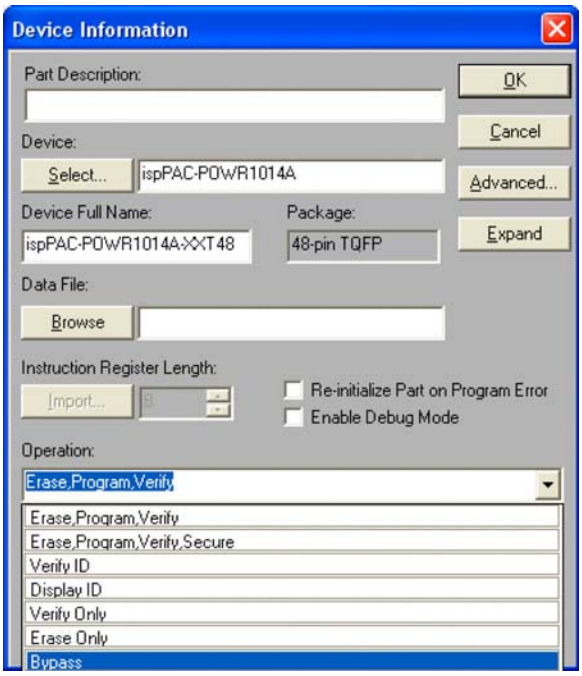
3. Click **Scan** on the top toolbar.

Figure 10. ispVM Session Window for MachXO640C Only Programming

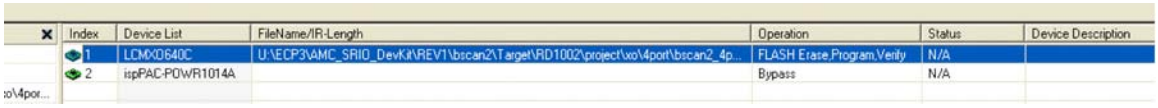


4. Place the POWR1014A in BYPASS.

Figure 11. POWR1014A Device Window



5. Browse to the programming file for the MachXO640 device and select **FLASH Erase, Program, Verify**.



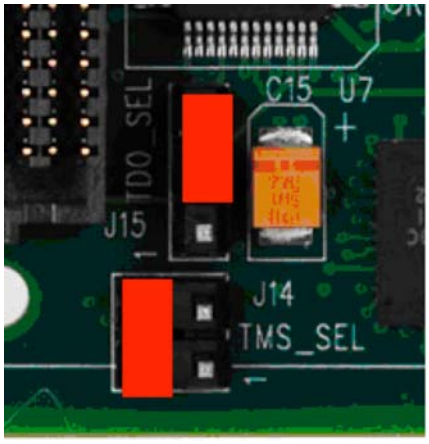
Using ispVM to Access and Program the Chained Devices

In this configuration, the board will utilize the BSCAN2 soft core within the MachXO640C device. Use the ispVM System software to communicate with the targeted devices on the board.

1. Connect the ispVM colored leads to J4 with the green lead connected to Pin 4 (BS_EN).

2. Add jumpers to J14 and J15 as shown in Figure 12.

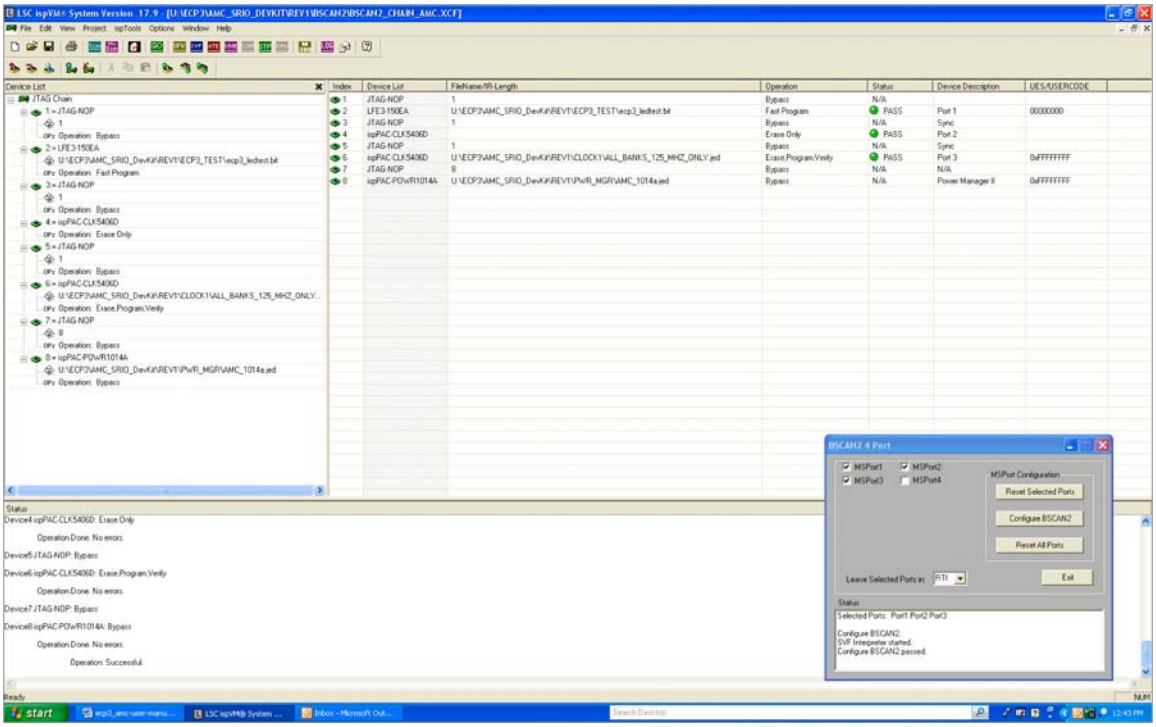
Figure 12. Jumpers for Accessing the Complete JTAG Chain (see Appendix D, Figure 39)



3. Open an ispVM session.

4. In the ispVM session, go to **Open > File > Browse** to locate the Lattice-supplied .xcf file.

Figure 13. ispVM JTAG Chain Session Window



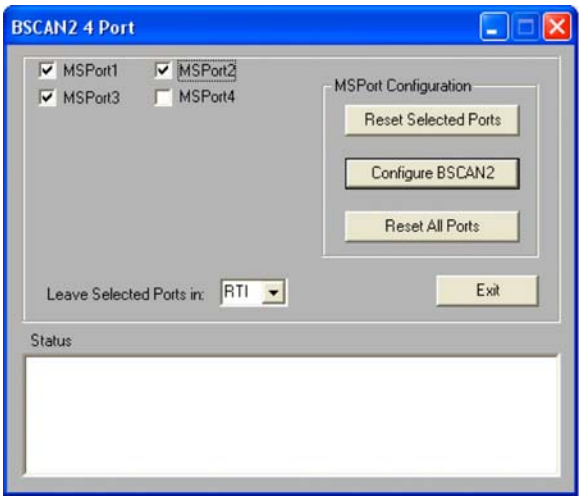
Index	Device List	FileName/IR-Length	Operation	Status	Device Description	UES/USERCODE
1	JTAG-NOP	1	Bypass	N/A		
2	LFE3-150EA	U:\ECP3\AMC_SRIO_DevKit\REV1\ECP3_TEST\ecp3_ledtest.bit	Fast Program	PASS	Port 1	00000000
3	JTAG-NOP	1	Bypass	N/A	Sync	
4	ispPAC-CLK5406D		Erase Only	PASS	Port 2	
5	JTAG-NOP	1	Bypass	N/A	Sync	
6	ispPAC-CLK5406D	U:\ECP3\AMC_SRIO_DevKit\REV1\CLOCK1\ALL_BANKS_125_MHZ_ONLY.jed	Erase,Program,Verify	PASS	Port 3	0xFFFFFFFF
7	JTAG-NOP	8	Bypass	N/A	N/A	
8	ispPAC-POWR1014A	U:\ECP3\AMC_SRIO_DevKit\REV1\PWR_MGR\AMC_1014a.jed	Bypass	N/A	Power Manager II	0xFFFFFFFF

In this session ispVM can control each device target separately by use of the BSCAN2 linker controller held within the MachXO640C device. As shown below, the devices included can be bypassed and/or programmed via this session.

1. To begin this session, navigate to the **Options > Cable and IO Port Setup > TRST Connected**. Set **High > OK**.

2. Next, navigate to **ispTools > BSCAN Config > BSCAN2 4-PORT**. Enable the appropriate targets. **MSPort1 = ECP3 (U1)**, **MSPort2 = CLK5406A (U28)**, **MSPort3 = CLK5406A (U30)**, **MSPort4 = FMC**.

Figure 14. BSCAN2 GUI Control Window

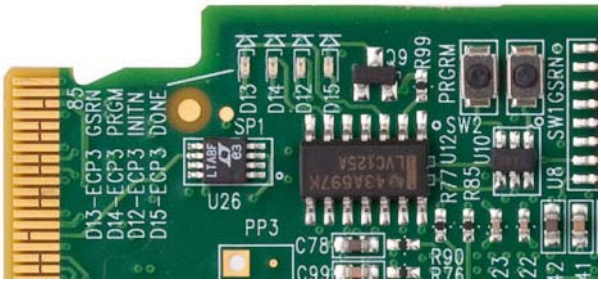


3. From the window above, **Configure BSCAN2** will initialize the JTAG targets.

Configuration Status Indicators

(see Appendix B, Figure 5)

Figure 15. ECP3 Status LEDs and Pushbutton Controls (see Appendix D, Figure 30)



The LEDs indicate the status of the LatticeECP3 FPGA configuration.

- **D12 (red)** – Illumination indicates that the programming was aborted or reinitialized driving the INITN output low.
- **D15 (green)** – Illumination indicates the successful completion of configuration by releasing the open collector DONE output pin.
- **D14 (red)** – Illumination indicates that PROGRAMN is low.
- **D13 (red)** – Illumination indicates that GSRN is low.

PROGRAMN and GSRN

These pushbutton switches assert/de-assert the logic levels on PROGRAMN (SW2) and GSRN (SW1). Depressing the button drives a logic level "0" to the device.

Programming Serial SPI Flash Memory

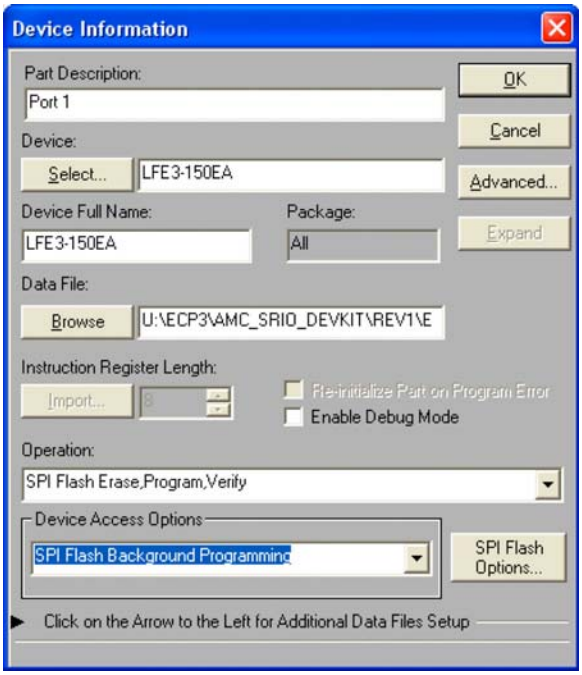
A Serial SPI (16-pin TSSOP 64M) Flash memory device (U8) is on-board for non-volatile configuration memory storage. A STMicro M25P64VMF16 device or equivalent is populated on-board.

The Serial SPI Flash memory device can be configured easily via its JTAG port. This mode enables the FPGA to be programmed at power-up or by assertion of PROGRAMN with a bitstream stored in the memory device.

1. Connect the LatticeECP3 AMC Evaluation Board and follow the beforementioned procedure to complete the BSCAN2 chain.

2. In the dialog box, select **SPI Flash Programming mode** in the **Device Access Options** pull-down menu. This will open the SPI Serial Flash Dialog box.

Figure 16. Device Information Dialog Box



3. In the SPI Serial Flash Device dialog box, select **SPI Flash Erase, Program, Verify** in the **Operation** pull-down menu.

4. Select **SPI Serial Flash** in the **Device Family** pull-down menu, **STMicro** under the **Vendor** pull-down menu, **SPI-M2564** under the **Device** pull-down menu, and **16-lead SOIC** under the **Package** submenu.

Figure 17. Select Device Dialog Box

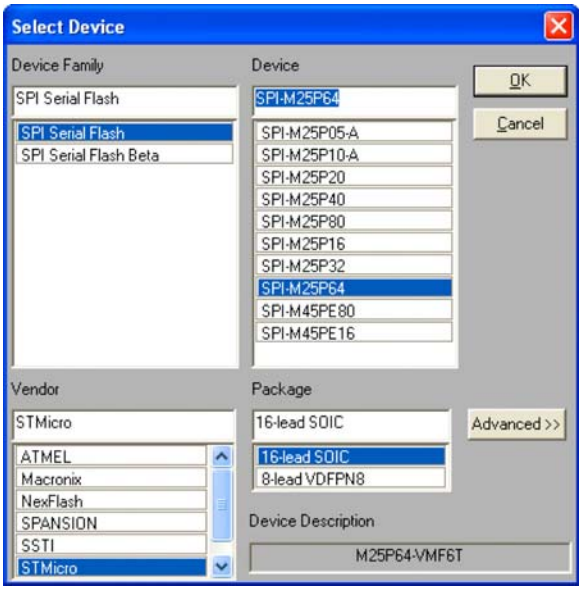
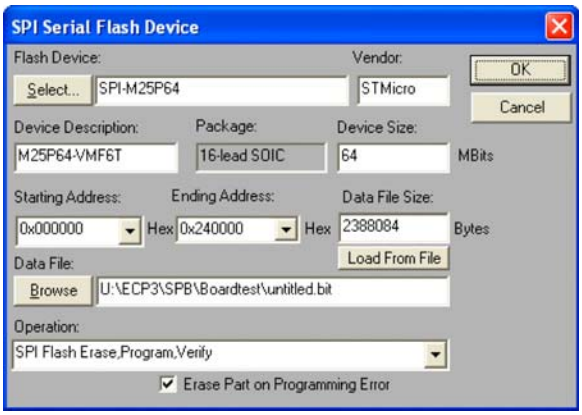


Figure 18. Sample SPI Serial Flash Device Dialog Box



5. Click **OK** in the SPI Flash Device dialog box. Then click **OK** in the Select Device dialog box. The main configuration window will appear.

6. From the main programming window, select **Go** from the top toolbar. SPI Serial Flash programming will begin.

On-Board Parallel SPI Flash Memory

(see Appendix D, Figure 31)

A 32-bit parallel Flash interface to two 16-bit Flash memory devices are included. The LatticeECP3 AMC Evaluation Board incorporates the use of the LatticeMico32™ system builder to access them.

Table 4. Flash Memory Interface

Signal	LatticeECP31156BGA
flash_a2	Y31
flash_a3	Y32
flash_a4	AA29
flash_a5	Y30
flash_a6	Y33
flash_a7	Y34
flash_a8	W26
flash_a9	W27
flash_a10	W29
flash_a11	W30
flash_a12	W28
flash_a13	V29
flash_a14	W31
flash_a15	W32
flash_a16	V26
flash_a17	V27
flash_a18	W33
flash_a19	W34
flash_a20	V28
flash_a21	U28
flash_a22	V30
flash_cem	AN34
flash_oe_n	AN33
flash_we_n	AH33
flash_byte_n	AJ33
flash_wp_n	AP33
flash_rst_n	AP32
flash_rdby_a	AL34
flash_rdby_b	AL33

Signal	LatticeECP3-1156BGA
flash_d0	N30
flash_d1	N29
flash_d2	N26
flash_d3	P26
flash_d4	AF31
flash_d5	AF32
flash_d6	AE29
flash_d7	AE30
flash_d8	AE31
flash_d9	AE32
flash_d10	N32
flash_d11	N31
flash_d12	N27
flash_d13	N28
flash_d14	AA27
flash_d15	AA28
flash_d16	AC33
flash_d17	AC34
flash_d18	AC30
flash_d19	AB30
flash_d20	AA30
flash_d21	AA31
flash_d22	AA26
flash_d23	AA25
flash_d24	AB33
flash_d25	AB34
flash_d26	N34
flash_d27	N33
flash_d28	P28
flash_d29	P27
flash_d30	Y25
flash_d31	Y26

On-Board Clock Capabilities

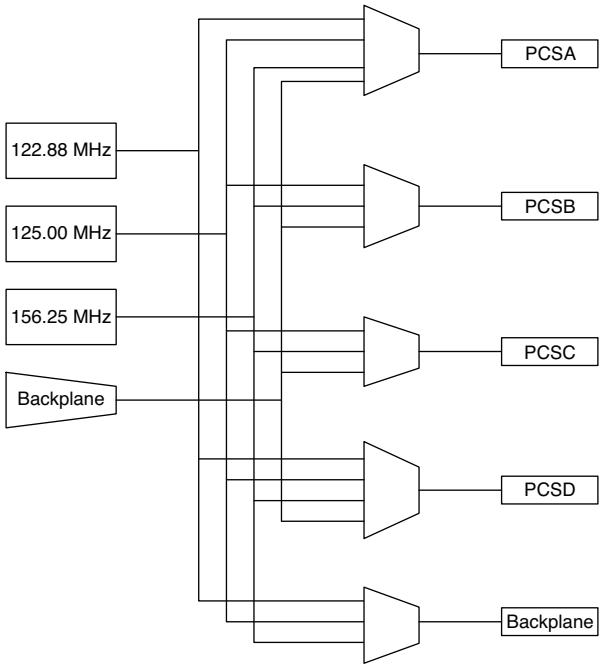
(see Appendix D, Figure 40)

The LatticeECP3 AMC Evaluation Board allows for several clock source options. These options are controlled via the two ispClock5406A programmable clock management devices. There are several on-board oscillator sources that can be synthesized and/or fanned out to several clock input destinations.

As shown in Figure 19, the SERDES/PCS core of the FPGA has several optional connections that can be used with the PCB. All of the clock variations can be managed via programming of the ispClock5406A devices.

- **PCSA** – Clock is sourced from an on-board 122.88, 125, or 156.25 MHz clock. If 122.88 MHz is used, however, this will disallow any non-CPRI interfaces of PCSA. PCSA can also receive a clock from the AMC backplane.
- **PCSB and PCSC** – Clock is sourced from an on-board 125 or 156.25 MHz device. They can also receive clocks from the AMC backplane. The clocking will allow for different rate or same rate clocks to be individually provided to PCSB and PCSC reference clocks.
- **PCSD** – Clock is sourced from an on-board 122.88, 125 or 156.25 MHz device. They can also receive clocks from the AMC backplane.
- **Clock from AMC** – The telcom clock of the AMC edge-finger (TCLKB) will be connected. This clock is capable of driving a reference clock to the PCS reference clocks for all four quads. This clock can be disabled when not in use.
- **Clock to AMC** – The telcom clock of the AMC edge-finger (TCLKB) will be connected. The clock is capable of driving off the AMC module to the backplane and can be the same reference source of any of the PCS quads. This clock can be disabled when not in use.
- **Telcom Clock** – TCLKB is known as CLK2. This clock needs to be bi-directional because it will need to both receive or send a clock on the same pins of the backplane. It is controlled via a single-channel M-LVDS receiver device that determines whether the board is supplying or receiving the clock from the AMC backplane.

Figure 19. Clock Controller Scheme (see Appendix D, Figure 40)



SERDES

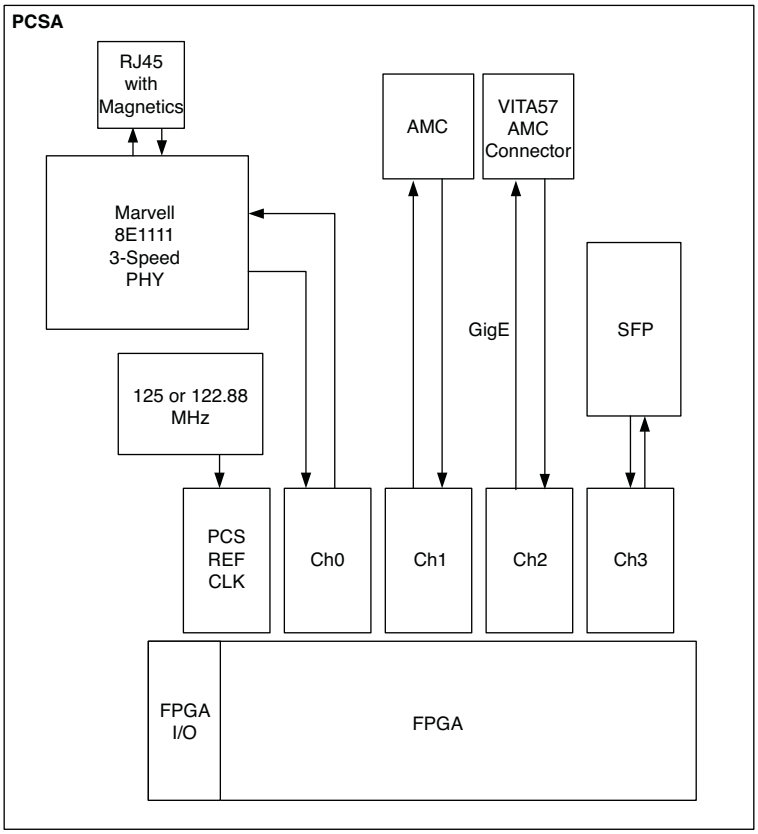
(see Appendix D, Figure 32)

The PCSA quad is used for the following purposes.

PCSA Usage

1. One duplex SERDES channel connected to the 1000BASEX to SFP interface.
2. One duplex SERDES channel connected to the Marvel 88E1111 PHY device SGMII utilizing RJ-45 connections.
3. One duplex Gigabit Ethernet SERDES channel with connectivity to the VITA57 FMC connector.
4. One duplex Gigabit Ethernet SERDES channel with connectivity to the AMC edge.
5. Reference clock will include a 125 MHz or 156.25 MHz source connected to the PCSA dedicated clock inputs. A 122.88 MHz source is available for CPRI-only demos that disallows any non-CPRI usage of PCSA interfaces.

Figure 20. PCSA Channel Provisioning



PCSB Usage

All four duplex channels are interfaced to the AMC backplane on the PCB edge.

PCSC Usage

All four duplex channels are interfaced to the AMC backplane on the PCB edge.

PCSD Usage

All four duplex channels are interfaced to the FMC interface connector for use with a custom FMC module.

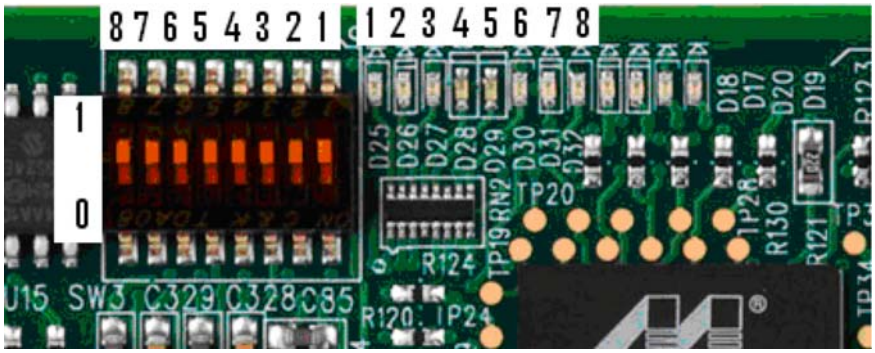
FPGA Test Pins

(see Appendix D, Figure 37)

General Purpose DIP Switch

General purpose FPGA pins are available for user applications. FPGA pins are connected to a SPST slide actuated DIP switch (SW3). The switches are connected to logic level 0 when moved to the ON position inward toward the board and a 1 when outward from the board. In Figure 21, the SW3 (left) switch position 1 is indicated with DOT.

Figure 21. PCB LEDs and Switches



The designated pins are connected according to Table 5.

Table 5. FPGA to DIP Pins

FPGA BGA	SW3 Switch Position
C25	1
D25	2
G26	3
G25	4
B28	5
A28	6
A26	7
A27	8

General Purpose LEDs

(see Appendix D, Figure 37)

The LEDs on the LatticeECP3 AMC Evaluation Board are connected to general-purpose FPGA I/Os. These LEDs can be used to indicate the status of user designs. The LEDs illuminate when the FPGA output is driven to a LOW. Table 6 lists the LEDs and their associated FPGA pins.

Table 6. LED Definitions

Name	FPGA Pin #	PCB Designator	LED Color
LED1	A29	D25	Red
LED2	A30	D26	Amber
LED3	H26	D27	Green
LED4	H25	D28	Blue
LED5	A31	D29	Blue
LED6	B31	D30	Green
LED7	C29	D31	Amber
LED8	C30	D32	Red

DDR2 Memory Devices

(see Appendix D, Figures 34 and 35)

- The board is equipped with two 1.8V, 256MB/84-ball BGA DDR2 SDRAM memory devices such as the Micron Technology MT47H16M16BG-3:B TR device.
- The DDR2 memory includes a 32-bit wide interface.
- The board includes termination of data, address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP3 device.

Table 7. DDR2 Memory Controller Interconnections

Net Name	LatticeECP3 FPGA
DQ0	W1
DQ1	W8
DQ2	W9
DQ3	W4
DQ4	W3
DQ5	Y2
DQ6	Y1
DQ7	Y8
DQ8	AA1
DQ9	Y7
DQ10	AA7
DQ11	AA4
DQ12	AA3
DQ13	AB2
DQ14	AB1

Net Name	LatticeECP3 FPGA
A0	R4
A1	R1
A2	R2
A3	P10
A4	P9
A5	R5
A6	R7
A7	P8
A8	N8
A9	P4
A10	P5
A11	N1
A12	N2
K_0	T2
K_0#	T1

Net Name	LatticeECP3 FPGA
DQ15	AA5
DQ16	AN1
DQ17	AN2
DQ18	AD9
DQ19	AD8
DQ20	AP2
DQ21	AP3
DQ22	AL3
DQ23	AK3
DQ24	AN3
DQ25	AM3
DQ26	AJ5
DQ27	AJ6
DQ28	AL5
DQ29	AM5
DQ30	AL4
DQ31	AM4
DQS0	W6
DQS0#	Y6
DQS1	AA10
DQS1#	AB9
DQS2	AJ2
DQS2#	AJ3
DQS3	AM6
DQS3#	AN6

Net Name	LatticeECP3 FPGA
K_1	AD4
K_1#	AD3
CAS#	T7
BA0	T6
BA1	T5
ODT	R3
CS0#	T3
WE#	T4
VREF	V7
DM0	W2
DM1	AA2
DM2	AJ4
DM3	AP5
CEO#	U9
RAS#	R8

Ethernet Interface

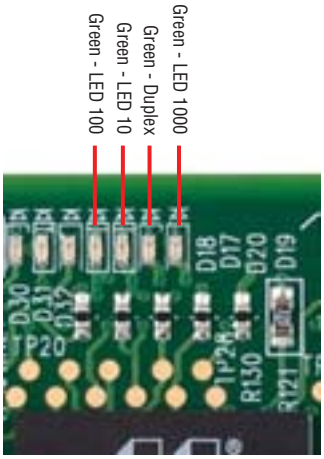
(see Appendix D, Figure 33)

The Marvell 88E1111 Gigabit Ethernet transceiver device (U17) is included on-board. This physical layer device supports 1000BASE-T, 100BASE-TX, and 10BASE-T applications via a standard media interface to an RJ-45 (Bel Stewart "MAGJACK", part number L829-1J1T-43) connection. The RJ-45 connection includes network magnetics that provide the proper signal conditioning, electro-magnetic interference suppression and signal isolation. This connector includes two LEDs and the board includes four status LEDs from the Marvell device. The LEDs are register-programmed. Detailed descriptions can be found in the Marvell data sheet.

Table 8. PHY Status Indicators

LED	Status Description
RJ45- Yellow	LED RX
RJ45- Yellow	LED TX
PCB Amber (D17)	LINK 10
PCB Amber (D18)	LINK 100
PCB Green (D19)	LINK 1000
PCB Amber (D20)	DUPLEX

Figure 22. Ethernet PHY Status LEDs



The Marvell 88E1111 device communicates via a MAC interface to the LatticeECP3 device via a SGMII SERDES interconnection.

Table 9. FPGA GPIO to PHY Interface

Signal	LatticeECP3 FPGA
phy_mdio	J21
phy_mdc	H22
phy_resetn	A23
phy_int_n	B23
phy_freq_sel	E22
phy_clk25	E23
phy_125clk	C23
phy_crs	D23
phy_col	K22

CPLD Device

(see Appendix D, Figure 39, U27)

The board includes a Lattice MachXO (LCMXO-640C-MN100) CPLD device that is used in conjunction with the BSCAN2 linker design for managing the on-board JTAG chain. It is also used for general purpose board management functions. Table 10 lists connections from the MachXO device that are not associated with the BSCAN2 linker design.

Table 10. CPLD TO FPGA Interconnections

MachXO Pin	Connected to
B1	AMC Hotswap Switch SW4
C1	POWR1014A Input Pin 4
D2	LatticeECP3 GPIO AH27
D1	LatticeECP3 GPIO AH28
C2	LatticeECP3 GPIO AL29
E1	POWR1014A Output Pin 1
E2	POWR1014A Output Pin 10
F1	POWR1014A Input Pin 47

MachXO Pin	Connected to
F2	POWR1014A Output Pin 6
J1	LatticeECP3 GPIO D16
K1	LatticeECP3 GPIO K16
N14	AMC LED3 Blue
M14	AMC LED2 Green
L13	AMC LED1 Red
L14	AMC I^2C SDA AMC Pin 71
M13	AMC I^2C SCL AMC Pin 56

AMC Backplane Interface

(see Appendix D, Figure 39, CN1)

Table 11. AMC Edge Interface Connections

AMC Pin#	Name	Connected To	LatticeECP3 Pin
85	GND		
84	PWR	12VDC	
83	PS0#	See Schematic	
82	GND		
81	FCLKA-	See Schematic	
80	FCLKA+	See Schematic	
79	GND		
78	TCLKB-	N/C	
77	TCLKB+	N/C	
76	GND		
75	TCLKA-	N/C	
74	TCLKA+	N/C	
73	GND		
72	PWR	12VDC	
71	SDA_L	See Schematic	
70	GND		
69	RX7-	PCSB_HDINN0	AK17
68	RX7+	PCSB_HDINP0	AL17
67	GND		
66	TX7-	PCSB_HDOUTN0*	AN17
65	TX7+	PCSB_HDOUTP0 *	AP17
64	GND		
63	RX6-	PCSB_HDINN1	AK16
62	RX6+	PCSB_HDINP1	AL16
61	GND		
60	TX6-	PCSB_HDOUTN1*	AN16
59	TX6+	PCSB_HDOUTP1 *	AP16
58	GND		
57	PWR	12VDC	
56	SCL_L	See Schematic	
55	GND		

AMC Pin#	Name	Connected To	LatticeECP3 Pin
86	GND		
87	RX8-	PCSC_HDINN3	AK22
88	RX8+	PCSC_HDINP3	AL22
89	GND		
90	TX8-	PCSC_HDOUTN3*	AN22
91	TX8+	PCSC_HDOUTP3 *	AP22
92	GND		
93	RX9-	PCSC_HDINN2	AK23
94	RX9+	PCSC_HDINP2	AL23
95	GND		
96	TX9-	PCSC_HDOUTN2*	AN23
97	TX9+	PCSC_HDOUTP2 *	AP23
98	GND		
99	RX10-	PCSC_HDINN1	AK24
100	RX10+	PCSC_HDINP1	AL24
101	GND		
102	TX10-	PCSC_HDOUTN1*	AN24
103	TX10+	PCSC_HDOUTP1 *	AP24
104	GND		
105	RX11-	PCSC_HDINN0	AK25
106	RX11+	PCSC_HDINP0	AL25
107	GND		
108	TX11-	PCSC_HDOUTN0*	AN25
109	TX11+	PCSC_HDOUTP0 *	AP25
110	GND		
111	RX12-	N/C	
112	RX12+	N/C	
113	GND		
114	TX12-	N/C	
115	TX12+	N/C	
116	GND		

Table 11. AMC Edge Interface Connections (Continued)

AMC Pin#	Name	Connected To	LatticeECP3 Pin
54	RX5-	PCSB_HDINN2	AK15
53	RX5+	PCSB_HDINP2	AL15
52	GND		
51	TX5-	PCSB_HDOUTN2*	AN15
50	TX5+	PCSB_HDOUTP2 *	AP15
49	GND		
48	RX4-	PCSB_HDINN3	AK14
47	RX4+	PCSB_HDINP3	AL14
46	GND		
45	TX4-	PCSB_HDOUTN3*	AN14
44	TX4+	PCSB_HDOUTP3 *	AP14
43	GND		
42	PWR	12VDC	
41	ENABLE	See Schematic	
40	GND		
39	RX3-	N/C	
38	RX3+	N/C	
37	GND		
36	TX3-	N/C	
35	TX3+	N/C	
34	GND		
33	RX2-	N/C	
32	RX2+	N/C	
31	GND		
30	TX2-	N/C	
29	TX2+	N/C	
28	GND		
27	PWR	12VDC	
26	GA2	See Schematic	
25	GND		
24	RX1-	N/C	
23	RX1+	N/C	
22	GND		
21	TX1-	N/C	
20	TX1+	N/C	
19	GND		
18	PWR	12VDC	
17	GA1	See Schematic	
16	GND		
15	RX0-	PCSA_HDINN0	AK21
14	RX0+	PCSA_HDINP0	AL21
13	GND		
12	TX0-	PCSA_HDOUTN0*	AN21

AMC Pin#	Name	Connected To	LatticeECP3 Pin
117	RX13-	N/C	
118	RX13+	N/C	
119	GND		
120	TX13-	N/C	
121	TX13+	N/C	
122	GND		
123	RX14-	N/C	
124	RX14+	N/C	
125	GND		
126	TX14-	N/C	
127	TX14+	N/C	
128	GND		
129	RX15-	N/C	
130	RX15+	N/C	
131	GND		
132	TX15-	N/C	
133	TX15+	N/C	
134	GND		
135	RX16-	N/C	
136	RX16+	N/C	
137	GND		
138	TX16-	N/C	
139	TX16+	N/C	
140	GND		
141	RX17-	N/C	
142	RX17+	N/C	
143	GND		
144	TX17-	N/C	
145	TX17+	N/C	
146	GND		
147	RX18-	N/C	
148	RX18+	N/C	
149	GND		
150	TX18-	N/C	
151	TX18+	N/C	
152	GND		
153	RX19-	N/C	
154	RX19+	N/C	
155	GND		
156	TX19-	N/C	
157	TX19+	N/C	
158	GND		
159	RX20-	N/C	

Table 11. AMC Edge Interface Connections (Continued)

AMC Pin#	Name	Connected To	LatticeECP3 Pin	AMC Pin#	Name	Connected To	LatticeECP3 Pin
11	TX0+	PCSA_HDOUTP0 *	AP21	160	RX20+	N/C	
10	GND			161	GND		
9	PWR	12VDC		162	TX20-	N/C	
8	RSRVD8	N/C		163	TX20+	N/C	
7	GND			164	GND		
6	RSRVD6	N/C		165	TCK	N/C	
5	GA0	See Schematic		166	TMS	N/C	
4	MP	3.3VDC MP		167	TRST#	N/C	
3	PS1#	See Schematic		168	TDO	N/C	
2	PWR	12VDC		169	TDI	N/C	
1	GND			170	GND		

Notes:
*Denotes AC coupling capacitor is on board.
N/C = floating

FMC Interconnection

(see Appendix D, Figure 42, CN3)

A VITA57.1 compliant FPGA Mezzanine Card (FMC) connection in available on the AMC module. This connector provides a low overhead bridge to the unique user FMC.

Figure 23. FMC Interface Connection

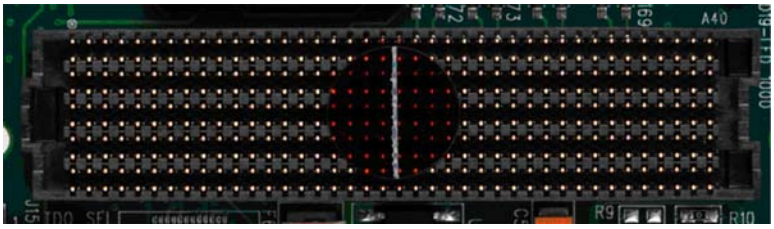


*Table 12. FPGA Mezzanine Card Connections**

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
A1	GND		
A2	DP1_M2C_P	PCSD_HDINP0	AL13
A3	DP1_M2C_N	PCSD_HDINN0	AK13
A4	GND		
A5	GND		
A6	DP2_M2C_P	PCSD_HDINP1	AL12
A7	DP2_M2C_N	PCSD_HDINN1	AK12
A8	GND		
A9	GND		
A10	DP3_M2C_P	PCSD_HDINP2	AL11
A11	DP3_M2C_N	PCSD_HDINN2	AK11
A12	GND		

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
A13	GND		
A14	DP4_M2C_P	PCSD_HDINP2	AL10
A15	DP4_M2C_N	PCSD_HDINN2	AK10
A16	GND		
A17	GND		
A18	DP5_M2C_P	N/C	
A19	DP5_M2C_N	N/C	
A20	GND		
A21	GND		
A22	DP1_C2M_P	PCSD_HDOUTP0	AP13
A23	DP1_C2M_N	PCSD_HDOUTN0	AN13
A24	GND		
A25	GND		
A26	DP2_C2M_P	PCSD_HDOUTP1	AP12
A27	DP2_C2M_N	PCSD_HDOUTN1	AN12
A28	GND		
A29	GND		
A30	DP3_C2M_P	PCSD_HDOUTP2	AP11
A31	DP3_C2M_N	PCSD_HDOUTN2	AN11
A32	GND		
A33	GND		
A34	DP4_C2M_P	PCSD_HDOUTP3	AP10
A35	DP4_C2M_N	PCSD_HDOUTN3	AN10
A36	GND		
A37	GND		
A38	DP5_C2M_P	N/C	
A39	DP5_C2M_N	N/C	
A40	GND		
B1	RES1	N/C	
B2	GND		
B3	GND		
B4	DP9_M2C_P	N/C	
B5	DP9_M2C_N	N/C	
B6	GND		
B7	GND		
B8	DP8_M2C_P	N/C	
B9	DP8_M2C_N	N/C	
B10	GND		
B11	GND		
B12	DP7_M2C_P	N/C	
B13	DP7_M2C_N	N/C	
B14	GND		
B15	GND		

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
B16	DP6_M2C_P	N/C	
B17	DP6_M2C_N	N/C	
B18	GND		
B19	GND		
B20	GBTCLK1_M2C_P	RUM2_PLL	P30[2]
B21	GBTCLK1_M2C_N	RUM2_PLL	R29[2]
B22	GND		
B23	GND		
B24	DP9_C2M_P	N/C	
B25	DP9_C2M_N	N/C	
B26	GND		
B27	GND		
B28	DP8_C2M_P	N/C	
B29	DP8_C2M_N	N/C	
B30	GND		
B31	GND		
B32	DP7_C2M_P	N/C	
B33	DP7_C2M_N	N/C	
B34	GND		
B35	GND		
B36	DP6_C2M_P	N/C	
B37	DP6_C2M_N	N/C	
B38	GND		
B39	GND		
B40	RES0	N/C	
C1	GND		
C2	DP0_C2M_P	PCSA_HDOUTP2	AP19
C3	DP0_C2M_N	PCSA_HDOUTN2	AN19
C4	GND		
C5	GND		
C6	DP0_M2C_P	PCSA_HDINP2	AL19
C7	DP0_M2C_N	PCSA_HDINN2	Ak19
C8	GND		
C9	GND		
C10	LA06_P	GPIO_0[1]	D6
C11	LA06_N	GPIO_0[1]	C5
C12	GND		
C13	GND		
C14	LA10_P	GPIO_0[1]	A8
C15	LA10_N	GPIO_0[1]	A9
C16	GND		
C17	GND		
C18	LA14_P	GPIO_0[1]	G11

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
C19	LA14_N	GPIO_0[1]	G12
C20	GND		
C21	GND		
C22	LA18_P_CC	GPIO_0[1]	F10
C23	LA18_N_CC	GPIO_0[1]	E10
C24	GND		
C25	GND		
C26	LA27_P	GPIO_0[1]	C13
C27	LA27_N	GPIO_0[1]	G13
C28	GND		
C29	GND		
C30	SCL		
C31	SDA		
C32	GND		
C33	GND		
C34	GA0		
C35	12P0V	12VDC	
C36	GND		
C37	12P0V	12VDC	
C38	GND		
C39	3P3V	3.3VDC	
C40	GND		
D1	PG_C2M		AP27
D2	GND		
D3	GND		
D4	GBTCLK0_M2C_P	RUM0_GPLL	V34[2]
D5	GBTCLK0_M2C_N	RUM0_GPLL	V33[2]
D6	GND		
D7	GND		
D8	LA01_P_CC	GPIO_0[1]	B1
D9	LA01_N_CC	GPIO_0[1]	B2
D10	GND		
D11	LA05_P	GPIO_0[1]	B4
D12	LA05_N	GPIO_0[1]	A3
D13	GND		
D14	LA09_P	GPIO_0[1]	B6
D15	LA09_N	GPIO_0[1]	A6
D16	GND		
D17	LA13_P	GPIO_0[1]	C11
D18	LA13_N	GPIO_0[1]	D11
D19	GND		
D20	LA17_P_CC	GPIO_0[1]	E11
D21	LA17_N_CC	GPIO_0[1]	F12
D22	GND		

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
D23	LA23_P	GPIO_0[1]	E13
D24	LA23_N	GPIO_0[1]	F14
D25	GND		
D26	LA26_P	GPIO_0[1]	D10
D27	LA26_N	GPIO_0[1]	E10
D28	GND		
D29	TCK	Connected to BSCAN Linker	
D30	TDI	Connected to BSCAN Linker	
D31	TDO	Connected to BSCAN Linker	
D32	3P3VAUX		
D33	TMS	Connected to BSCAN Linker	
D34	TRST_L	N/C	
D35	GA1		
D36	3P3V	3.3VDC	
D37	GND		
D38	3P3V	3.3VDC	
D39	GND		
D40	3P3V	3.3VDC	
E1	GND		
E2	HA01_P_CC	N/C	
E3	HA01_N_CC	N/C	
E4	GND		
E5	GND		
E6	HA05_P	N/C	
E7	HA05_N	N/C	
E8	GND		
E9	HA09_P	N/C	
E10	HA09_N	N/C	
E11	GND		
E12	HA13_P	N/C	
E13	HA13_N	N/C	
E14	GND		
E15	HA16_P	N/C	
E16	HA16_N	N/C	
E17	GND		
E18	HA20_P	N/C	
E19	HA20_N	N/C	
E20	GND		
E21	HB03_P	N/C	
E22	HB03_N	N/C	
E23	GND		
E24	HB05_P	N/C	

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
E25	HB05_N	N/C	
E26	GND		
E27	HB09_P	N/C	
E28	HB09_N	N/C	
E29	GND		
E30	HB13_P	N/C	
E31	HB13_N	N/C	
E32	GND		
E33	HB19_P	N/C	
E34	HB19_N	N/C	
E35	GND		
E36	HB21_P	N/C	
E37	HB21_N	N/C	
E38	GND		
E39	VADJ	GND	
E40	GND		
F1	PG_M2C		AN28
F2	GND		
F3	GND		
F4	HA00_P_CC	N/C	
F5	HA00_N_CC	N/C	
F6	GND		
F7	HA04_P	N/C	
F8	HA04_N	N/C	
F9	GND		
F10	HA08_P	N/C	
F11	HA08_N	N/C	
F12	GND		
F13	HA12_P	N/C	
F14	HA12_N	N/C	
F15	GND		
F16	HA15_P	N/C	
F17	HA15_N	N/C	
F18	GND		
F19	HA19_P	N/C	
F20	HA19_N	N/C	
F21	GND		
F22	HB02_P	N/C	
F23	HB02_N	N/C	
F24	GND		
F25	HB04_P	N/C	

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
F26	HB04_N	N/C	
F27	GND		
F28	HB08_P	N/C	
F29	HB08_N	N/C	
F30	GND		
F31	HB12_P	N/C	
F32	HB12_N	N/C	
F33	GND		
F34	HB16_P	N/C	
F35	HB16_N	N/C	
F36	GND		
F37	HB20_P	N/C	
F38	HB20_N	N/C	
F39	GND		
F40	VADJ	GND	
G1	GND		
G2	CLK0_C2M_P	PCLKT2	U26
G3	CLK0_C2M_N	PCLKC2	U27
G4	GND		
G5	GND		
G6	LA00_P_CC	GPIO_0[1]	C3
G7	LA00_N_CC	GPIO_0[1]	C4
G8	GND		
G9	LA03_P	GPIO_0[1]	B3
G10	LA03_N	GPIO_0[1]	A2
G11	GND		
G12	LA08_P	GPIO_0[1]	B7
G13	LA08_N	GPIO_0[1]	A7
G14	GND		
G15	LA12_P	GPIO_0[1]	J12
G16	LA12_N	GPIO_0[1]	K12
G17	GND		
G18	LA16_P	GPIO_0[1]	K13
G19	LA16_N	GPIO_0[1]	J13
G20	GND		
G21	LA20_P	GPIO_0[1]	J14
G22	LA20_N	GPIO_0[1]	H13
G23	GND		
G24	LA22_P	GPIO_0[1]	K14
G25	LA22_N	GPIO_0[1]	K15
G26	GND		

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
G27	LA25_P	GPIO_0[1]	A13
G28	LA25_N	GPIO_0[1]	B13
G29	GND		
G30	LA29_P	GPIO_0[1]	D3
G31	LA29_N	GPIO_0[1]	C2
G32	GND		
G33	LA31_P	GPIO_0[1]	A14
G34	LA31_N	GPIO_0[1]	B14
G35	GND		
G36	LA33_P	GPIO_0[1]	D15
G37	LA33_N	GPIO_0[1]	E15
G38	GND		
G39	VADJ	GND	
G40	GND		
H1	VREF_A_M2C		
H2	PRSNT_M2C_L	GPIO_0[1]	J16
H3	GND		
H4	CLK0_M2C_P	GPIO_0[1]	A15
H5	CLK0_M2C_N	GPIO_0[1]	B15
H6	GND		
H7	LA02_P	GPIO_0[1]	E4
H8	LA02_N	GPIO_0[1]	D4
H9	GND		
H10	LA04_P	GPIO_0[1]	D5
H11	LA04_N	GPIO_0[1]	C6
H12	GND		
H13	LA07_P	GPIO_0[1]	A4
H14	LA07_N	GPIO_0[1]	A5
H15	GND		
H16	LA11_P	GPIO_0[1]	A10
H17	LA11_N	GPIO_0[1]	B10
H18	GND		
H19	LA15_P	GPIO_0[1]	B11
H20	LA15_N	GPIO_0[1]	K13
H21	GND		
H22	LA19_P	GPIO_0[1]	A12
H23	LA19_N	GPIO_0[1]	B12
H24	GND		
H25	LA21_P	GPIO_0[1]	D12
H26	LA21_N	GPIO_0[1]	E12
H27	GND		

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
H28	LA24_P	GPIO_0[1]	G13
H29	LA24_N	GPIO_0[1]	H14
H30	GND		
H31	LA28_P	GPIO_0[1]	J15
H32	LA28_N	GPIO_0[1]	H15
H33	GND		
H34	LA30_P	GPIO_0[1]	C14
H35	LA30_N	GPIO_0[1]	D15
H36	GND		
H37	LA32_P	GPIO_0[1]	G16
H38	LA32_N	GPIO_0[1]	G17
H39	GND		
H40	VADJ	GND	
J1	GND		
I2	CLK1_C2M_P	N/C	
J3	CLK1_C2M_N	N/C	
J4	GND		
J5	GND		
J6	HA03_P	N/C	
J7	HA03_N	N/C	
J8	GND		
J9	HA07_P	N/C	
J10	HA07_N	N/C	
J11	GND		
J12	HA11_P	N/C	
J13	HA11_N	N/C	
J14	GND		
J15	HA14_P	N/C	
J16	HA14_N	N/C	
J17	GND		
J18	HA18_P	N/C	
J19	HA18_N	N/C	
J20	GND		
J21	HA22_P	N/C	
J22	HA22_N	N/C	
J23	GND		
J24	HB01_P	N/C	
J25	HB01_N	N/C	
J26	GND		
J27	HB07_P	N/C	
J28	HB07_N	N/C	

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
J29	GND		
J30	HB11_P	N/C	
J31	HB11_N	N/C	
J32	GND		
J33	HB15_P	N/C	
J34	HB15_N	N/C	
J35	GND		
J36	HB18_P	N/C	
J37	HB18_N	N/C	
J38	GND		
J39	VIO_B_M2C	N/C	
J40	GND		
K1	VREF_B_M2C	N/C	
K2	GND		
K3	GND		
K4	CLK1_M2C_P	N/C	
K5	CLK1_M2C_N	N/C	
K6	GND		
K7	HA02_P	N/C	
K8	HA02_N	N/C	
K9	GND		
K10	HA06_P	N/C	
K11	HA06_N	N/C	
K12	GND		
K13	HA10_P	N/C	
K14	HA10_N	N/C	
K15	GND		
K16	HA17_P_CC	N/C	
K17	HA17_N_CC	N/C	
K18	GND		
K19	HA21_P	N/C	
K20	HA21_N	N/C	
K21	GND		
K22	HA23_P	N/C	
K23	HA23_N	N/C	
K24	GND		
K25	HB00_P_CC	N/C	
K26	HB00_N_CC	N/C	
K27	GND		
K28	HB06_P_CC	N/C	
K29	HB06_N_CC	N/C	

Table 12. FPGA Mezzanine Card Connections (Continued)*

FMC Pin	FMC Port	LatticeECP3 Port	LatticeECP3 BGA
K30	GND		
K31	HB10_P	N/C	
K32	HB10_N	N/C	
K33	GND		
K34	HB14_P	N/C	
K35	HB14_N	N/C	
K36	GND		
K37	HB17_P_CC	N/C	
K38	HB17_N_CC	N/C	
K39	GND		
K40	VIO_B_M2C	N/C	

1. GPIO_0= LatticeECP3 Bank0/Top. These I/Os only support emulated LVDS differential outputs. Refer to the LatticeECP3 Family Data Sheet for details.
2, FPGA input pin only.

Technical Support Assistance

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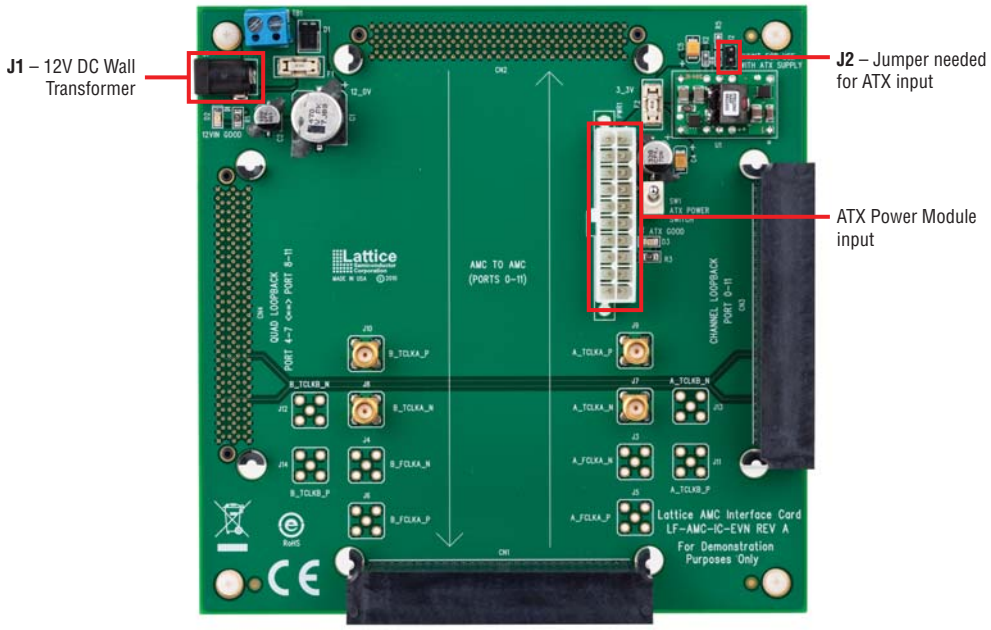
Revision History

Date	Version	Change Summary
September 2010	01.0	Initial release.
August 2012	01.1	Updated document with new corporate logo.
		Updated Programming schematic.

Appendix A. Lattice AMC Interface Card

A Lattice-supplied bench board is available for simple demonstrations. The Lattice AMC Interface Card provides a simple interface for powering the LatticeECP3 AMC Evaluation Board when an AMC chassis or backplane is not available. The Lattice AMC Interface Card also provides hardware loopbacks and interfaces for simple debug and demonstrations.

Figure 24. Lattice AMC Interface Card



To supply power from the wall transformer, first remove the jumper shunt from J2, connect the output connection of the power cord to J1, and plug the wall transformer into an AC wall outlet. This will immediately power up the board and the green LED D2 will illuminate. The 12V DC input will supply both 12V DC and 3.3V DC to all four AMC socket connections. The wall-wart is a good source for simple and less power consuming evaluations.

TheLattice AMC Interface Card can alternately be connected to an ATX-style power supply via a standard 20-pin connection. A jumper must shunt J2. A switch SW1 will turn on power from an ATX supply that has an AC-supply and is in the power-on position. When the SW1 is in the ON position, green LEDs D2 and D3 will illuminate. The supply power from the ATX unit will supply both 12V DC and 3.3V DC to all four AMC socket connections. This supply is needed when multiple AMC modules are used with the card.

The Lattice AMC Interface Card incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided for use with a benchtop supply adjusted to provide a nominal +12V DC. It should be set up similar to the wall power supply, as described above.

When power is applied, the green LED D2 will illuminate indicating that 12V DC is present. Another green LED, D10, will also illuminate to indicate all individual supplies have come up to their operating levels

Figure 25. Lattice AMC Interface Card Orientation

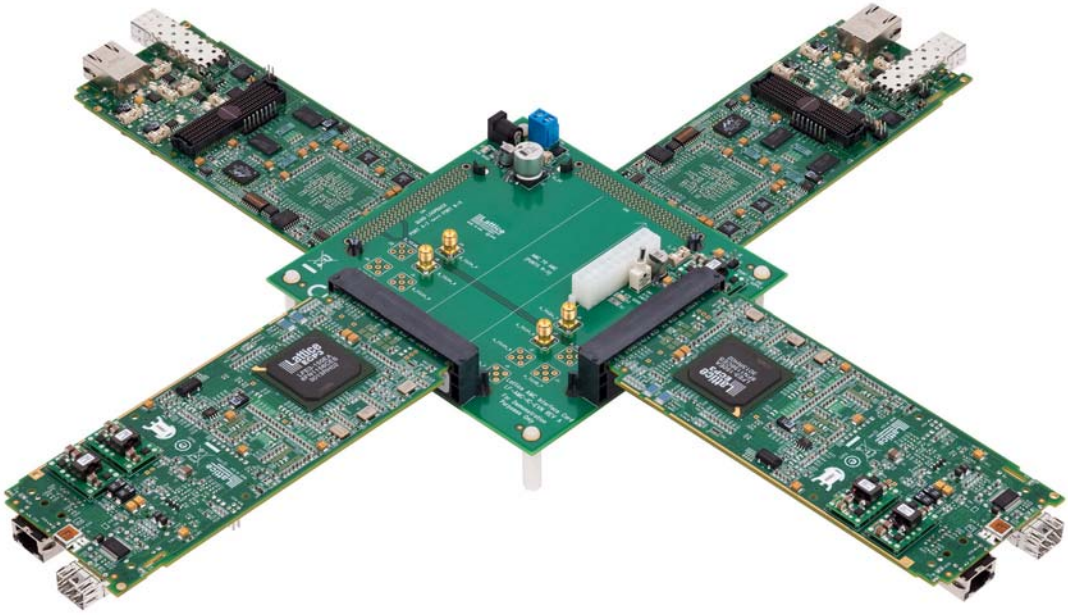


Figure 25 shows the correct orientation of the LatticeECP3 AMC Evaluation Boards in the Lattice AMC Interface Card. Users must assure correct insertion in the AMC sockets. Interface card schematics are shown in Appendix E and the bill of materials is shown in Appendix C.

Appendix B. LatticeECP3 AMC Evaluation Board Bill of Materials

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
1	1	CG1	SFP_CAGE	Tyco/AMP	6367034-1	Bottom EMI Cage
1a	1			Tyco/AMP	6367035-1	Top EMI Cage
2	1	CN1	AMC	EDGE FINGER		
3	1	CN2	HOST_SFP	Tyco/AMP	1367073-1	20-pin host connector
4	1	CN3	VITA57	ASP-134486-01		
5	2	C1, C2	100UF-D3POSCAP	Sanyo	16TQC100M	100UF, 16V, D3. POSCAP
6	5	C3, C5, C361, C406, C408	10UF-16V-TANTBSMT	AVX	TAJB106K016R	CAP TANTALUM 10UF 16V 10% SMD
7	2	C4, C12	330UF-DL3POSCAP	Sanyo	6TPE330MIL	330UF, 6.3V, D3L. POSCAP
8	3	C6, C7, C9	100UF-CER-1812SMT	Murata	GRM435R60J107ME20L	100UF, 6.3V, X5R, 1812
9	107	C14, C17, C28, C30, C32, C34, C36, C38, C40, C42, C52, C54, C56, C58, C60, C62, C64, C66, C70, C72, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C88, C89, C106, C111, C112, C114, C115, C117, C119, C186, C188, C191, C193, C195, C197, C230, C232, C234, C237, C247, C249, C252, C254, C257, C260, C262, C264, C266, C268, C270, C274, C277, C279, C281, C283, C285, C287, C288, C290, C292, C302, C303, C304, C306, C312, C314, C319, C321, C322, C324, C327, C329, C331, C338, C340, C342, C346, C348, C350, C358, C359, C360, C362, C364, C366, C368, C371, C372, C373, C387, C388, C389, C404, C405, C407, C409, C410	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
10	16	C15, C20, C22, C24, C26, C44, C46, C48, C50, C68, C86, C108, C189, C242, C245, C255	22UF-16V-TANTBSMT	Kemet	T491B226M016AT	CAPACITOR TANT 22UF 16V 20% SMD
11	25	C16, C21, C23, C25, C27, C45, C47, C49, C51, C69, C87, C107, C185, C190, C231, C243, C246, C256, C271, C272, C289, C351, C352, C353, C356	1UF-16V-0805SMT	Panasonic	ECJ-2FB1C105K	CAP 1UF 16V CERAMIC 0805 X5R
12	100	C18, C19, C29, C31, C33, C35, C37, C39, C41, C43, C53, C55, C57, C59, C61, C63, C65, C67, C71, C73, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C116, C118, C187, C194, C196, C198, C199, C200, C201, C235, C236, C248, C250, C251, C253, C258, C259, C261, C263, C265, C267, C269, C275, C276, C278, C280, C282, C284, C286, C297, C305, C307, C308, C309, C311, C313, C318, C320, C323, C325, C326, C328, C330, C337, C339, C341, C345, C347, C349, C357, C363, C365, C367, C369, C374, C376, C378, C380, C382, C384, C390, C392, C394, C396, C398, C400	10NF-0603SMT	Kemet	C0603C103K5RACTU	CAP .01UF 50V CERAMIC X7R 0603
13	2	C109, C113	100NF-0402SMT	Panasonic	ECJ-0EB1A104K	CAP .1UF 10V CERAMIC X5R 0402
14	13	C110, C202, C203, C204, C205, C206, C244, C273, C310, C317, C334, C335, C336	10NF-0402SMT	Panasonic	ECJ0EB1E103K	CAP .01UF 25V CERAMIC X7R 0402

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
15	32	C126, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C152, C153, C154, C155, C156, C157, C158, C161, C168, C169, C170, C171, C172, C173, C174, C175	100NFX5R-0402SMT	Kemet	C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402
16	3	C184, C233, C291	47UF-10V-TANTBSMT	Kemet	B45196H2476K209	CAP TANTALUM 47UF 10V 10% SMD
17	1	C192		AVX	0402YC223KAT2A	CAP CERM .022UF 10% 16V X7R 0402
18	2	C238, C298	100UF-D2EPOSCAP	Sanyo	6TPE100MI	100UF, 6.3V, D2E. POSCAP
19	2	C370, C386	6.8UF-TANT-0805SMT	Kemet	T494R685K006AS	CAP TANT 6.8UF 6.3V 10% SMD
	ALT	TACR685K010XTA				
20	12	C375, C377, C379, C381, C383, C385, C391, C393, C395, C397, C399, C401	560PF-0603SMT	Kemet	C0603C561K5RACTU	CAP 560PF 50V CERAMIC X7R 0603
21	41	C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453	1000PF-0402SMT	Panasonic	ECJ-0EB1E102K	CAP 1000PF 25V CERAMIC X7R 0402
22	2	D1, D35	SCHOTTKY/VISHAY-V12P10	Vishay	V12P10-M3/87A	TO277 SCHOTTKY DIODE
23	2	D2, D37	LED_GREEN_0603	Panasonic	LNJ336W83RA	LED GREEN 0603 SMD
24	12	D10, D15, D16, D19, D20, D27, D30, D33, D34, D39, D40, D41	LED_GREEN_0402	Rohm	SML-P12PTT86	LED GREEN 0.2MM 13MCD 0402 SMD
25	5	D12, D13, D14, D25, D32	LED_RED_0402	Rohm	SML-P12VTT86	LED RED 0.2MM 60MCD 0402 SMD
26	4	D17, D18, D26, D31	LED_AMBER_0402	Avago	HSMA-C280	LED CHIP ALINGAP AMBER TOP MOUNT 0402SMD
	ALT	SML-P12YT	YELLOW			
	ALT	SML-P12DT	ORANGE			
	ALT	SML	AMBER			
27	2	D28, D29	LED_BLUE_0402	Kingbright	APHHS1005PBC/A	LED 1X0.5MM 470NM BL WTR CLR SMD
28	1	D36	LED_BLUE_0603	Panasonic	LNJ936W8CRA	LED BLUE HIGH BRIGHT 0603 SMD
29	1	D38	LED_RED_0603	Panasonic	LNJ236W82RA	LED RED HIGH BRIGHT ESS SMD
30	19	FB5, FB6, FB7, FB8, FB13, FB14, FB15, FB16, FB17, FB18, FB20, FB21, FB22, FB23, FB24, FB25, FB26, FB27, FB28	MPZ1608Y600B	TDK	MPZ1608Y600B	FERRITE CHIP 60 OHM 2.3A 0603
31	1	F1	F1251CT-ND	Littlefuse	0154010.DR	FUSEBLOCK WITH 10A FUSE SMD
32	5	F2, F3, F4, F5, F6	F1228CT-ND	Littlefuse	0154005.DR	FUSEBLOCK WITH 5A FUSE SMD
33	2	J2, J11	HEADER 2	Samtec	TSW-102-07-T-S	2x1-0.25 Header
34	0	J3	HEADER 2[DNP]			
35	1	J4	HEADER 8	Samtec	TSW-108-07-T-S	8x1-0.25 Header
36	1	J5	RJ-45	Bel Fuse	L-829-1J1T-43	Integrated RJ45 Connector
37	1	J9	USB_MINI_AB	MOLEX	56579-0576	
38	0	J10	HEADER 3(DNP)			
39	1	J13	HEADER 3	Samtec	TSW-103-07-T-S	3x1-0.25 Header
40	1	J14	HEADER 2X2	Samtec	TSW-102-07-T-D	2x2-0.25 Header
41	1	J15	HEADER 3	Samtec	TSW-103-07-T-S	3x1-0.25 Header
42	7	LP1, LP2, LP3, LP4, LP5, LP6, LP7	5016	Keystone Electronics	5016	TEST POINT PC COMPACT SMT
43	3	L1, L2, L3	1UH-1210SMT	Panasonic	ELJ-FA1R0KF2	Inductor 1uH 10% 230mA 1210 (Digikey PCD1008CT-ND)
44	2	MH1, MH2	MHOLE_1			

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
45	3	MH5, MH6, MH7	M HOLE2			
46	0	PNL1	FRONT PANEL			
47	4	PP1, PP2, PP3, PP4	PROBEPOINT			
48	1	Q2	NTMS4503	ON Semiconductor	NTMS4503NR2G	MOSFET N-CH 28V 14A 8-SOIC
49	5	Q4, Q5, Q6, Q7, Q9	2N2222/SOT23	Diodes Inc	MMBT2222A-7	TRANS NPN 40V 350MW SMD SOT-23
50	1	RN1	EXBV8V472JV	Panasonic	EXBV8V472JV	RES ARRAY 4.7K OHM 5% 4 RES SMD
51	1	RN2	EXB2HV681JV	Panasonic	EXB2HV681JV	RES ARRAY 680 OHM 5% 8 RES SMD
52	1	RN3	EXB2HV472JV	Panasonic	EXB2HV472JV	RES ARRAY 4.7K OHM 5% 8 RES SMD
53	1	RN4	EXB2HV201JV	Panasonic	EXB-2HV201JV	RES ARRAY 200 OHM 5% 8 RES SMD
	ALT					
54	3	RP1, RP2, RP3	CTS-RT1402B7	CTS Corporation Resistor/Electro-components	RT2402B7	RES NET DDR SDRAM 50 OHM 3X9 BGA
55	1	R1	680R-1206SMT	Panasonic	ERJ-8GEYJ681V	RES 680 OHM 1/4W 5% 1206 SMD
56	22	R6, R7, R10, R11, R102, R103, R104, R105, R185, R187, R198, R200, R213, R214, R228, R229, R242, R246, R287, R288, R296, R297	0R-0603SMT	Panasonic	ERJ-3GEY0R00V	RES ZERO OHM 1/10W 5% 0603 SMD
57	0	R8, R9, R188, R197, R199, R290, R291, R292, R293, R255, R260, R263, R267, R268, R272, R276	OPEN-0603SMT			
58	1	R16	12_1K-0603SMT	Susumu Co. Ltd.	RG1608P-1212-B-T5	RES 12.1K OHM 1/10W .1% 0603 SMD
59	2	R17, R22	2K-0603SMT	Panasonic	ERJ-3EKF2001V	RES 2.00K OHM 1/10W 1% 0603 SMD
60	3	R18, R19, R20	100R-0805SMT	Panasonic	ERJ-6GEYJ101V	RES 100 OHM 1/8W 5% 0805 SMD
61	8	R21, R23, R25, R183, R189, R194, R201, R281	1K-0603SMT	Panasonic	ERJ-3EKF1001V	RES 1.00K OHM 1/16W 1% 0603 SMD
62	1	R24	470R-0603SMT	Yageo	RC0603FR-07470RL	RES 470 OHM 1/10W 1% 0603 SMD
63	1	R26	806R-0603SMT	Panasonic	ERJ-3EKF8060V	RES 806 OHM 1/10W 1% 0603 SMD
64	33	R45, R51, R52, R53, R54, R55, R56, R58, R61, R64, R65, R66, R74, R75, R76, R77, R79, R80, R82, R83, R84, R85, R86, R90, R91, R93, R94, R100, R101, R278, R279, R280, R283	10K-0402SMT	Panasonic	ERJ-2RKF1002X	RES 10.0K OHM 1/16W 1% 0402 SMD
65	6	R35, R36, R37, R39, R41, R42	2_2K-0402SMT	Panasonic	ERJ-2RKF2201X	RES 2.20K OHM 1/10W 1% 0402 SMD
66	4	R44, R215, R216, R282	330R-0402SMT	Panasonic	ERJ-2RKF3300X	RES 330 OHM 1/10W 1% 0402 SMD
67	1	R59	100R-0603SMT	Panasonic	ERA-3YEB101V	RES 100 OHM 1/16W .1% 0603 SMD
68	3	R72, R73, R78	680R-0603SMT	Panasonic	ERJ-3GEYJ681V	RES 680 OHM 1/10W 5% 0603 SMD
69	2	R81, R96	220R-0603SMT	Panasonic	ERJ-3GEYJ221V	RES 220 OHM 1/10W 5% 0603 SMD
70	3	R87, R88, R89	OPEN-0402SMT			
71	12	R92, R217, R219, R220, R221, R222, R223, R224, R320, R27, R29, R30	10K-0603SMT	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1/10W 5% 0603 SMD
72	13	R95, R97, R118, R122, R123, R195, R218, R270, R275, R284, R285, R286, R298	4_7K-0402SMT	Panasonic	ERJ-2RKF4701X	RES 4.70K OHM 1/10W 1% 0402 SMD
73	4	R98, R99, R131, R132	100R-0402SMT	Panasonic	ERJ-2RKF1000X	RES 100 OHM 1/10W 1% 0402 SMD
74	6	R106, R107, R108, R109, R251, R252	680R-0402SMT	Panasonic	ERJ-2GEJ681X	RES 680 OHM 1/10W 5% 0402 SMD

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
75	25	R110, R111, R112, R113, R114, R115, R116, R117, R190, R191, R192, R193, R196, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R230, R250	50R-0402SMT	Vishay	FC0402E50R0BTBST1	RES 50 OHM 50MW .1% 0402 SMD
76	2	R119, R120	33R-0402SMT	Panasonic	ERJ-2GEJ330X	RES 33 OHM 1/16W 5% 0402 SMD
77	1	R121	22R-0603SMT	Yageo	RC0603FR-0722RL	RES 22.0 OHM 1/10W 1% 0603 SMD
78	12	R57, R60, R62, R63, R67, R124, R125, R126, R127, R128, R129, R130	0R-0402SMT	Panasonic	ERJ-2GE0R00X	RES ZERO OHM 1/10W 5% 0402 SMD
79	6	R231, R233, R238, R245, R258, R259	220R-0402SMT	Panasonic	ERJ-2RKF2200X	RES 220 OHM 1/10W 1% 0402 SMD
80	1	R184	4_7K-0603SMT	Panasonic	ERJ-3EKF4701V	RES 4.70K OHM 1/10W 1% 0603 SMD
81	1	R212	1_5K-0402SMT	Panasonic	ERJ-2RKF1501X	RES 1.50K OHM 1/16W 1% 0402 SMD
82	1	R225	270R-0603SMT	Panasonic	ERJ-3EKF2700V	RES 270 OHM 1/10W 1% 0603 SMD
83	2	R226, R227	330R-0603SMT	Panasonic	ERJ-3GEYJ331V	RES 330 OHM 1/10W 5% 0603 SMD
84	24	R232, R234, R235, R236, R237, R240, R241, R243, R244, R247, R248, R249, R254, R256, R257, R261, R262, R264, R266, R269, R271, R273, R274, R277	10R-0402SMT	Panasonic	ERJ-2RKF10R0X	RES 10.0 OHM 1/10W 1% 0402 SMD
85	2	R239, R265	470R-0402SMT	Panasonic	ERJ-2RKF4700X	RES 470 OHM 1/10W 1% 0402 SMD
86	1	R289	160R-2010SMT	Panasonic	ERJ-12ZYJ161U	RES 160 OHM 3/4W 5% 2010 SMD
87	2	R294, R295	1M-2500V	OHMCRAFT	HVC2512L1005LT	RES SMT 10M 2.5kV 20%
88	1	SEG1	ESD SEGMENT			
89	4	SP1, SP2, SP7, SP8	TEST POINT			
90	2	SW1, SW2	B3U-1000P	Omron	B3U-1000P	SWITCH TACT SPST W/O GND SMD
91	1	SW3	TDA DIP-8	ITT	TDA08H0SK1	SWITCH DIP 8POS HALF PITCH SMT
92	1	SW4	HOT SWAP	C&K	HDT0001	SWITCH DETECTOR SPST TOP ACT SMD
93	24	TP1, TP2, TP3, TP4, TP5, TP6, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35	TestPoint			
94	1	U1	ECP3-95-1156BGA	Lattice Supplied	ECP3-150EA-8FN1156I	1156-fpBGA
95	1	U2	PTH12060W	Texas Instruments	PTH12060WAH	TH MODULE PIP 12VIN 10A ADJ 10-TH
96	1	U3	PTH12060L	Texas Instruments	PTH12060LAH	TH MODULE PIP 12VIN 10A ADJ 10-TH(0.8v-1.8v)
97	3	U4, U5, U6	SC1592	Semtech	SC1592ISTRT	IC LDO ADJ REG 3A SOIC-8L
98	1	U7	ispPAC-POWR1014A-01T48/TN48	Lattice Supplied	ISPPAC-POWR1014A-01TN48I	48-TQFP
99	1	U8	M25P64-FLASH	Numonynx	M25P64-VMF6TP	IC SRL FLASH 64MBIT 3V 16-SOP Wide(300MIL)
100	2	U9, U11	NC7WZ16-MACO6A/Fairchild TinyLogic	Fairchild	NC7WZ16P6X	IC BUFFER UHS DUAL SC70-6
101	1	U10	MAX6817	Maxim	MAX6817-EUT+T	±15kV ESD-Protected, Dual, CMOS Switch Debouncers
102	1	U12	SN74LVC125A/SO14	Texas Instruments	SN74LVC125AD	IC QUAD BUS BUFFER GATE 14-SOIC
103	2	U13, U14	M29W32-FLASH	Numonynx	M29W320DB70ZE6F	IC FLASH 32MBIT 70NS 48TFBGA
104	1	U15	24AA1025-ISM	Microchip Technology	24AA1025-I/SM	IC SRL EEPROM 1024K 1.8V 8SOIC
105	1	U16	LT1963-ADJ	Linear Technology	LT1963ES8	IC REG LDO ADJ 1.5A LN 8SOIC
106	1	U17	88e1111	Marvell	88e1111-Bx-BAB-C000(Bx indicates any revision code)	Single-port Gigabit Ethernet (117 TFBGA)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
107	2	U20, U23	LP2997-SO8	National Semiconductor	LP2996M	IC DDR TERMINATION REG 8SOIC
108	2	U21, U22	DDR2-SDRAM-84FBGA	Micron Technology	MT47H16M16BG-3:B TR	IC DDR2 SDRAM 256MB 84-FBGA/3nS
109	1	U25	FT232R	Future Technology Devices International Ltd.	FTDI_FT232RL	USB Serial Converter SSOP28
110	1	U26	LTC4300A	Linear Technology	LTC4300A-1CMS8#PBF	IC BUFFER BUS 2WR HOTSWAP
111	1	U27	LCMXO640-M100/MN100	Lattice Supplied	LCMXO-640C-4-M100C	100-CBGA
112	2	U28, U30	ispClock5406D	Lattice Supplied	ISPPAC-CLK5406D-01SN48I	48-QFNS
113	1	U29	SN65MLVD3DRBT	Texas Instruments	SN65MLVD3DRBT	IC M-LVDS RECEIVER 1CH 8-SON
114	1	U31	NC7SZ125/SOT23	Fairchild	NC7SZ125P5X	IC BUFF TRI-ST UHS N-INV SC705
115	1	X1	156.25MHz	CTS	CB3LV-3I-156M2500	OSC 156.2500 MHZ 3.3V SMD
116	1	X2	125.00MHz	CTS	CB3LV-3I-125M0000	OSC 125.0000 MHZ 3.3V SMD
117	1	X3	SL-122_88MHz	Silicon Labs	530AA122M880DG	OSC 122.88MHZ 3.3V SMD
118	1	Y1	25MHz	Epson Toyocom Corporation	SG-636PCE 25.0000MC0:ROHS	OSCILLATOR 25.0000MHZ SMD 10.5mm x 5.8mm
119	3	R321,R322, R323	1K-0402SMT	Panasonic	ERJ-2RKF1001X	RES 1.00K OHM 1/10W 1% 0402 SMD

Appendix C. Lattice AMC Interface Card Bill of Materials

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
1	4	CN1, CN2, CN3, CN4	AMC			
2	1	C1	470UF-FKSMT	Panasonic	EEV-FK1V471Q	CAP 470UF 35V ELECT FK SMD
3	1	C2	100UF-FKSMT	Panasonic	EEE-FK1V101XP	CAP 100UF 35V ELECT FK SMD
4	1	C3	330UF-FKSMT	Panasonic	EEE-FK1C331P	CAP 330UF 16V ELECT FK SMD
5	2	C4, C5	10UF-16V-TANTBSMT	AVX	TAJB106K016R	CAP TANTALUM 10UF 16V 10% SMD
6	1	D1	SCHOTTKY/VISHAY-V12P10	Vishay	V12P10-E3/87A	TO277 SCHOTTKY DIODE
7	2	D2, D3	LED-SMT1206_GREEN	Panasonic	LNJ316C83RA	LED GREEN (UP) W/LENS 1206
8	1	F1	F1251CT-ND	Littlefuse		FUSEBLOCK WITH 10A FUSE SMD
9	1	F2	F1228CT-ND	Littlefuse	0154005.DR	FUSEBLOCK WITH 5A FUSE SMD
10	1	J1	22HP037-2.1mm	Condor	22HP037A	Power input
11	1	J2	HEADER 2	Samtec	TSW-102-07-T-S	2x1-0.25 Header
12	0	MH1, MH2, MH3, MH4	M HOLE2			
13	1	PWR1	MOLEX_39-29-9202			
14	2	R1, R3	470R-1206SMT	Panasonic	ERJ-8GEYJ471V	RES 470 OHM 1/4W 5% 1206 SMD
15	2	R2, R4	0R-0603SMT	Panasonic	ERJ-3GEY0R00V	RES ZERO OHM 1/10W 5% 0603 SMD
16	1	R5	2K-0603SMT	Panasonic	ERJ-3EKF2001V	RES 2.00K OHM 1/10W 1% 0603 SMD
17	1	SW1	SW SPST	C&K	ET2MD1CBE	
18	1	TB1	Terminal Block/ED1202DS	On-Shore Tech.	ED120/2DS	TERMINAL BLOCK 5.08MM VERT 2POS
19	1	U1	PTH12060W	Texas Instruments	PTH12060WAH	TH MODULE PIP 12VIN 10A ADJ 10-TH
	4	Standoffs MH1, MH3, MH4, MH5	Digikey 8440GK-ND or equal (1" nylon 4-40 threaded)			
	4		Screws - Digikey H542-ND or equal (nylon 4-40 screw) AND washer			
12	4	J3, J4, J5, J6,J7, J8, J9, J10, J11, J12, J13, J14	SMA	Molex	73391-0060	CONN JACK SMA STR 50 OHM PCB

Appendix D. LatticeECP3 AMC Evaluation Board Schematic

Figure 26. Cover Page

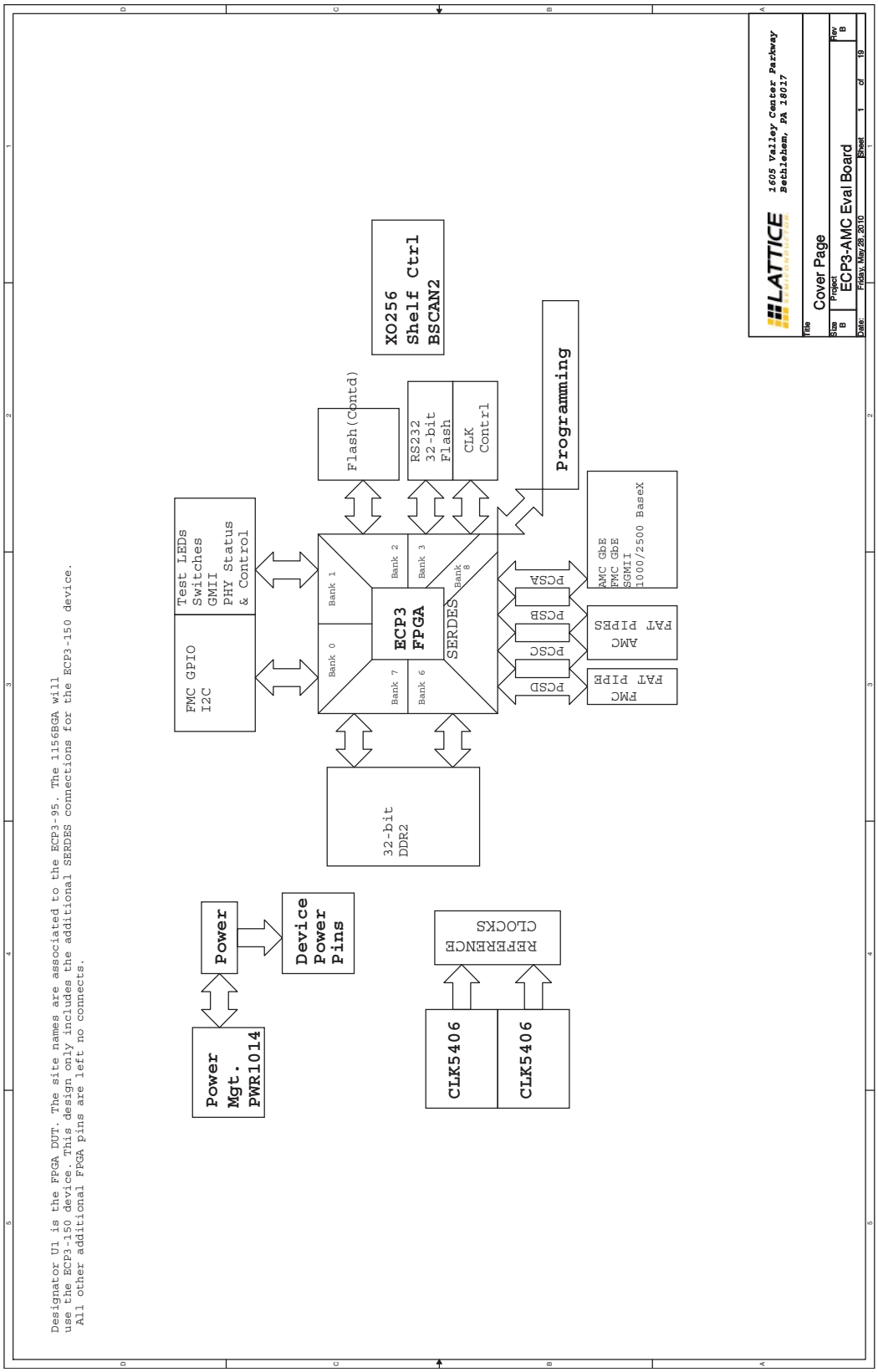


Figure 27. Power Generation

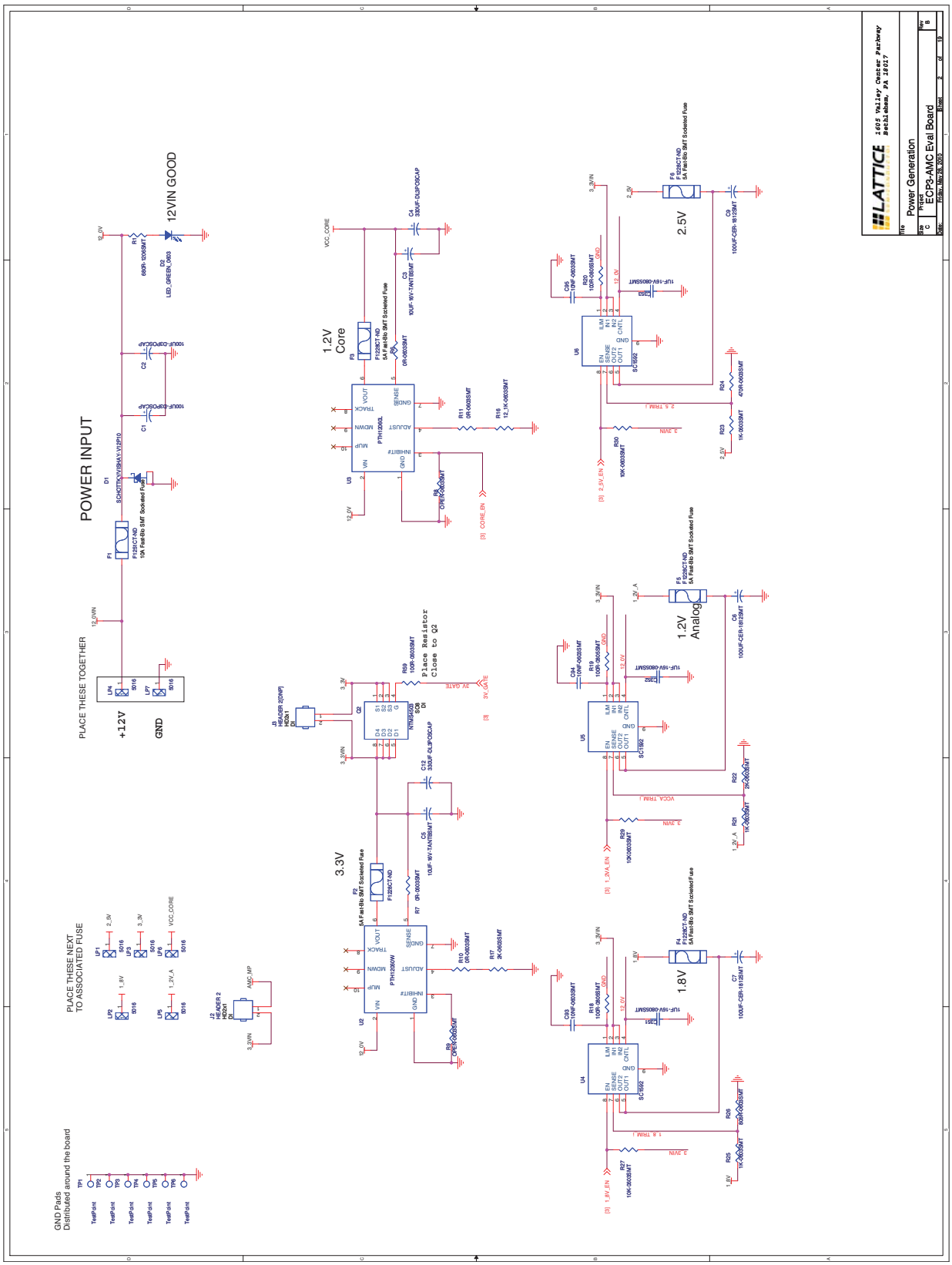


Figure 28. Power Management

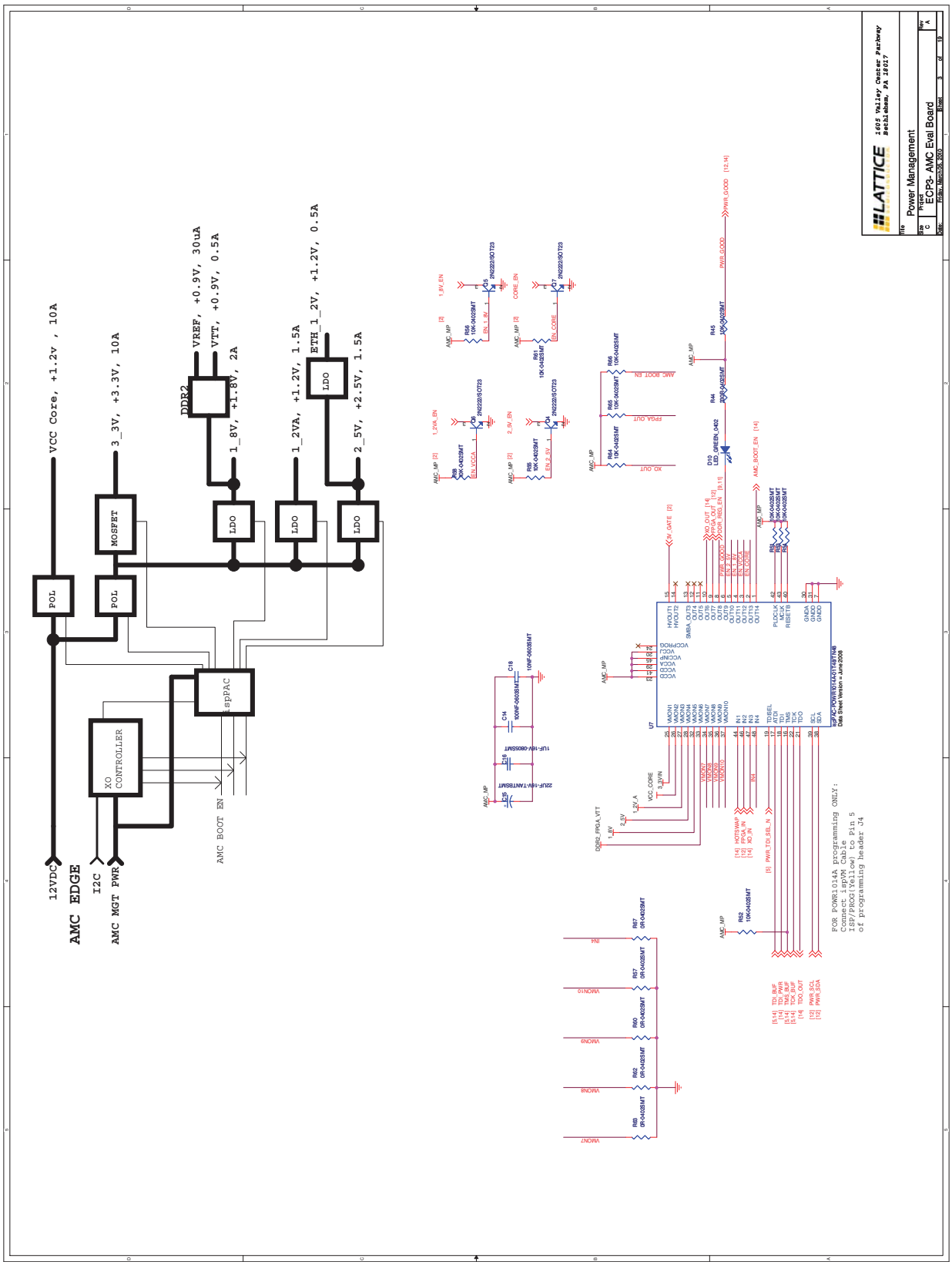


Figure 29. Power Supplies

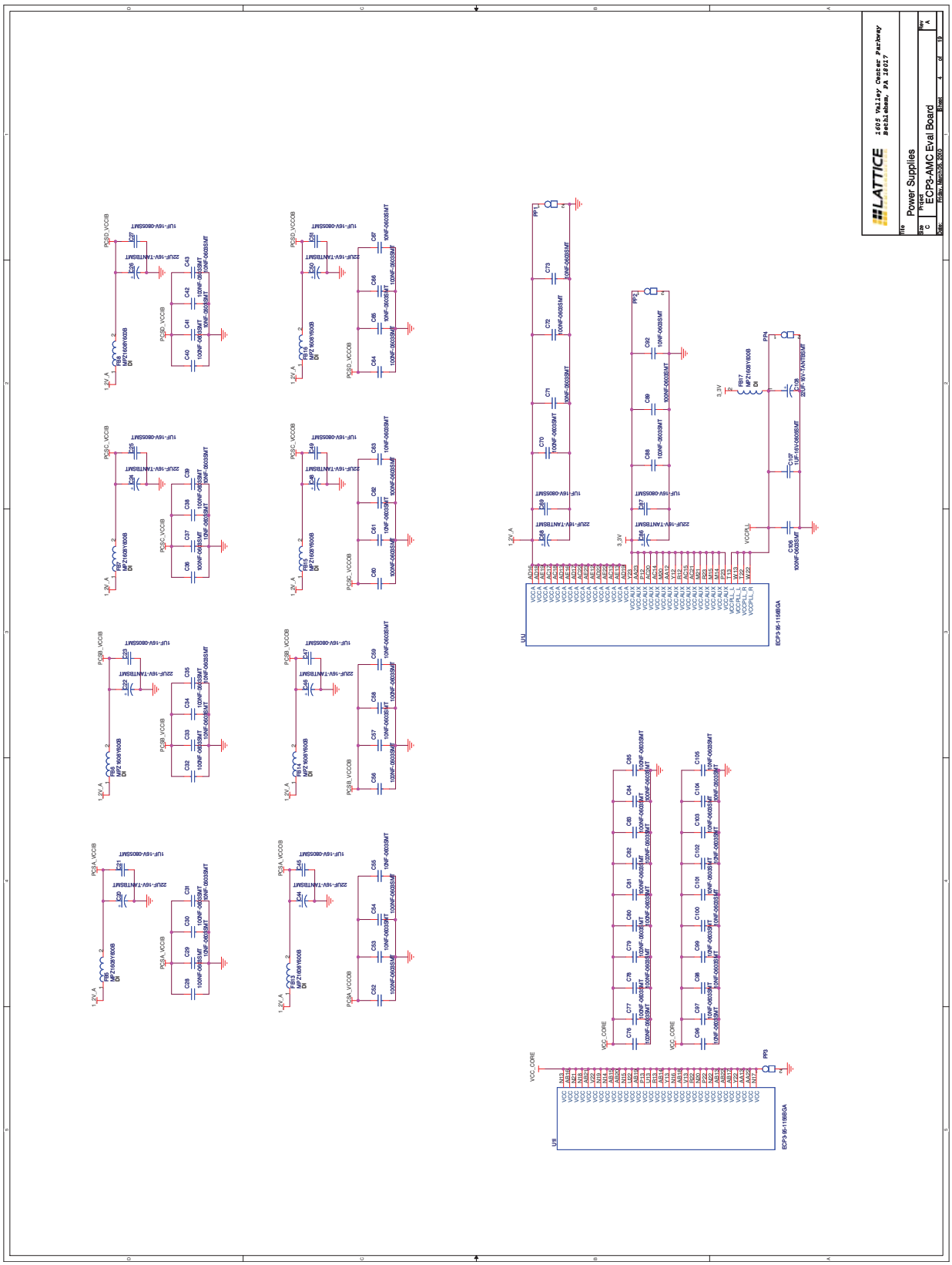


Figure 30. Programming

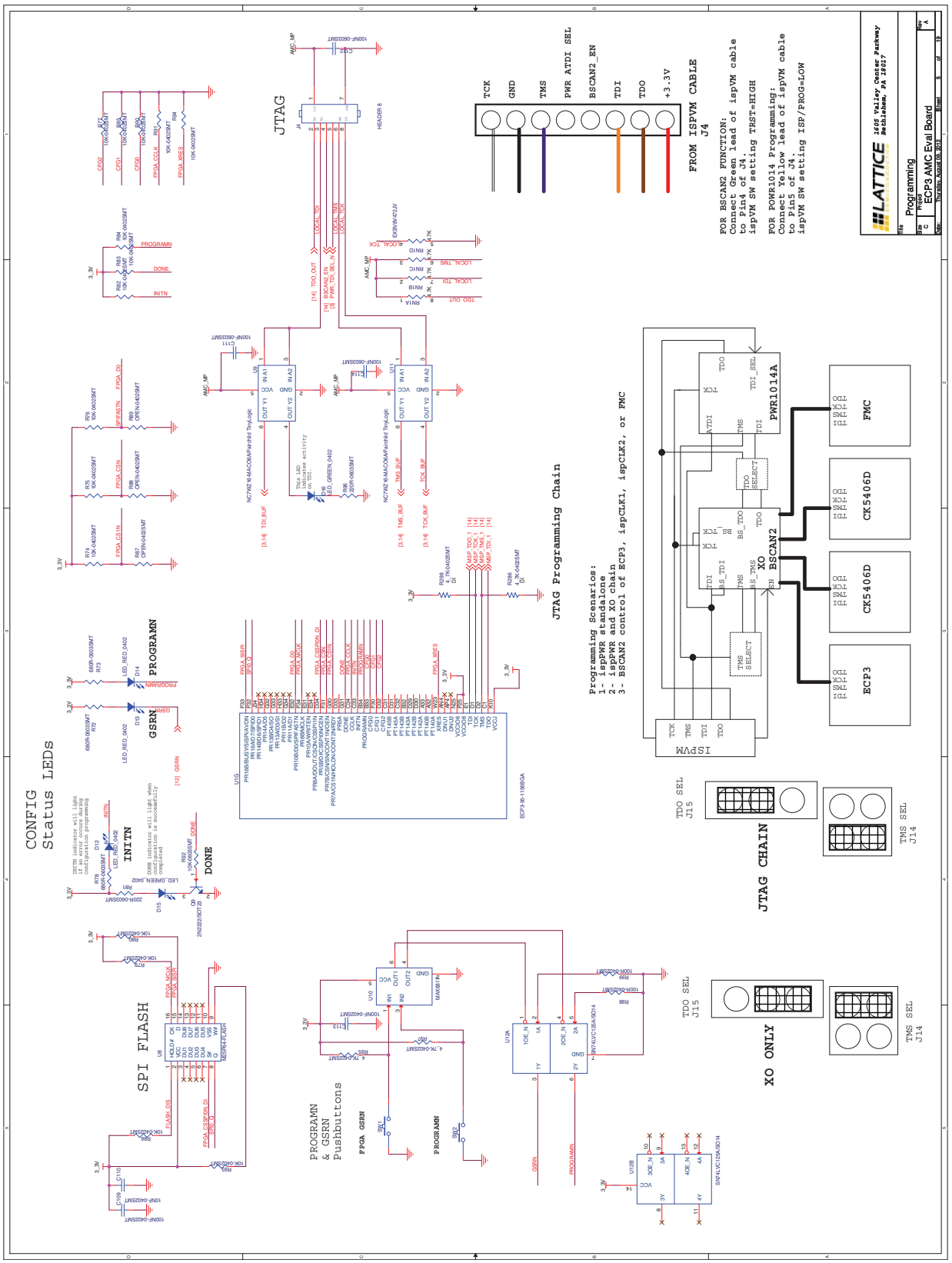


Figure 31. Parallel Flash/EEPROM

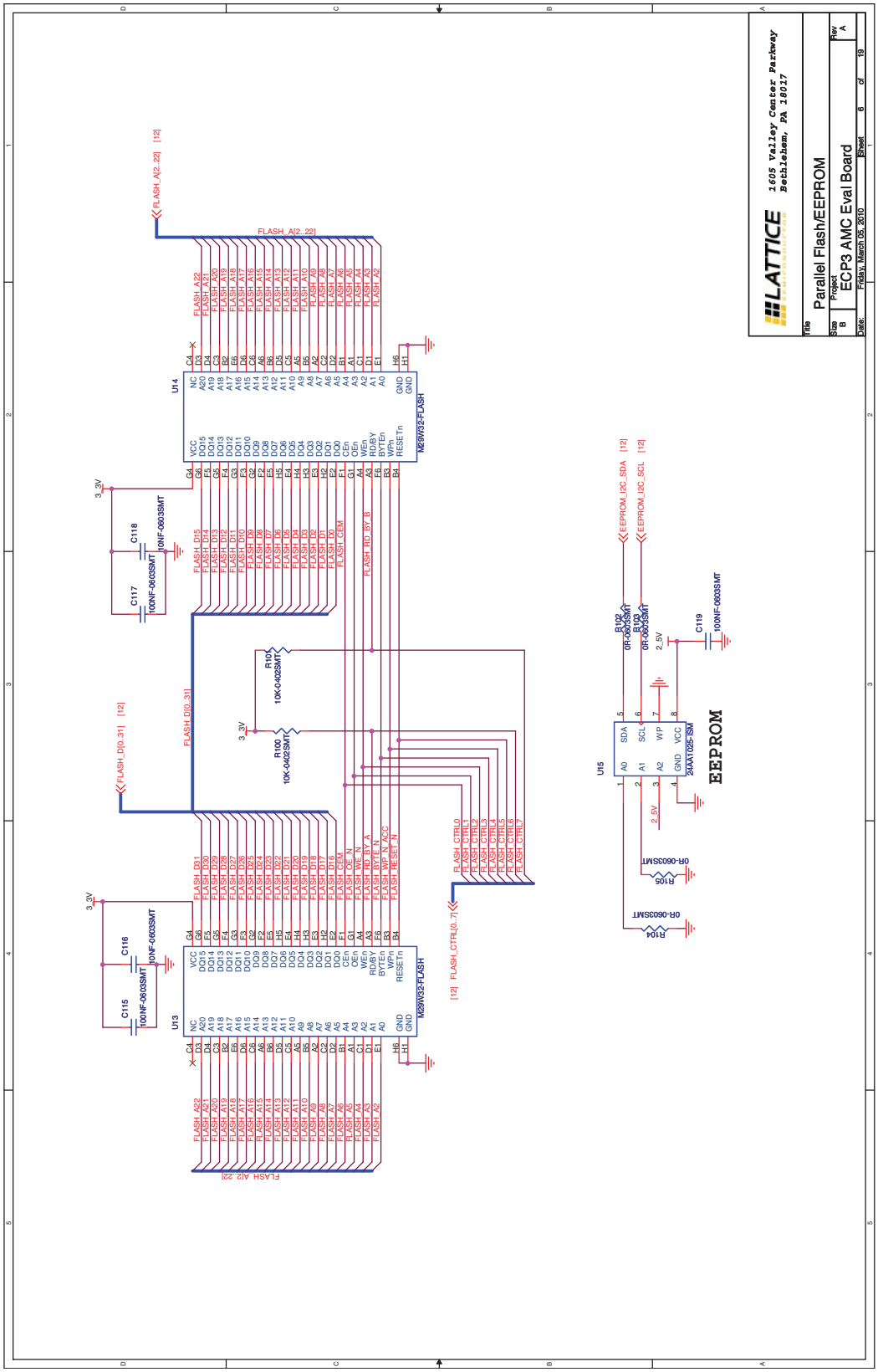


Figure 32. SERDES

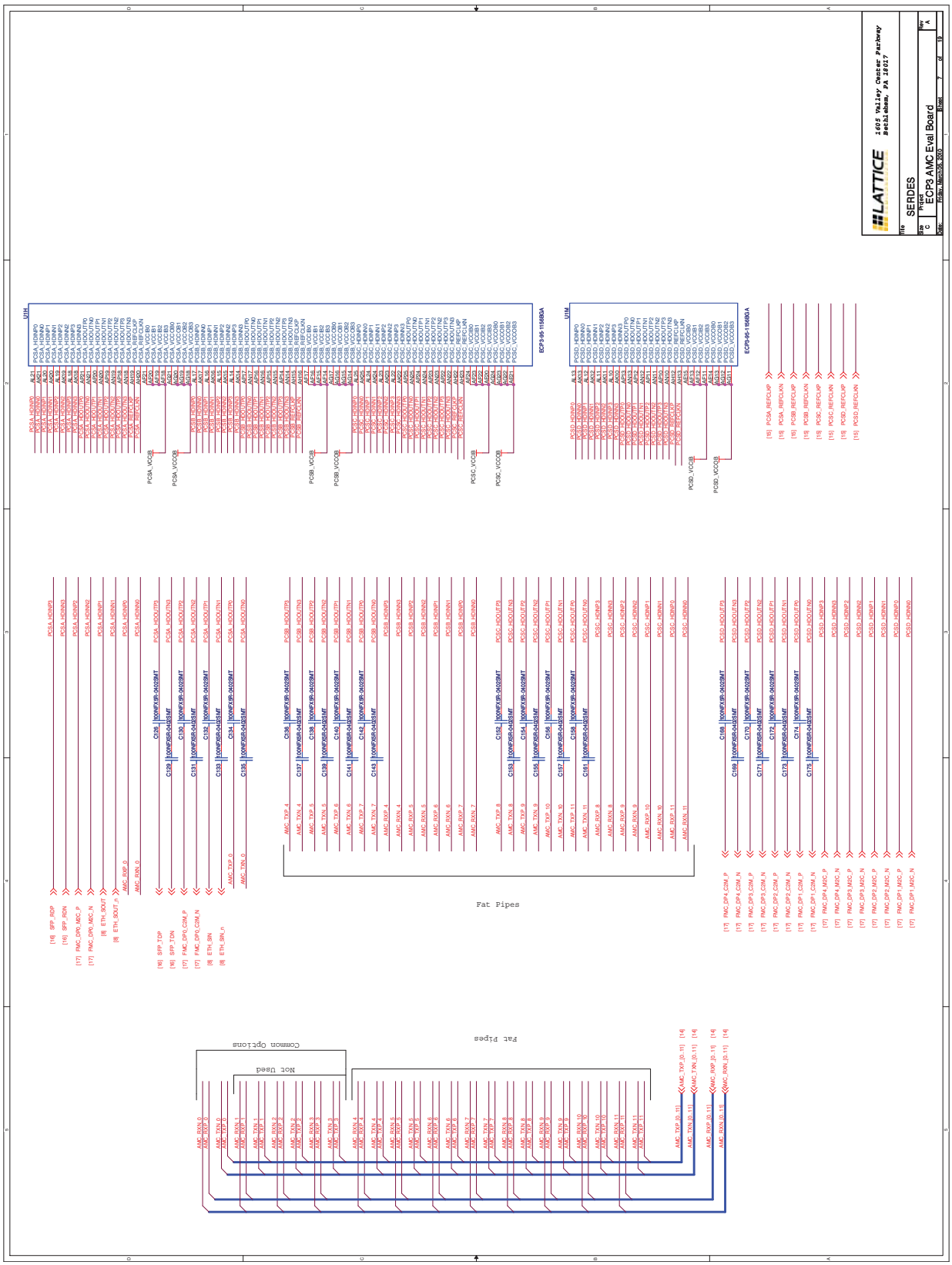


Figure 33. 1000BASE-T PHY/RJ45

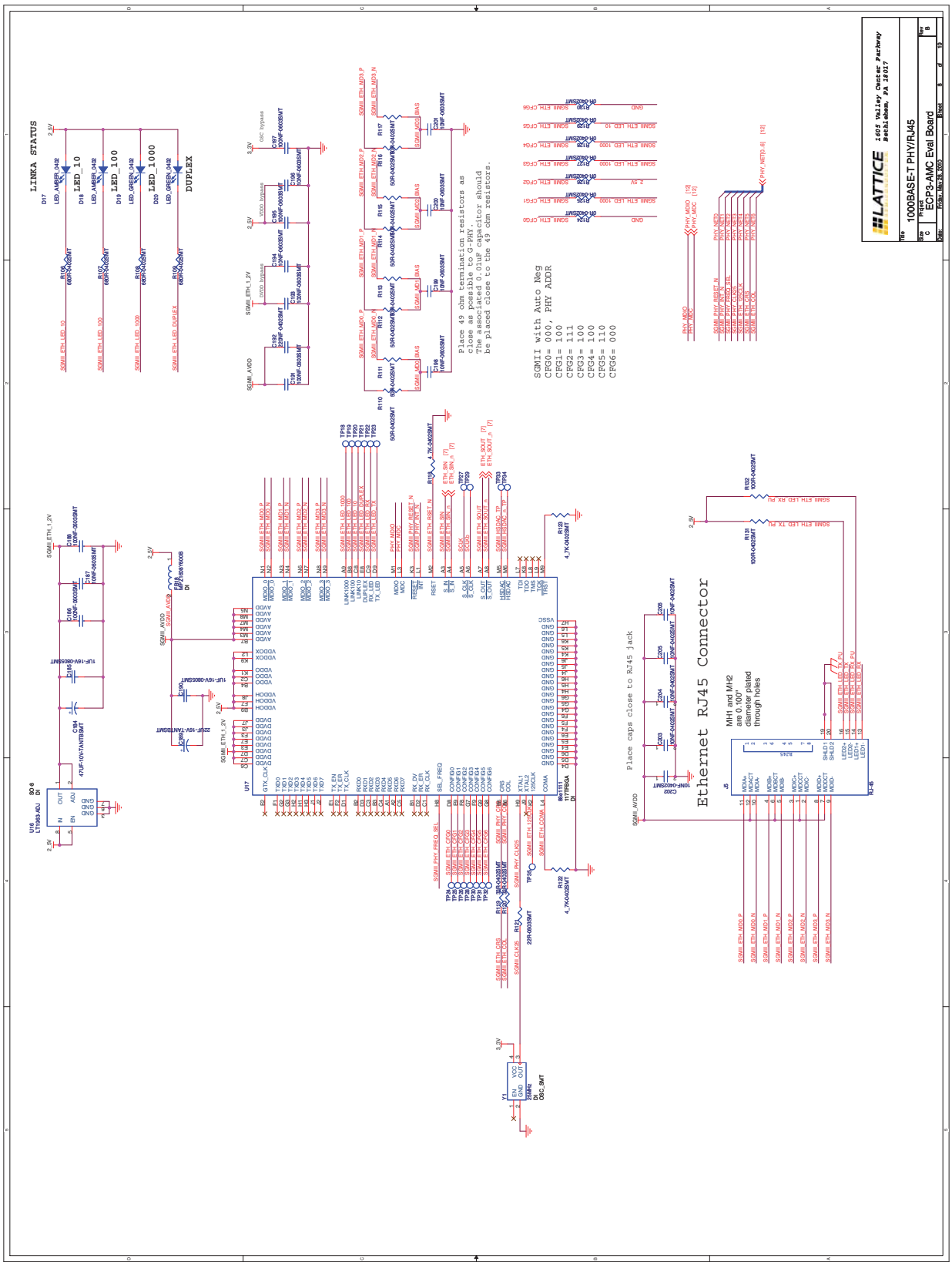


Figure 34. DDR2 Memory

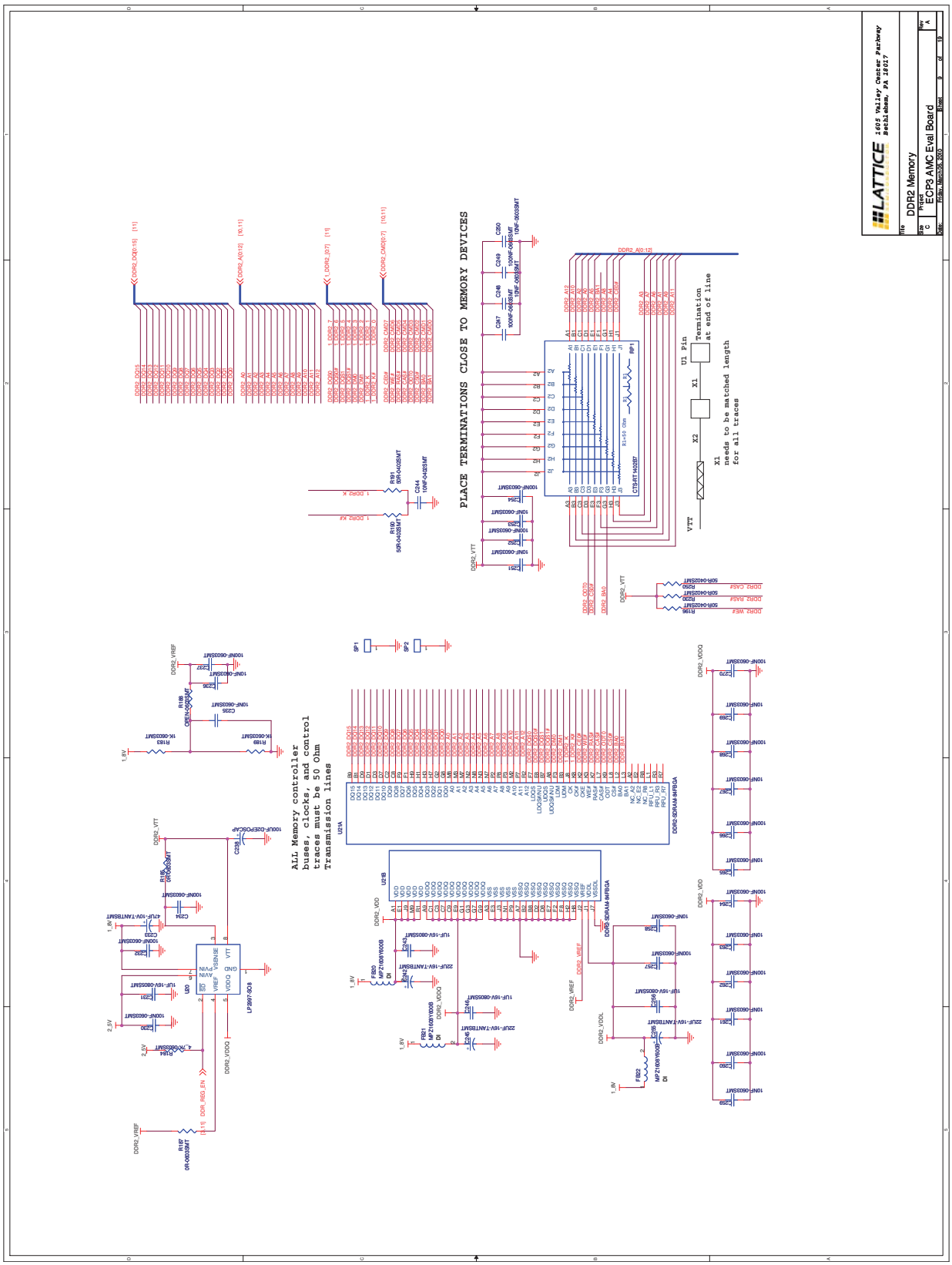


Figure 35. DDR2 Memory

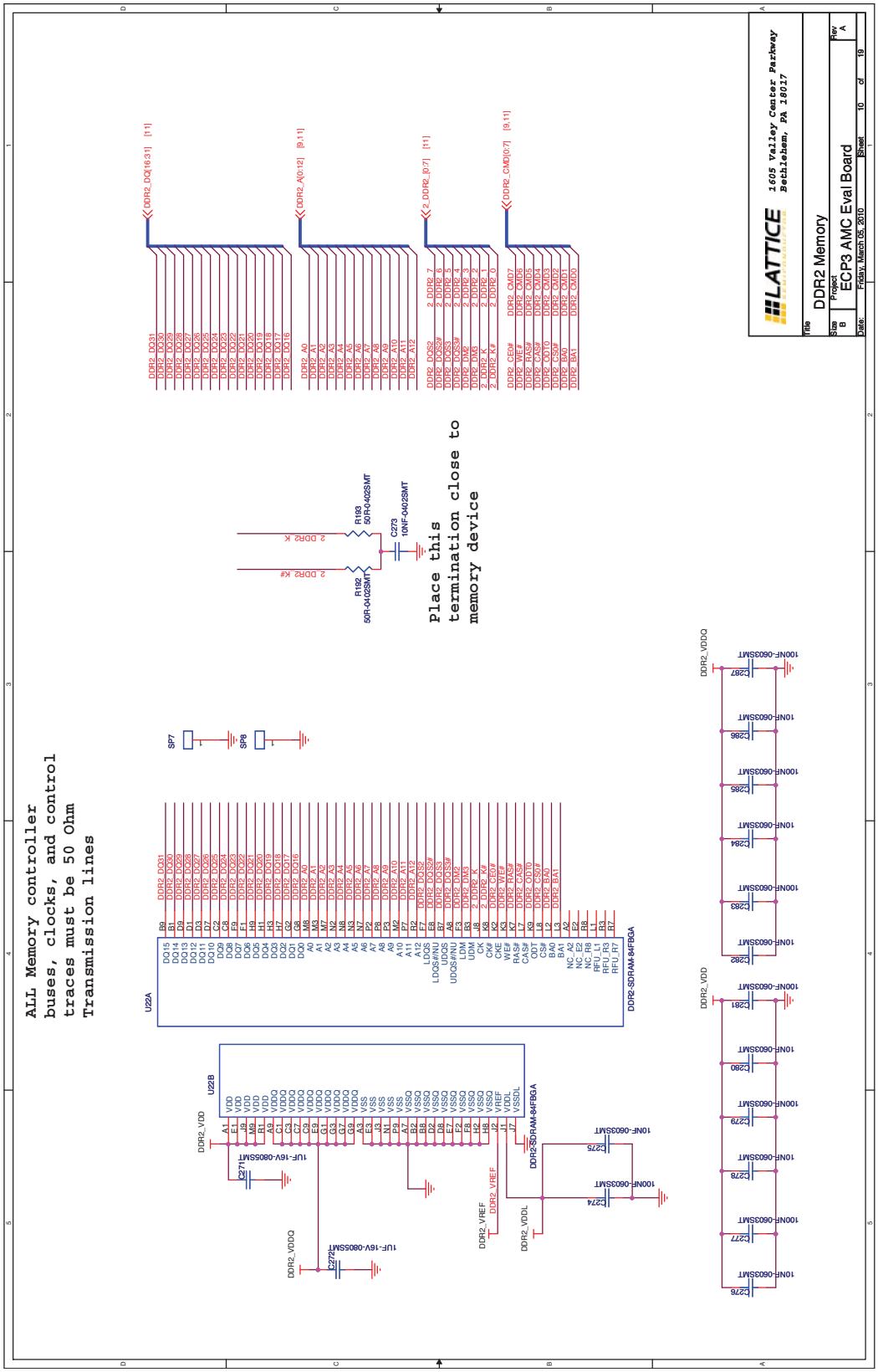


Figure 36. Memory Controllers

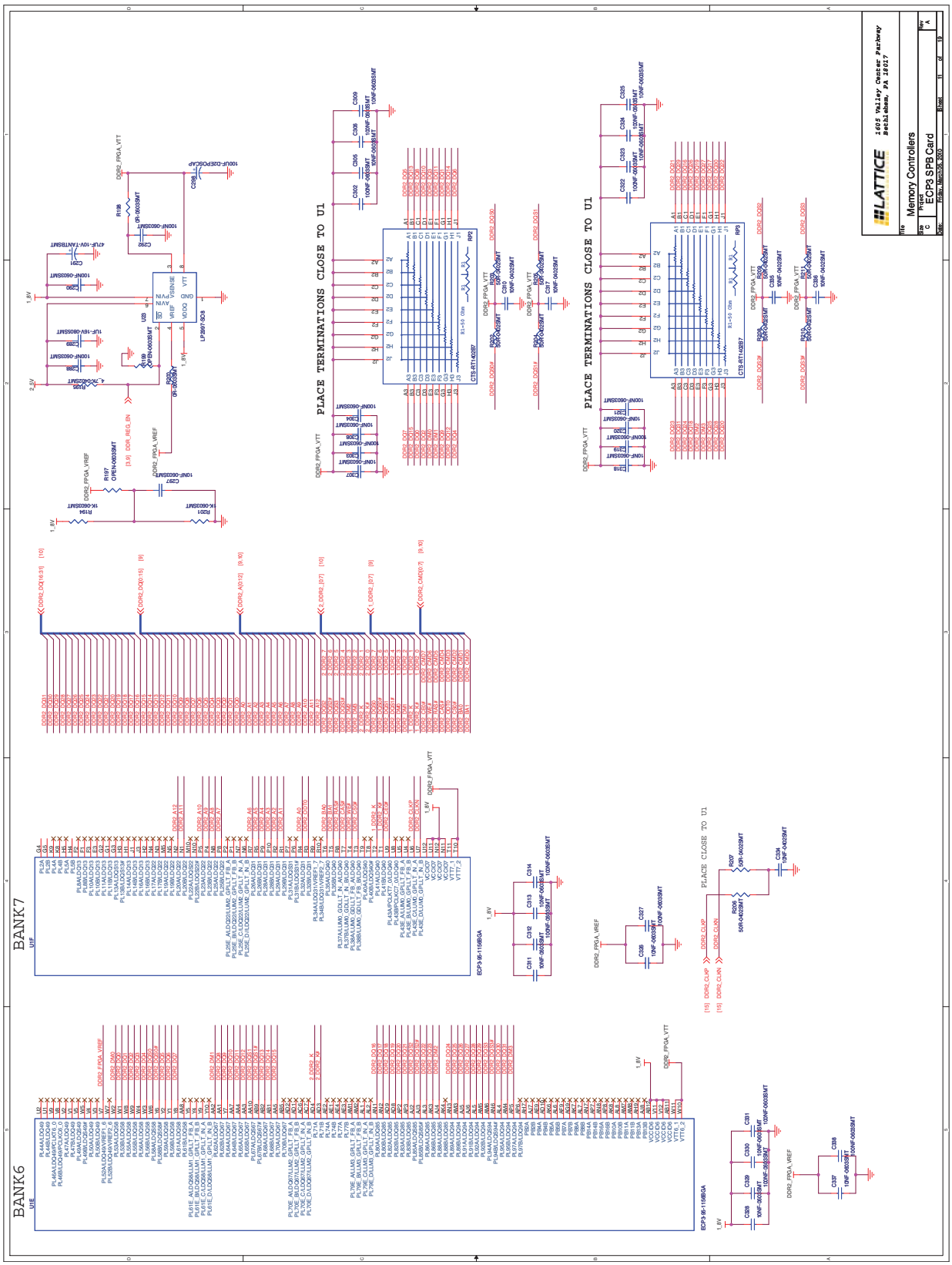


Figure 37. FPGA Pins

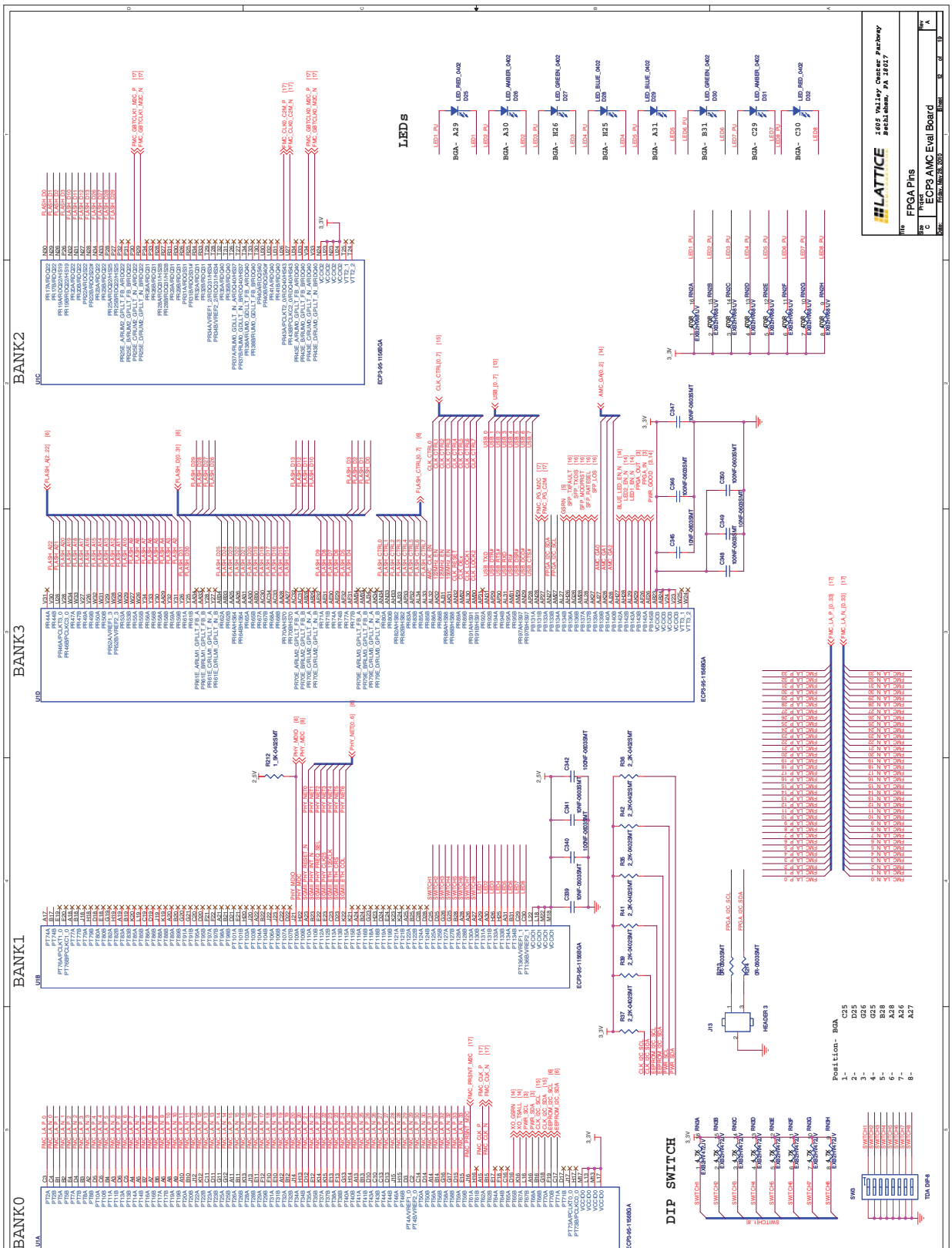


Figure 38. RS232

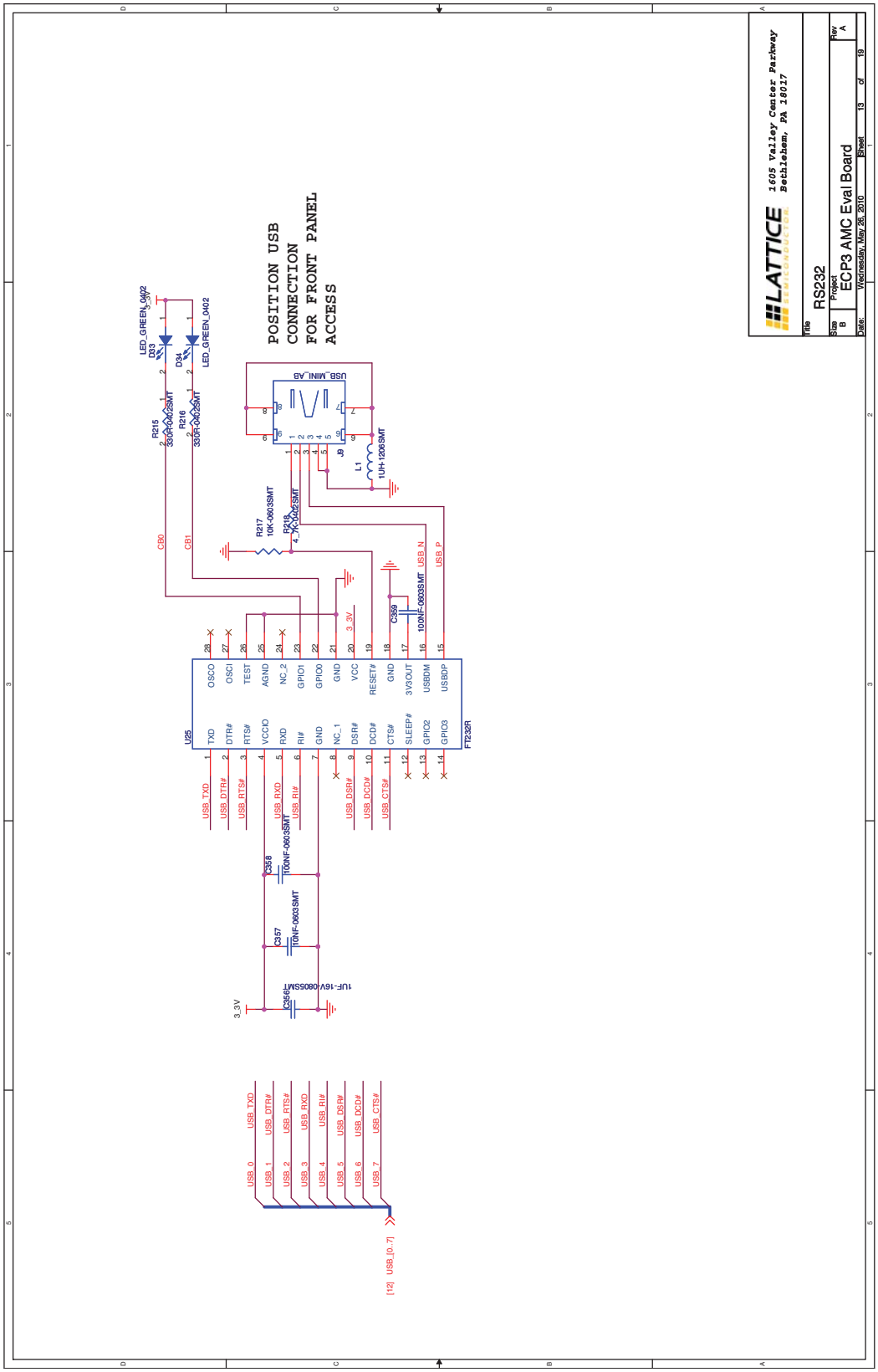


Figure 39. AMC Backplane

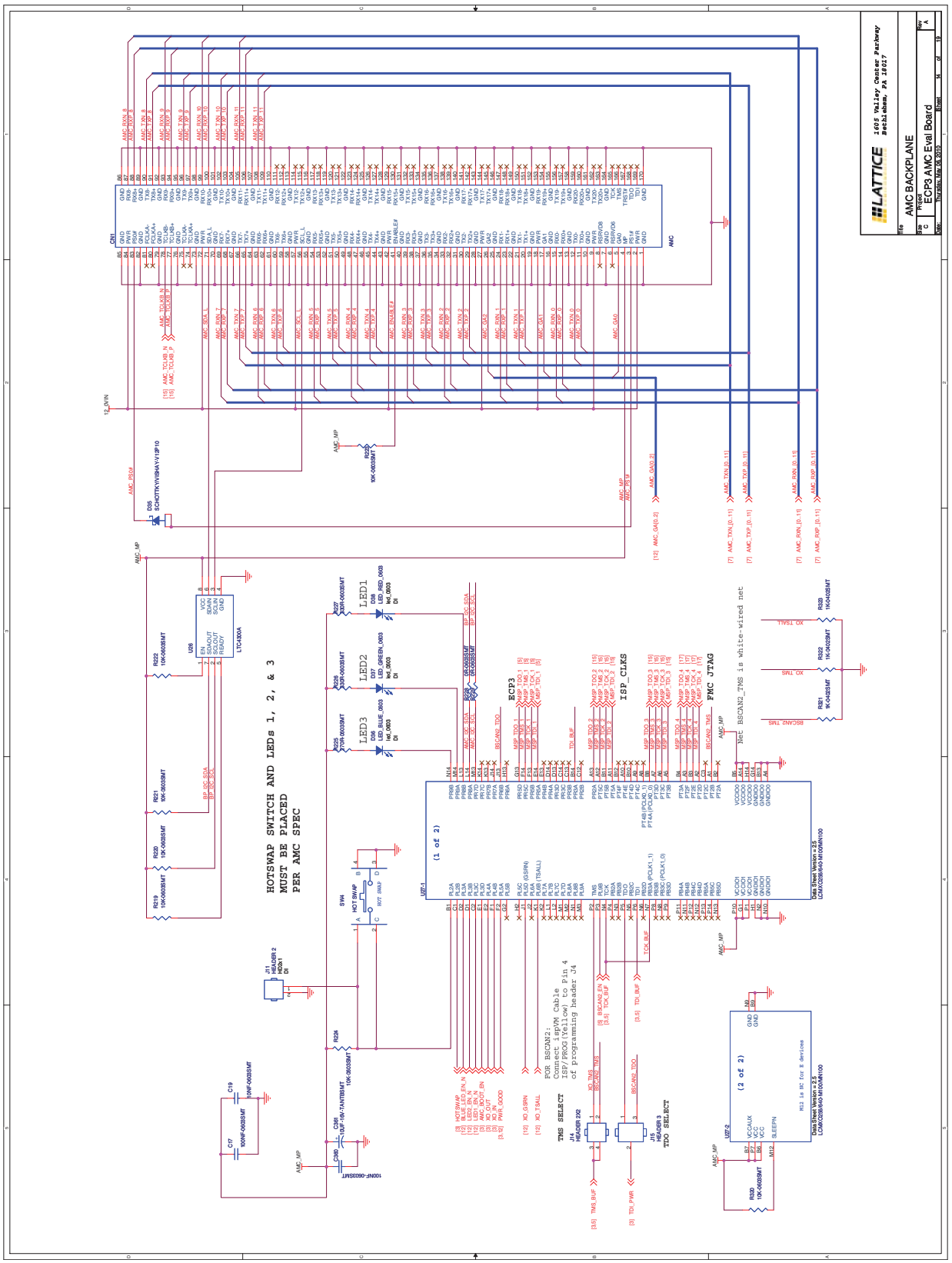


Figure 40. Reference Clock Generation

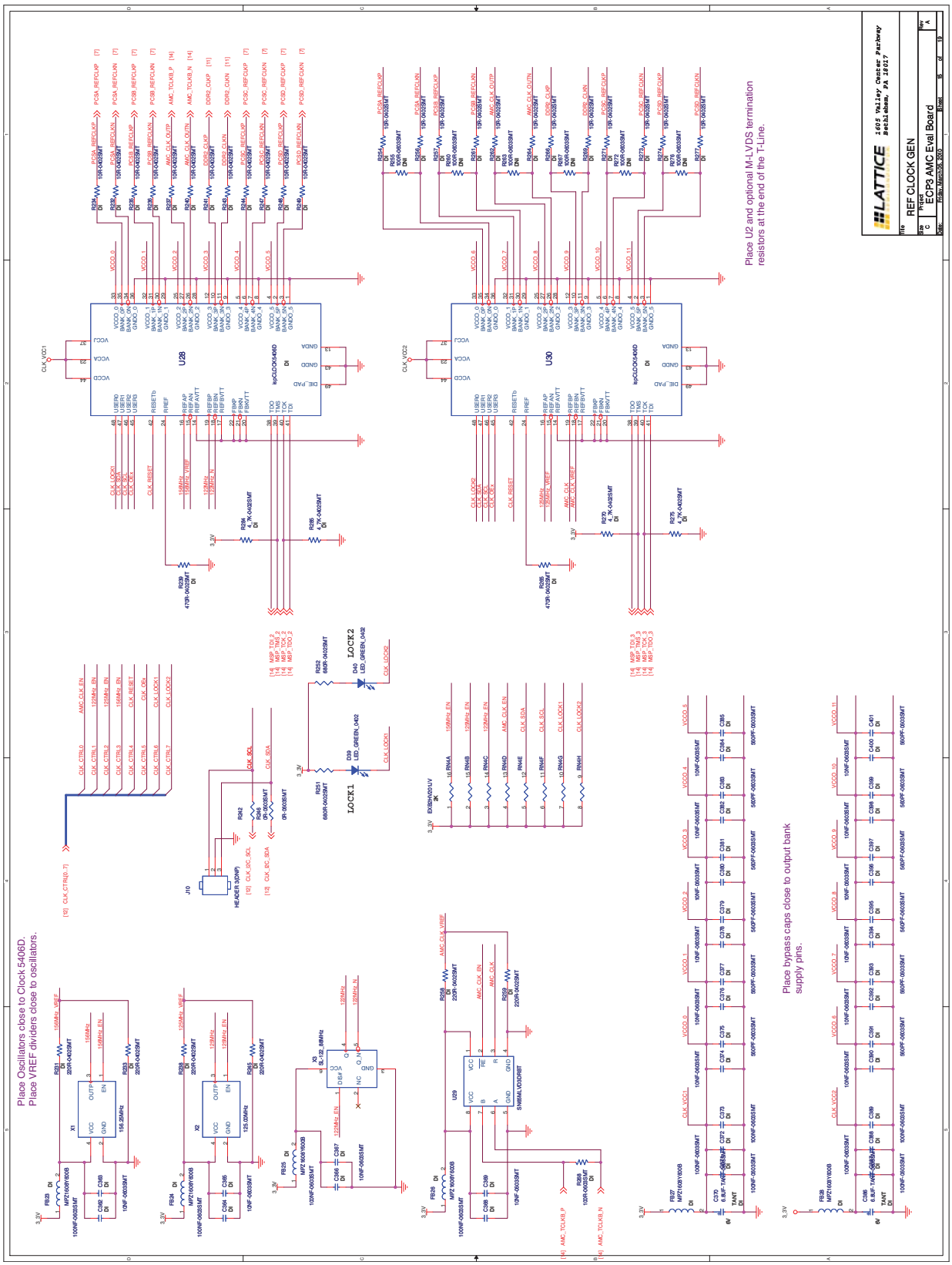


Figure 41. SFP Cage/Connector

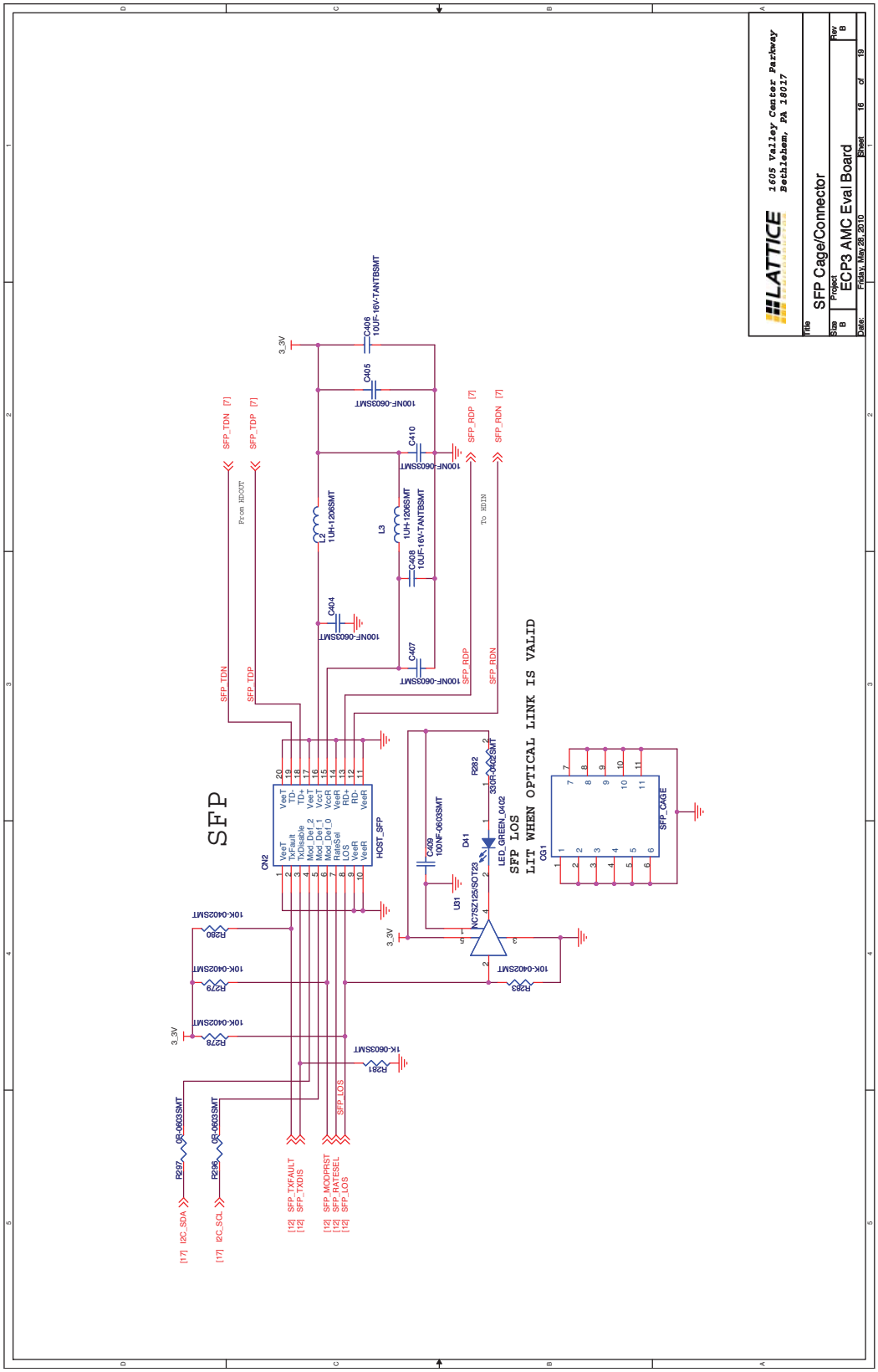


Figure 42. FMC Backplane

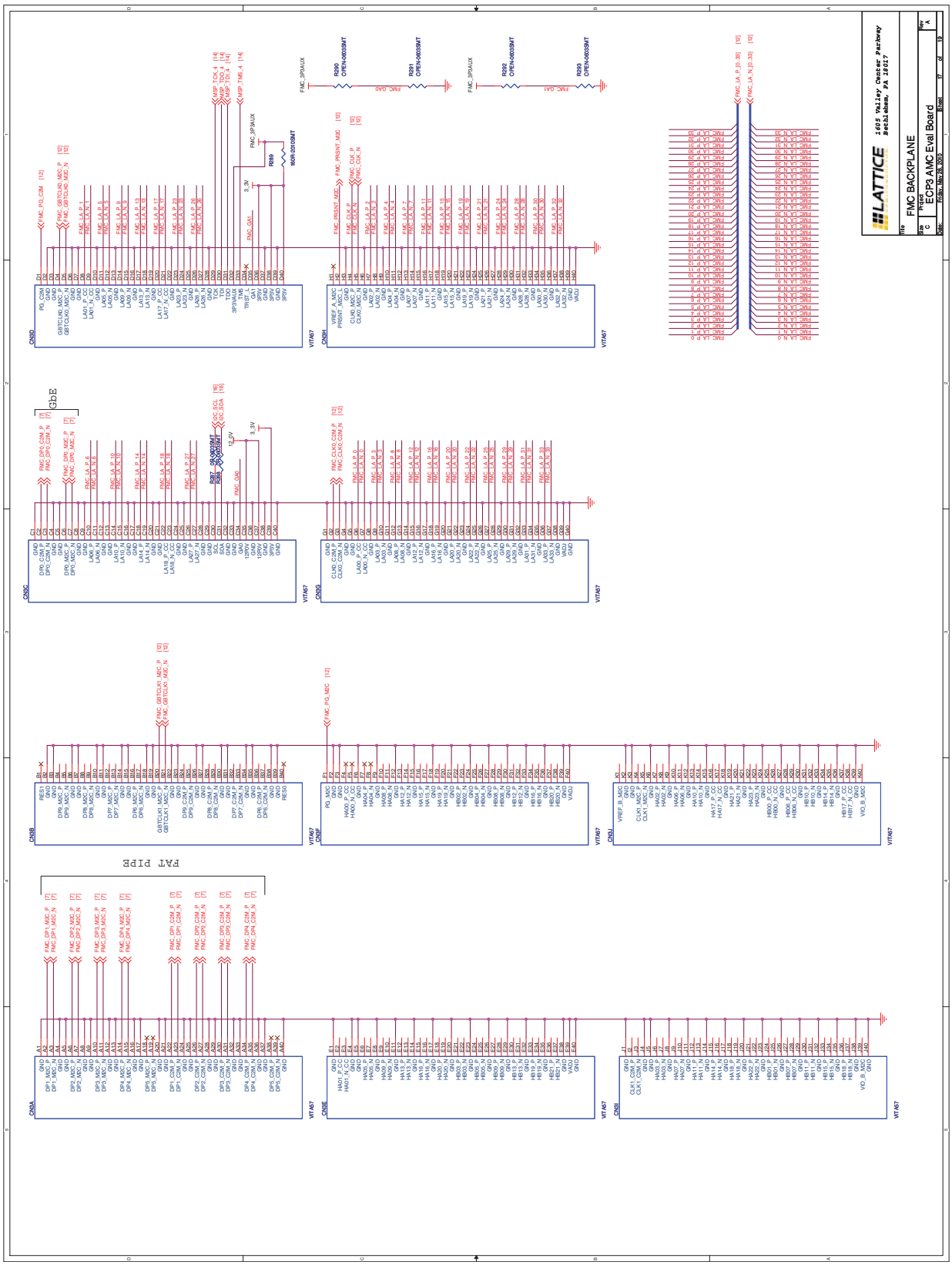


Figure 43. VSS/Decoupling

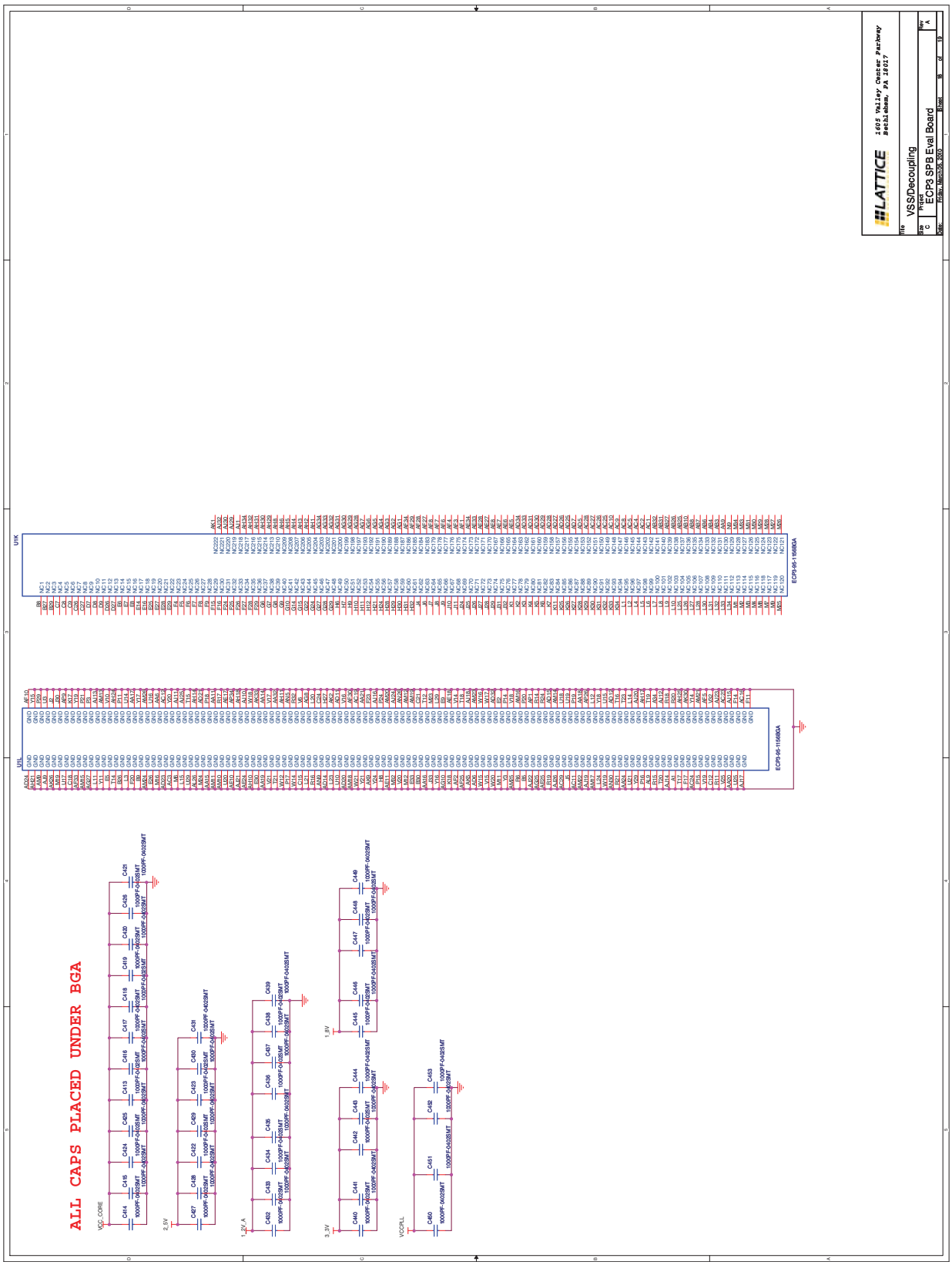
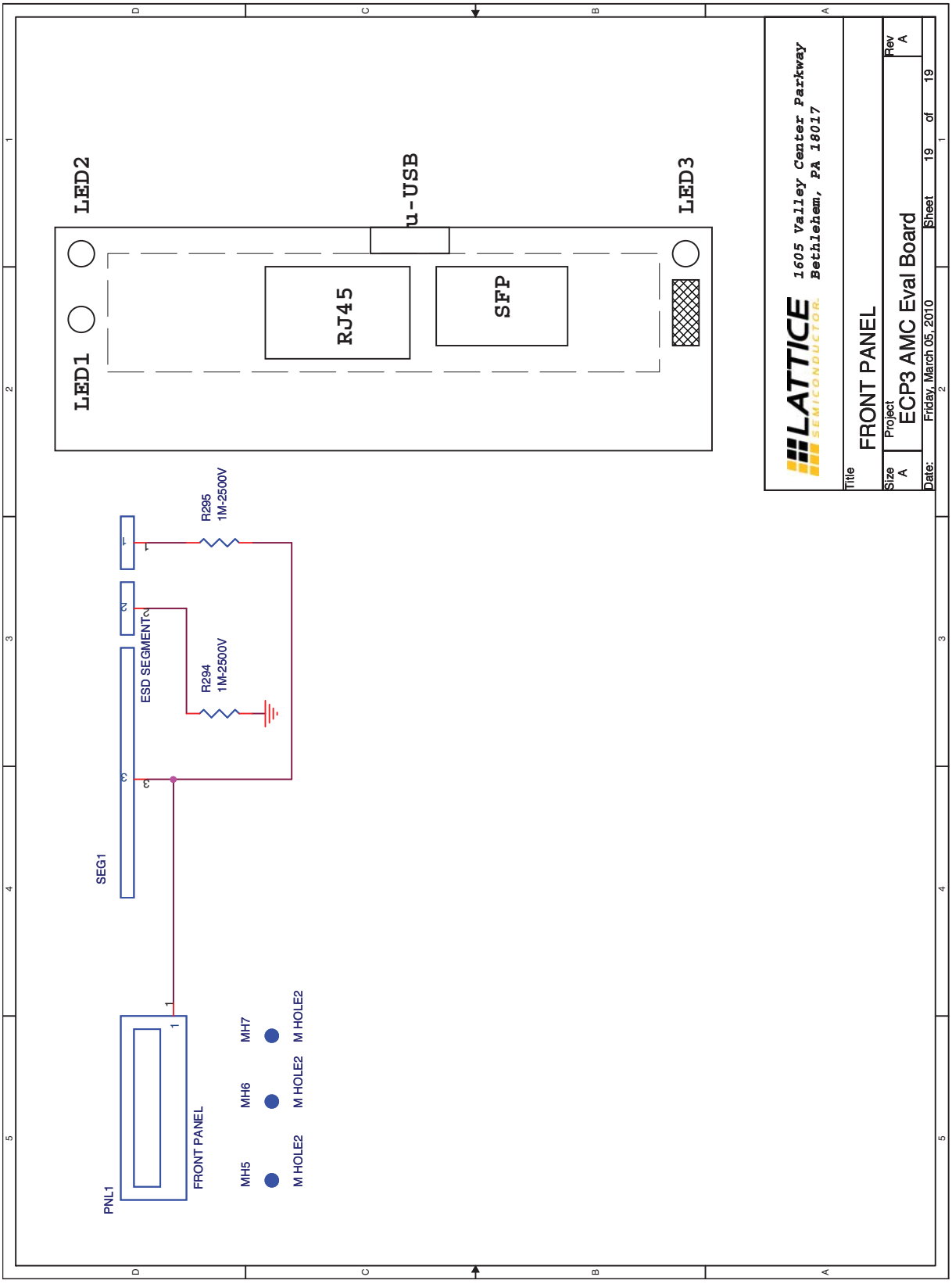


Figure 44. Front Panel



Appendix E. Lattice AMC Interface Card Schematic

Figure 45. Block Diagram

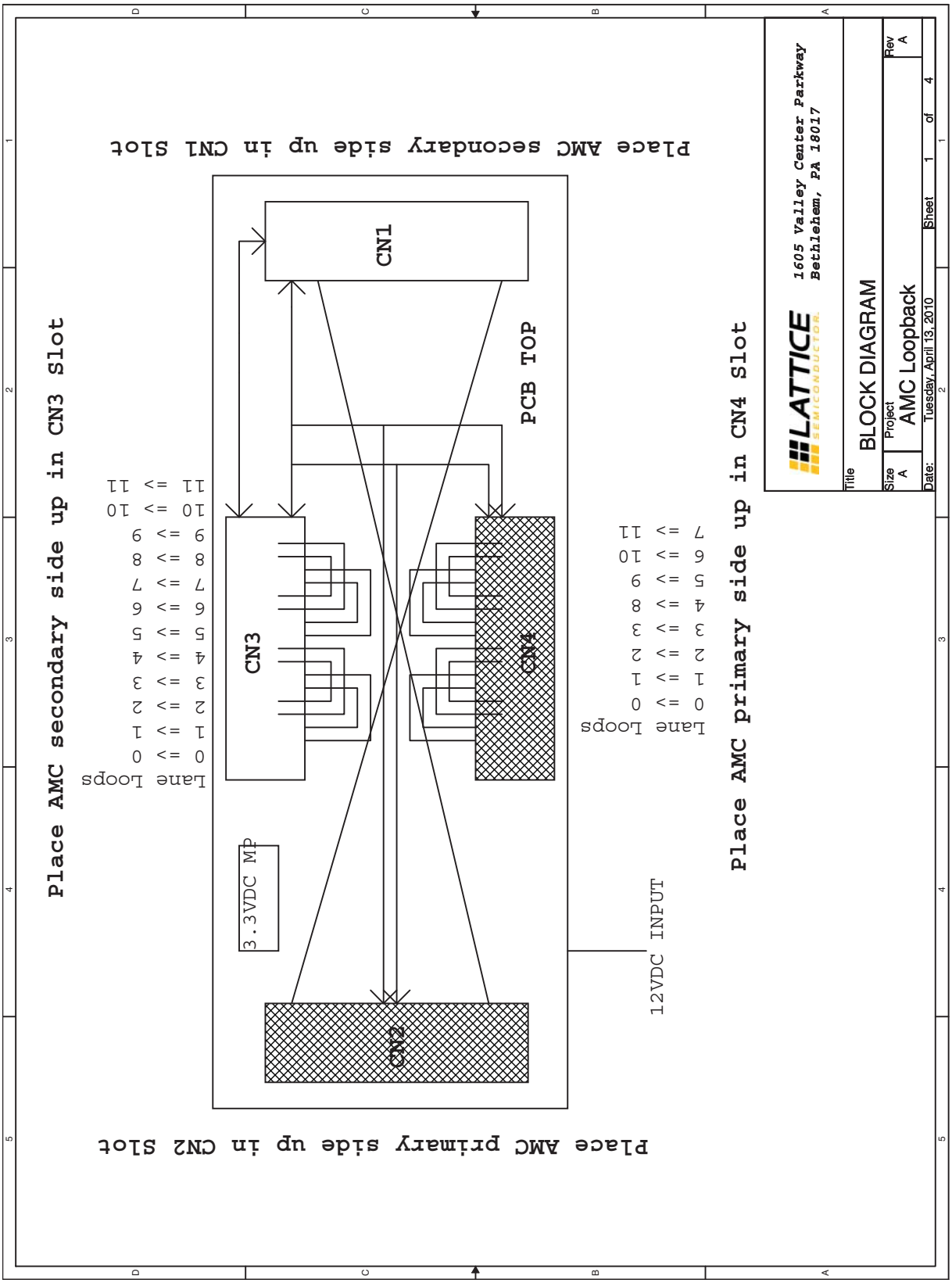


Figure 46. Power

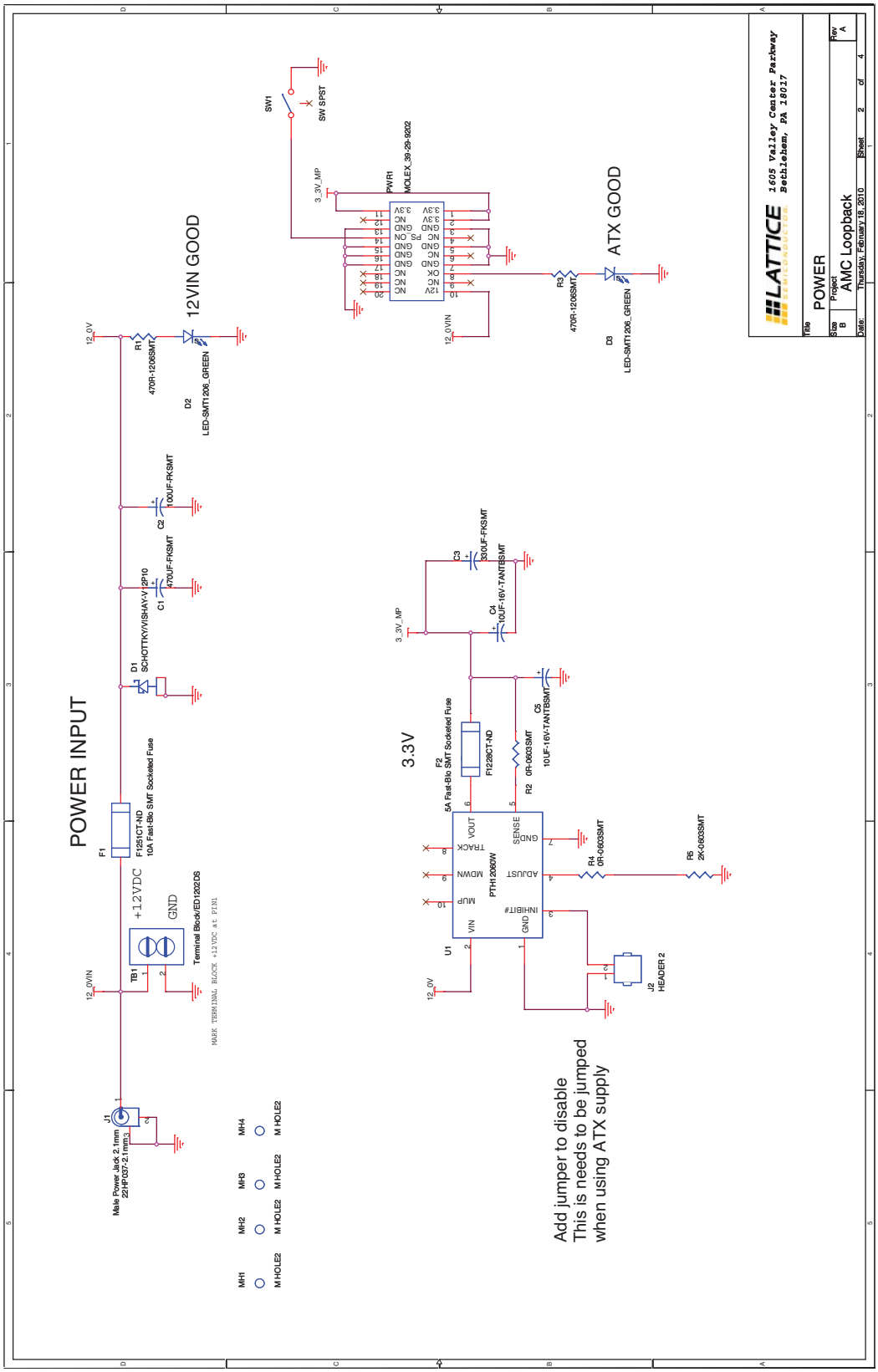


Figure 47. Board to Board

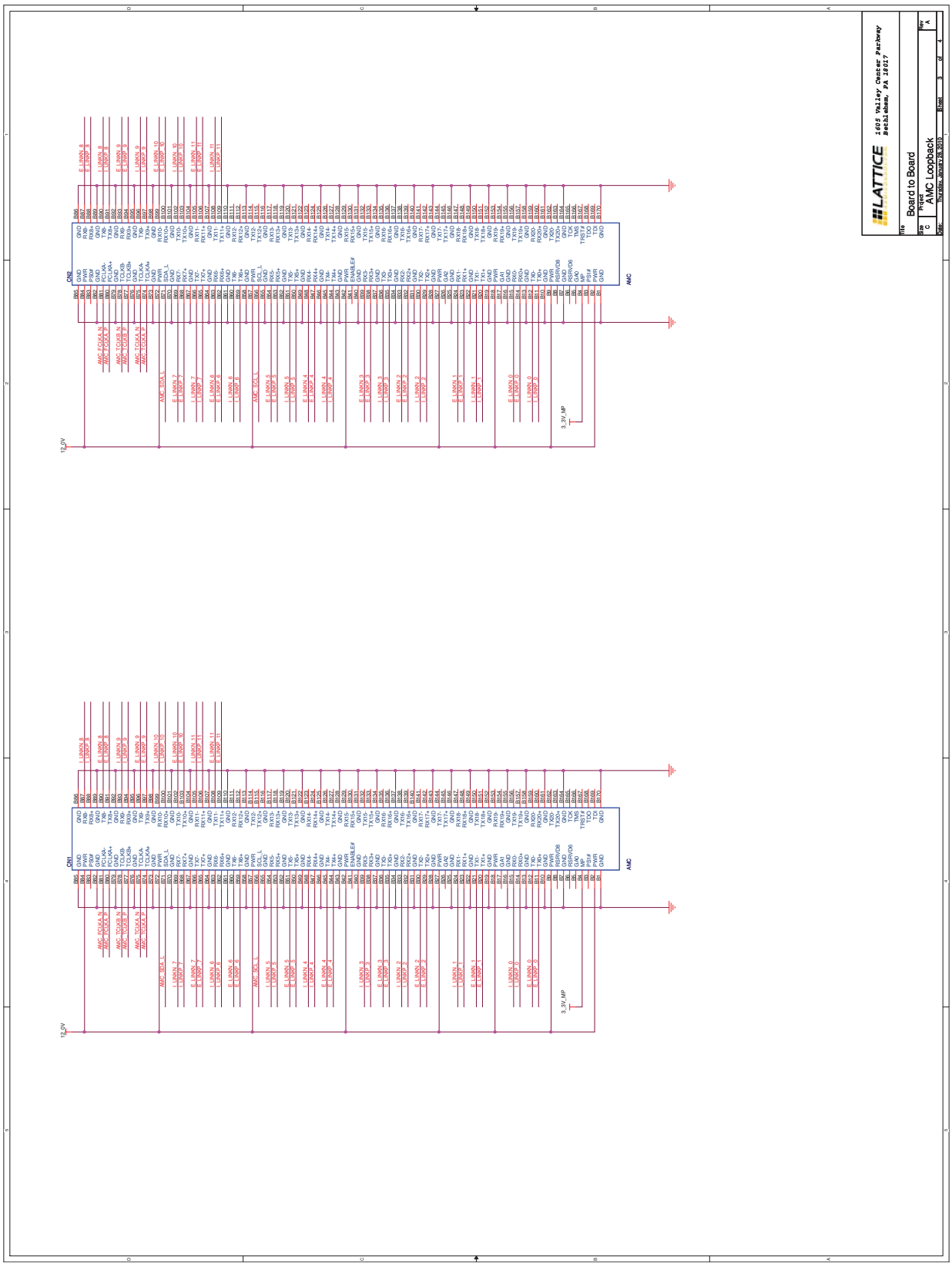
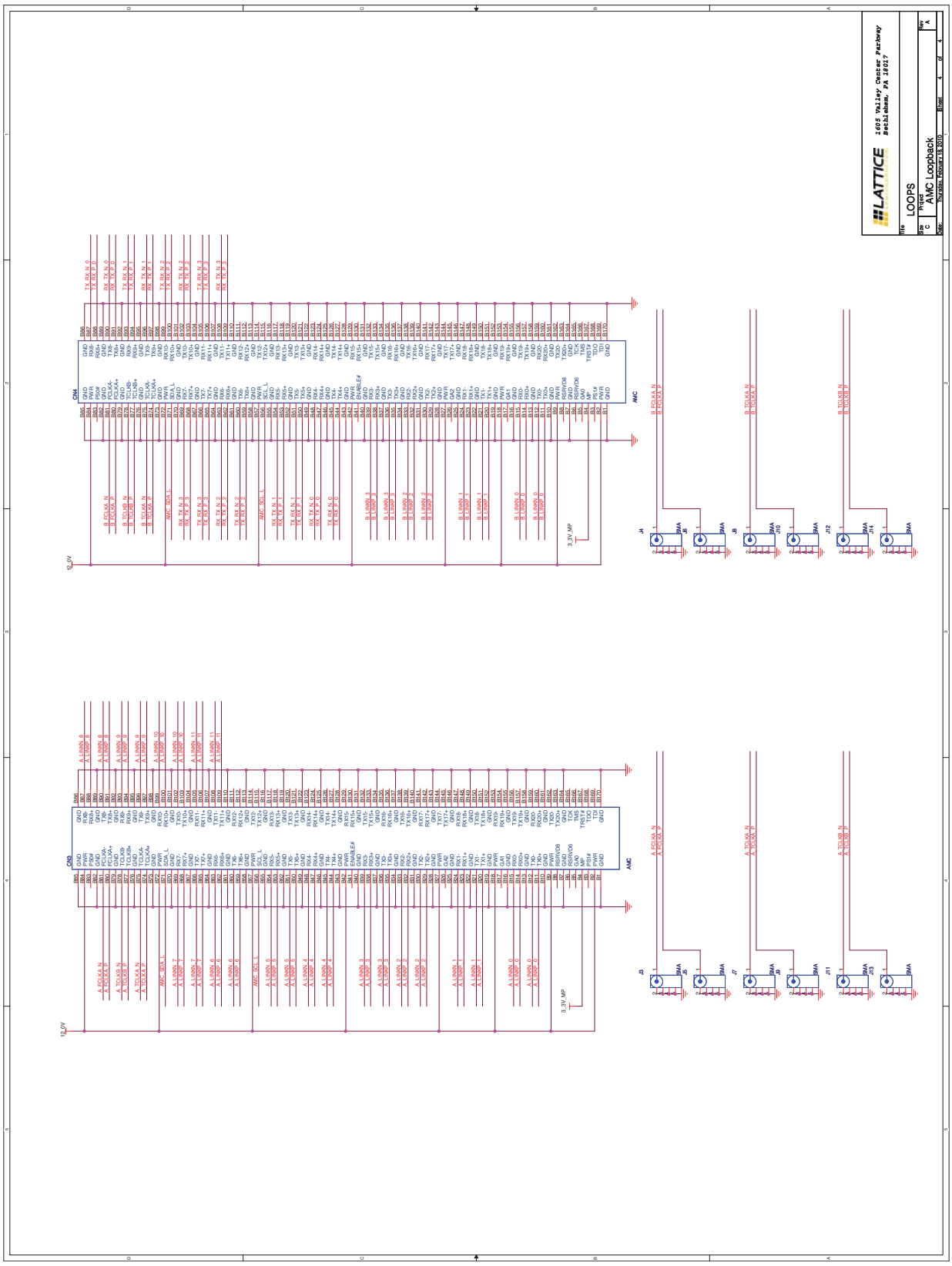


Figure 48. Loops



Appendix F. Example Preference File

```
BANK 0 VCCIO 3.3 V;
BANK 1 VCCIO 2.5 V;
BANK 2 VCCIO 3.3 V;
BANK 3 VCCIO 3.3 V;
BANK 6 VCCIO 1.8 V;
BANK 7 VCCIO 1.8 V;


# Clock Input
IOBUF PORT "clk_in" IO_TYPE=LVDS25 PCICLAMP=ON TERMINATEVTT=OFF DIFFRESISTOR=OFF ;
LOCATE COMP "clk_in" SITE "U6" ;

# RESETn
IOBUF PORT "reset_n" IO_TYPE=LVCMOS33 PCICLAMP=ON ;
LOCATE COMP "reset_n" SITE "AL27" ;

# Switches
IOBUF PORT "switch_0" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_1" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_2" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_3" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_4" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_5" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_6" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
IOBUF PORT "switch_7" IO_TYPE=LVCMOS25 PCICLAMP=ON ;
LOCATE COMP "switch_0" SITE "C25" ;
LOCATE COMP "switch_1" SITE "D25" ;
LOCATE COMP "switch_2" SITE "G26" ;
LOCATE COMP "switch_3" SITE "G25" ;
LOCATE COMP "switch_4" SITE "B28" ;
LOCATE COMP "switch_5" SITE "A28" ;
LOCATE COMP "switch_6" SITE "A26" ;
LOCATE COMP "switch_7" SITE "A27" ;

# LEDs
IOBUF PORT "oled_0" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_1" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_2" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_3" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_4" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_5" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_6" IO_TYPE=LVCMOS25 ;
IOBUF PORT "oled_7" IO_TYPE=LVCMOS25 ;
LOCATE COMP "oled_0" SITE "A29" ;
LOCATE COMP "oled_1" SITE "A30" ;
LOCATE COMP "oled_2" SITE "H26" ;
LOCATE COMP "oled_3" SITE "H25" ;
LOCATE COMP "oled_4" SITE "A31" ;
LOCATE COMP "oled_5" SITE "B31" ;
LOCATE COMP "oled_6" SITE "C29" ;
LOCATE COMP "oled_7" SITE "C30" ;
```

```
# Flash memory interface
LOCATE COMP "flash_a2" SITE "Y31" ;
LOCATE COMP "flash_a3" SITE "Y32" ;
LOCATE COMP "flash_a4" SITE "AA29" ;
LOCATE COMP "flash_a5" SITE "Y30" ;
LOCATE COMP "flash_a6" SITE "Y33" ;
LOCATE COMP "flash_a7" SITE "Y34" ;
LOCATE COMP "flash_a8" SITE "W26" ;
LOCATE COMP "flash_a9" SITE "W27" ;
LOCATE COMP "flash_a10" SITE "W29" ;
LOCATE COMP "flash_a11" SITE "W30" ;
LOCATE COMP "flash_a12" SITE "W28" ;
LOCATE COMP "flash_a13" SITE "V29" ;
LOCATE COMP "flash_a14" SITE "W31" ;
LOCATE COMP "flash_a15" SITE "W32" ;
LOCATE COMP "flash_a16" SITE "V26" ;
LOCATE COMP "flash_a17" SITE "V27" ;
LOCATE COMP "flash_a18" SITE "W33" ;
LOCATE COMP "flash_a19" SITE "W34" ;
LOCATE COMP "flash_a20" SITE "V28" ;
LOCATE COMP "flash_a21" SITE "U28" ;
LOCATE COMP "flash_a22" SITE "V30" ;


LOCATE COMP "flash_d0" SITE "N30";
LOCATE COMP "flash_d1" SITE "N29";
LOCATE COMP "flash_d2" SITE "N26";
LOCATE COMP "flash_d3" SITE "P26";
LOCATE COMP "flash_d4" SITE "AF31";
LOCATE COMP "flash_d5" SITE "AF32";
LOCATE COMP "flash_d6" SITE "AE29";
LOCATE COMP "flash_d7" SITE "AE30";
LOCATE COMP "flash_d8" SITE "AE31";
LOCATE COMP "flash_d9" SITE "AE32";
LOCATE COMP "flash_d10" SITE "N32";
LOCATE COMP "flash_d11" SITE "N31";
LOCATE COMP "flash_d12" SITE "N27";
LOCATE COMP "flash_d13" SITE "N28";
LOCATE COMP "flash_d14" SITE "AA27";
LOCATE COMP "flash_d15" SITE "AA28";
LOCATE COMP "flash_d16" SITE "AC33";
LOCATE COMP "flash_d17" SITE "AC34";
LOCATE COMP "flash_d18" SITE "AC30";
LOCATE COMP "flash_d19" SITE "AB30";
LOCATE COMP "flash_d20" SITE "AA30";
LOCATE COMP "flash_d21" SITE "AA31";
LOCATE COMP "flash_d22" SITE "AA26";
LOCATE COMP "flash_d23" SITE "AA25";
LOCATE COMP "flash_d24" SITE "AB33";
LOCATE COMP "flash_d25" SITE "AB34";
LOCATE COMP "flash_d26" SITE "N34";
LOCATE COMP "flash_d27" SITE "N33";
```

```
LOCATE COMP "flash_d28" SITE "P28";
LOCATE COMP "flash_d29" SITE "P27";
LOCATE COMP "flash_d30" SITE "Y25";
LOCATE COMP "flash_d31" SITE "Y26";
LOCATE COMP "flash_cem" SITE "AN34";
LOCATE COMP "flash_oe_n" SITE "AN33";
LOCATE COMP "flash_we_n" SITE "AH33";
LOCATE COMP "flash_byte_n" SITE "AJ33";
LOCATE COMP "flash_wp_n" SITE "AP33";
LOCATE COMP "flash_rst_n" SITE "AP32";
LOCATE COMP "flash_rdby_a" SITE "AL34";
LOCATE COMP "flash_rdby_b" SITE "AL33";

# I2C
LOCATE COMP "pwr_sda" SITE "A16";
LOCATE COMP "pwr_scl" SITE "L16";

LOCATE COMP "clk_sda" SITE "G18";
LOCATE COMP "clk_scl" SITE "B16";

LOCATE COMP "eeprom_sda" SITE "C17";
LOCATE COMP "eeprom" SITE "E19";



# 88E1111 PHY
LOCATE COMP "phy_mdio" SITE "J21";
LOCATE COMP "phy_mdc" SITE "H22";

LOCATE COMP "phy_resetn" SITE "A23";
LOCATE COMP "phy_int_n" SITE "B23";
LOCATE COMP "phy_freq_sel" SITE "E22";
LOCATE COMP "phy_clk25" SITE "E23";
LOCATE COMP "phy_125clk" SITE "C23";
LOCATE COMP "phy_crs" SITE "D23";
LOCATE COMP "phy_col" SITE "K22";



# DDR2 Memory Interface
IOBUF PORT "em_ddr_clk_0" IO_TYPE=SSTL18D_II ;
IOBUF PORT "em_ddr_clk_1" IO_TYPE=SSTL18D_II ;
IOBUF PORT "em_ddr_dqs_0" IO_TYPE=SSTL18D_II ;
IOBUF PORT "em_ddr_dqs_1" IO_TYPE=SSTL18D_II ;
IOBUF PORT "em_ddr_dqs_2" IO_TYPE=SSTL18D_II ;
IOBUF PORT "em_ddr_dqs_3" IO_TYPE=SSTL18D_II ;
IOBUF PORT "em_ddr_data_0" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_1" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_2" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_3" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_4" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_5" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_6" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_7" IO_TYPE=SSTL18_II ;
```

```
IOBUF PORT "em_ddr_data_8" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_9" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_10" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_11" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_12" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_13" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_14" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_15" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_16" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_17" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_18" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_19" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_20" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_21" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_22" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_23" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_24" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_25" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_26" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_27" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_28" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_29" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_30" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_data_31" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_ba_0" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_ba_1" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_cas_n" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_ras_n" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_dm_0" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_dm_1" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_dm_2" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_dm_3" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_odt" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_we_n" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_0" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_1" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_2" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_3" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_4" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_5" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_6" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_7" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_8" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_9" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_10" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_11" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_addr_12" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_cs_n_0" IO_TYPE=SSTL18_II ;
IOBUF PORT "em_ddr_cke_0" IO_TYPE=SSTL18_II ;

LOCATE COMP "em_ddr_data_0" SITE "W1" ;
LOCATE COMP "em_ddr_data_1" SITE "W8" ;
LOCATE COMP "em_ddr_data_2" SITE "W9" ;
LOCATE COMP "em_ddr_data_3" SITE "W4" ;
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LOCATE COMP "em_ddr_data_4" SITE "W3" ;
LOCATE COMP "em_ddr_data_5" SITE "Y2" ;
LOCATE COMP "em_ddr_data_6" SITE "Y1" ;
LOCATE COMP "em_ddr_data_7" SITE "Y8" ;
LOCATE COMP "em_ddr_data_8" SITE "AA1" ;
LOCATE COMP "em_ddr_data_9" SITE "Y7" ;
LOCATE COMP "em_ddr_data_10" SITE "AA7" ;
LOCATE COMP "em_ddr_data_11" SITE "AA4" ;
LOCATE COMP "em_ddr_data_12" SITE "AA3" ;
LOCATE COMP "em_ddr_data_13" SITE "AB2" ;
LOCATE COMP "em_ddr_data_14" SITE "AB1" ;
LOCATE COMP "em_ddr_data_15" SITE "AA5" ;

LOCATE COMP "em_ddr_data_16" SITE "AN1" ;
LOCATE COMP "em_ddr_data_17" SITE "AN2" ;
LOCATE COMP "em_ddr_data_18" SITE "AD9" ;
LOCATE COMP "em_ddr_data_19" SITE "AD8" ;
LOCATE COMP "em_ddr_data_20" SITE "AP2" ;
LOCATE COMP "em_ddr_data_21" SITE "AP3" ;
LOCATE COMP "em_ddr_data_22" SITE "AL3" ;
LOCATE COMP "em_ddr_data_23" SITE "AK3" ;
LOCATE COMP "em_ddr_data_24" SITE "AN3" ;
LOCATE COMP "em_ddr_data_25" SITE "AM3" ;
LOCATE COMP "em_ddr_data_26" SITE "AJ5" ;
LOCATE COMP "em_ddr_data_27" SITE "AJ6" ;
LOCATE COMP "em_ddr_data_28" SITE "AL5" ;
LOCATE COMP "em_ddr_data_29" SITE "AM5" ;
LOCATE COMP "em_ddr_data_30" SITE "AL4" ;
LOCATE COMP "em_ddr_data_31" SITE "AM4" ;
LOCATE COMP "em_ddr_dqs_0" SITE "W6" ;
LOCATE COMP "em_ddr_dqs_1" SITE "AA10" ;
LOCATE COMP "em_ddr_dqs_2" SITE "AJ2" ;
LOCATE COMP "em_ddr_dqs_3" SITE "AM6" ;
LOCATE COMP "em_ddr_dm_0" SITE "W2" ;
LOCATE COMP "em_ddr_dm_1" SITE "AA2" ;
LOCATE COMP "em_ddr_dm_2" SITE "AJ4" ;
LOCATE COMP "em_ddr_dm_3" SITE "AP5" ;
LOCATE COMP "em_ddr_ba_0" SITE "T6" ;
LOCATE COMP "em_ddr_ba_1" SITE "T5" ;
LOCATE COMP "em_ddr_cas_n" SITE "T7" ;
LOCATE COMP "em_ddr_ras_n" SITE "R8" ;
LOCATE COMP "em_ddr_addr_0" SITE "R4" ;
LOCATE COMP "em_ddr_addr_1" SITE "R1" ;
LOCATE COMP "em_ddr_addr_2" SITE "R2" ;
LOCATE COMP "em_ddr_addr_3" SITE "P10" ;
LOCATE COMP "em_ddr_addr_4" SITE "P9" ;
LOCATE COMP "em_ddr_addr_5" SITE "R5" ;
LOCATE COMP "em_ddr_addr_6" SITE "R7" ;
LOCATE COMP "em_ddr_addr_7" SITE "P8" ;
LOCATE COMP "em_ddr_addr_8" SITE "N8" ;
LOCATE COMP "em_ddr_addr_9" SITE "P4" ;
LOCATE COMP "em_ddr_addr_10" SITE "P5" ;
LOCATE COMP "em_ddr_addr_11" SITE "N1" ;
LOCATE COMP "em_ddr_addr_12" SITE "N2" ;
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LOCATE COMP "em_ddr_cs_n_0" SITE "T3" ;
LOCATE COMP "em_ddr_odt" SITE "R3" ;
LOCATE COMP "em_ddr_we_n" SITE "T4" ;
LOCATE COMP "em_ddr_clk_0" SITE "T2" ;
LOCATE COMP "em_ddr_clk_1" SITE "AD4" ;
LOCATE COMP "em_ddr_cke_0" SITE "U9" ;

#150K Locates for ddr on amc board
LOCATE PGROUP
"ddr2_test_core/u_ddr_sdram_mem_top/U1_ddr_sdram_mem_core/U1_LSC_IP_ddr_core/genblk0
_u_0__dv_mod/u1_pio_read_macro/DQS_PIO_READ" SITE "R76C2D" ;
LOCATE PGROUP
"ddr2_test_core/u_ddr_sdram_mem_top/U1_ddr_sdram_mem_core/U1_LSC_IP_ddr_core/genblk0
_u_1__dv_mod/u1_pio_read_macro/DQS_PIO_READ" SITE "R85C2D" ;
#150K_LOCATE PGROUP
"ddr2_test_core/u_ddr_sdram_mem_top/U1_ddr_sdram_mem_core/U1_LSC_IP_ddr_core/genblk0
_u_2__dv_mod/u1_pio_read_macro/DQS_PIO_READ" SITE "R112C2D" ;
LOCATE PGROUP
"ddr2_test_core/u_ddr_sdram_mem_top/U1_ddr_sdram_mem_core/U1_LSC_IP_ddr_core/genblk0
_u_3__dv_mod/u1_pio_read_macro/DQS_PIO_READ" SITE "R121C2D" ;
LOCATE PGROUP "ddr2_test_core/DDR2_CORE_GROUP" SITE "R60C2D" ;
BLOCK JTAGPATHS ;
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