DDR3 Demo for the LatticeECP3 I/O Protocol Board

User's Guide

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UG38_01.4

Introduction

This document provides technical information and instructions on using the LatticeECP3™ DDR3 demo design. This demo demonstrates the functionality of the Lattice DDR3 IP core at a speed of 400 MHz and 800 Mbps using the LatticeECP3 I/O Protocol Board. The document provides a circuit description of the demo logic as well as instructions for running the DDR3 demo.

The demo package includes the following:

- DDR3 IP core configuration files (.lpc)
- Verilog source code for the demo logic design
- Lattice Diamond® implementation project files (.ldf/.syn) along with the preference files (.lpf) for the demo project
- Aldec® Active-HDL™ and Mentor Graphics® ModelSim® simulation scripts (.do) and Verilog test bench
- 64-bit DDR3 demo bitstream file (.bit)

Demo design hardware requirements:

- LatticeECP3 I/O Protocol Board Revision C with a LatticeECP3-150EA FPGA, 1156-ball fpBGA package
- 12V DC power supply for LatticeECP3 I/O Protocol Board
- 240-pin single or dual rank unbuffered DDR3 UDIMM with 1.5V, 800/1066/1333 speed bin
- Windows PC or Linux machine for implementing the demo project and downloading the bitstream
- Optional external clock generator to run the demo at different clock rates
- JTAG download cable

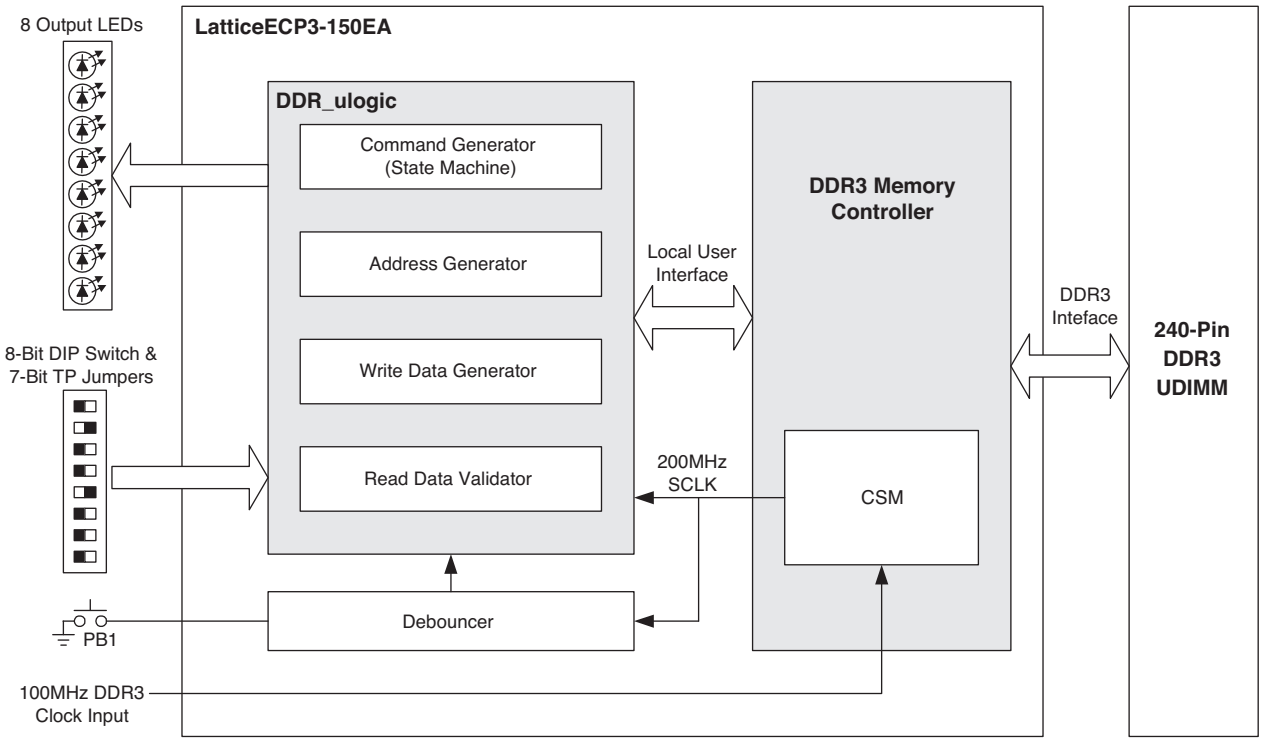
Demo design software requirements:

- Diamond 1.3 (or later)

DDR3 Demo Design Overview

The DDR3 demo design consists of two major parts: a DDR3 controller IP core and the user logic block. The latter includes a function block that exercises and analyzes the DDR3 data stream. Figure 1 illustrates a block diagram of the demo design.

Figure 1. DDR3 Demo Design Block Diagram



DDR3 IP Core

The demo has been designed to support the parameterized DDR3 data bus widths (8-, 16-, 32-, and 64-bit configurations). The user logic is also parameterized by the core parameter file. Once a DDR3 core is generated with a supported data width, the whole demo design can be simulated and implemented without modifying the code. A DDR3 IP core configuration file for the 64-bit data width is provided in the demo package. If a different configuration is to be used, the following conditions need to be met:

- DDR3 data width is 8, 16, 32, or 64 bits supporting both single- and dual-rank configurations
- Select the default DDR3 memory device and keep the default DDR3 timing parameters (If a UDIMM module with a different specification is to be used, make the necessary updates in the DDR3 timing parameters to match them with the timing parameters of the UDIMM to be used)
- Keep all other core options unchanged

User Logic

The user logic implemented in the DDR3 demo design provides the following functions:

- State machine programs the mode registers and controls DDR3 read and write operations
- Address generation
- Write data generation
- Read data validation
- Control and observation

Demo Control State Machine

The state machine controls the demo using the user control input through an 8-bit DIP switch. Once the LatticeECP3 device is programmed or a system reset is applied (the GSR button is pressed), the state machine will be in the idle state waiting for the push button input on PB1. When PB1 is pressed, the state machine programs all DDR3 mode registers (MR0~MR3) based on the user test configuration (DIP switch setting). Then, it generates a write command sequence. The write command can be repeated up to 32 times using either the command burst feature of the core or multiples of single write commands depending on the user setting. After the write command sequence, a read command sequence is initiated. The read command sequence can also be repeated up to 32 times in the same way as the write command sequence. The read command sequence that follows the write command sequence must include the same number of commands as the as the write command sequence. The state machine makes sure that both the write and the following read command sequences are always the same even when the user test configuration is changed at any time during the command sequences. This allows the DDR3 demo to be dynamically reconfigurable.

Address Generation

The address generation block provides the start address for the current user read/write command which is generated by the state machine. When the burst command mode is enabled, the address generation block automatically calculates the next address according to the demo control input.

Write Data Generation

The demo uses both PRBS and sequential data patterns. When PRBS is selected, either a 128-bit or 32-bit PRBS pattern generator is implemented to the local write data bus to generate an 8-to-64-bit DDR3 data pattern. For 64-bit DDR3 data, an identical 128-bit PRBS pattern is allocated to both the upper and lower halves of the local data bus. For the sequential data pattern, the demo design uses only a 32-bit sequential data pattern generator to provide 8-to-64-bit DDR3 data. This 32-bit data pattern is allocated to each 32-bit wide local data bus slot. For example, a 64-bit DDR3 bus requires a 256-bit local data bus which has eight identically sequenced 32-bit patterns allocated on eight 32-bit slots. The write data generation is enabled and driven by the datain_rdy signal assertions.

Read Data Validation

The read data checker validates the read data from the DDR3 memory module. To do this, it generates the expected data patterns using exactly the same data sequences as the Write Data Generator block. The expected data generation is enabled and driven by the read_data_valid signal assertions. The read data captured by read_data_valid is compared with the expected data generated from the Expected Data Generator block. As soon as both data patterns mismatch each other, the demo design will flag the error detection signal.

Control and Observation

The Control and Observation block includes the demo control input and result display functions. The demo control input uses an 8-bit DIP switch available on the LatticeECP3 I/O Protocol Board. The demo result is displayed through the eight LEDs on the board. See the following section for descriptions of the demo control input switches and the result display LEDs.

LatticeECP3 I/O Protocol Board Setup for Demo

This section describes the setup requirements for the DDR3 demo using the LatticeECP3 I/O Protocol Board.

DDR3 Memory

The LatticeECP3 I/O Protocol Board has two sockets that can accommodate two DDR3 memory modules. Only one memory module is supported by the demo and the DDR3 IP core.

Module Selection

The DDR3 memory module used for the DDR3 demo on the LatticeECP3 I/O Protocol Board is a 240-pin unbuffered DDR3 DIMM (UDIMM). The demo design uses up to 2GB of memory space with a single-rank configuration or 4GB with a dual-rank configuration. A smaller size UDIMM is also allowed for the demo. The bistream that is included in the package is for a single-rank configuration. Therefore, it is recommended that a 1GB or 2GB single-rank 240-pin DDR3 UDIMM be used for the demo. A dual rank 2GB or 4GB UDIMM (2GB per rank) will work as

well because only the first rank will be accessed. The following DDR3 module specification is required to be selected as a valid memory module for the demo:

- Vdd = 1.5V
- Data Rate: 800 (PC3-6400), 1066 (PC3-8500) or 1333 (PC3-10600)
  Note: Faster data rate UDIMMs may work but have not been tested.

Installation

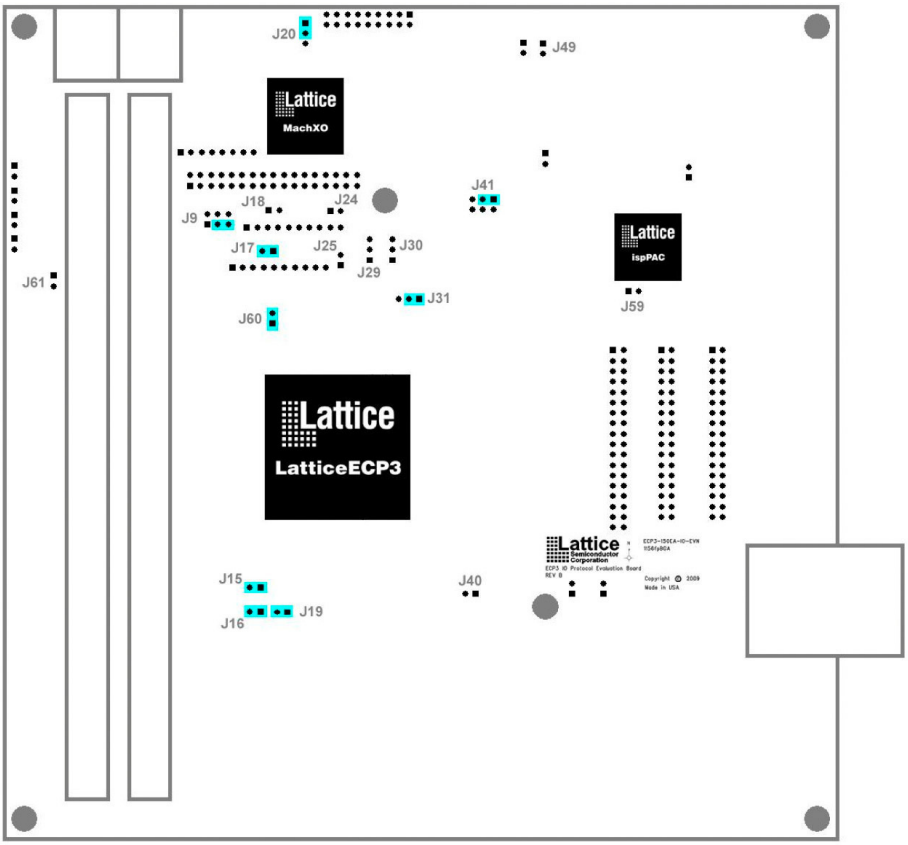
The DDR3 demo design supports one UDIMM with a single rank. The DDR3 socket located on the left-most side of the LatticeECP3 I/O Protocol Board is the one to be used for the demo. It is marked as DIMM1 on the board. The DDR3 socket marked as DIMM2 is not used for the demo. Proper installation of the selected module is important for a successful demo. It is difficult to distinguish a DDR3 DIMM module from a DDR2 DIMM module by visual inspection. Inserting a module other than a DDR3 DIMM into a DDR3 socket may damage the module or the socket. If you are not sure that the module you have is a DDR3 DIMM, visually check whether the module key aligns exactly with the socket key. Try turning over the memory module if the memory module direction misaligns with the socket key. If the key does not align in both ways, the DIMM you are trying to install is not a DDR3 DIMM. When a single-sided DDR3 DIMM is installed (usually single rank), the DDR3 components are shown on the right side of the installed module.

Board Connections

Jumpers

The jumpers on the LatticeECP3 I/O Protocol Board should be installed with the default settings, as shown in Figure 2.

Figure 2. LatticeECP3 I/O Protocol Board Default Jumper Settings



Programming Cable Connections

The LatticeECP3 device on the LatticeECP3 I/O Protocol Board can be programmed via the USB port, JTAG download port or through the SPI Flash interface. If the JTAG port is used, it can both program the device and use the Reveal™ logic analyzer when internal signal paths are to be traced. The J10 connector, located between J17 and J60 in Figure 2, is used for the JTAG downloading.

External Clock Input

The DDR3 demo can use either the on-board oscillator clock or an external clock input. Clock selection is dynamically controlled by a DIP switch setting. See the Control and Observation Ports section of this document for further details. Since the DDR3 demo uses a SSTL15D type clock, a 1.5V differential clock input is to be connected to the clock connectors on the LatticeECP3 I/O Protocol Board, which is marked as EXT CLK (J33, J36). If an external differential clock is not available, a single-ended clock may also be used through a connection with J33.

Port Assignments and Descriptions

Table 1. DDR3 Bus Interface

Port Name	Active	Direction	Description
em_ddr_reset_n	Low	Output	Asynchronous reset signal from the controller to the memory device. Asserted by the controller for the duration of power on reset or GSR_N.
em_ddr_clk[CLKO_WIDTH-1:0]	N/A	Output	400 MHz memory clock generated by the controller.
em_ ddr_clk_n[CLKO_WIDTH-1:0]	N/A	Output	400 MHz complimentary memory clock generated by the controller.
em_ ddr_cke[CKE_WIDTH-1:0]	High	Output	Memory clock enable generated by the controller.
em_ ddr_addr[ROW_WIDTH-1:0]	N/A	Output	Memory address bus, multiplexed row and column address for the memory.
em_ ddr_ba[2:0]	N/A	Output	Memory bank address.
em_ ddr_data[DATA_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data bus.
em_ ddr_dm[(DATA_WIDTH/8)-1:0]	High	Output	DDR3 memory write data mask.
em_ ddr_dqs[DQS_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data strobe.
em_ ddr_dqs_n[DQS_WIDTH-1:0]	N/A	In/Out	Memory complementary bi-directional data strobe
em_ ddr_cs_n[CS_WIDTH-1:0]	Low	Output	Memory chip select.
em_ ddr_cas_n	Low	Output	Memory column address strobe.
em_ ddr_ras_n	Low	Output	Memory row address strobe.
em_ ddr_we_n	Low	Output	Memory write enable.
em_ ddr_odt[CS_WIDTH-1:0]	High	Output	Memory on-die termination control.

Table 2. Demo User Interface Ports

Port Name	Active	Direction	Description
Clk_in	N/A	Input	Reference clock connected to a dedicated PLL clock input (U6) of the LatticeECP3-150EA FPGA.
Reset_n	Low	Input	Asynchronous reset connected to the GSRN button (D33). This resets the entire demo system including the DDR3 IP core when asserted.
Pb1	Low	Input	Push-button switch connected to the PB1 button switch (AM34). It is used to start the DDR3 demo transactions after a system reset.
ClkSel	N/A	Output	Clock selector connected to a clock mux that provides a DDR3 reference clock source. Clock selection is controlled by a DIP switch.
Dip_sw[7:0]	N/A	Input	User test configuration input. See the Control and Observation Port Description section of this document for further information.
TP[6:0]	N/A	Input	Additional test configuration input. See the Control and Observation Port Description section of this document for further information.
Oled[7:0]	N/A	Output	Demo result LED indicator output. See the Control and Observation Port Description section of this document for further information.

Control and Observation Port Descriptions

Table 3. DIP Switch Definitions

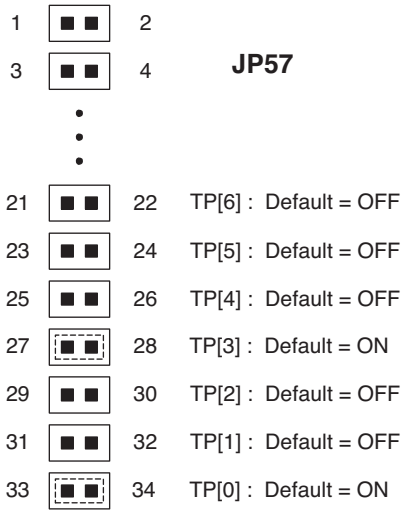
Signal Name	DIP Switch Number	Assigned Function Control	Setting	Description
dip_sw[0]	8	Burst Length Selection	Up	Set Burst Length to BL8.
			Down	Set Burst Length to BC4.
dip_sw[1]	7	On-the-Fly (OTF) Mode. Works with Burst Length Selection.	Up	Fixed burst size mode. The core is set to BL8 or BC4 during initialization depending on the Burst Length Selection setting.
			Down	OTF mode. Dynamic burst length change is controlled by the Burst Length Selection switch.
dip_sw[2]	6	Command Burst Enable. The core repeats a user R/W command as many times as specified by the Maximum Command Size setting.	Up	Enable command burst mode. 32-command burst when Maximum Command Size = 1. User-selectable burst size when Maximum Command Size = 0.
			Down	Disable command burst mode. Demo works in the single command mode, and manual single command repetitions are performed instead of using the command burst mode. The single command repetition is also controlled by the Maximum Command Size setting.
dip_sw[3]	5	Maximum Command Size	Up	Use maximum command burst size/repetition. When the command burst mode is enabled, the DDR3 core performs a 32-command burst on a user read or write command. When disabled, the maximum single command repetition is defined to 32 times. The demo back-end logic generates consecutive 32 single read or write commands.
			Down	Use user command burst size. Both the command burst and single command repetition modes use the burst size value (UsrCmdBrstCnt) defined in the ddr3_test_params.v file. The allowed values are 2, 4, 8, 16 or 32 with the default value set to 2. Note that 1 can be used only when OTF is disabled because dynamic OTF change from BC4 to BL8 may result in read data corruption due to the limitation of addressing.

Signal Name	DIP Switch Number	Assigned Function Control	Setting	Description
dip_sw[4]	4	Clock Selection	Up	Use the on-board 100MHz oscillator.
			Down	Use an external clock generator. The EXT CLK input connectors (SMAs J33 and J36) are used to feed the DDR3 reference clock.
dip_sw[5]	3	Data Mode	Up	PRBS data patterns are used for the DDR3 demo. 128-bit pseudo random patterns are generated. For 64-bit DDR3, two 128-bit PRBS patterns are used for a 256-bit local data bus.
			Down	Sequential data patterns. 32-bit sequential data pattern generators are used. For example, a 32-bit DDR3 demo will have four 32-bit sequential patterns allocated to each 32-bit slot on a local data bus.
dip_sw[6]	2	Test Mode	Up	Continuous write-then-read transactions. The DDR3 demo runs without pause until a system reset is applied.
			Down	Single read/write command with a push-button input (PB1). The first press of the push-button sends a single write command. The following press will provide a read command and then write again and so on. This mode is useful for debugging activities with lab equipment like oscilloscopes.
dip_sw[7]	1	Default Demo Setting.	Up	The optimized default setting is applied to the demo regardless of TP jumper settings.
			Down	Allow users to change the Read Pulse Tap and ODT configurations using the TP jumper settings. The “Default_Off” LED is turned on when the setting becomes different from the default. This LED warns the user about applying non-default values. See TP jumper setting.

TP Jumpers

TP jumper settings are effective only when the Default Demo Setting switch is disabled (dip_sw[7]=DOWN). The TP jumpers are assigned to the bottom side of J57 as illustrated in Figure 3.

Figure 3. TP Jumper Assignments



TP[0] is located to the bottom-most jumper of J57 (pins 33 and 34), TP[1] is on the next jumper, and so on. LED[5] is turned on when any of default settings is changed to provide a warning.

Table 4. TP Jumper Definitions

Name	Function	Value	Description
TP[1:0]	DDR3 Memory ODT TP[1] = MR1[6] TP[0] = MR1[2]	OFF / OFF	ODT disabled
		OFF / ON	60 ohm (RZQ/4), default setting.
		ON / OFF	120 ohm (RZQ/2)
		ON / ON	40 ohm (RZQ/6)
TP[4:2]	Read Pulse Tap	OFF / OFF / OFF	Read Pulse Tap = 0
		OFF / OFF / ON	Read Pulse Tap = 1
		OFF / ON / OFF	Read Pulse Tap = 2, default setting.
		OFF / ON / ON	Read Pulse Tap = 3
		ON / OFF / OFF	Read Pulse Tap = 4
		ON / OFF / ON	Read Pulse Tap = 5
		ON / ON / OFF	Read Pulse Tap = 6
		ON / ON / ON	Read Pulse Tap = 7
TP[5]	Rank Select. Ignored if TP[6]=OFF	OFF	Access Rank0 only, default setting
		ON	Access Rank1 only.
TP[6]	Rank Test Enable	OFF	Full range access, default setting.
		ON	Single rank test mode. This is a useful feature to check if the address mirroring option is correctly selected for the target DIMM memory.

Output LEDs

Eight LEDs are used to indicate the demo progress and results. The numbering of the LEDs starts from the right (LED[0]) to the left (LED[7]). The Assigned column shows the LatticeECP3 ball numbers printed on the LatticeECP3 I/O Protocol Board.

Table 5. Output LED Definitions

Name	Assigned	Function	Active	Description
OLED[0]	C3	Heartbeat indicator	Blink	This LED indicates that the board is alive, and the core is receiving the clock input.
OLED[1]	C4	Init-done and core ready indicator	ON	This LED indicates that the core and memory initialization is complete, and the core is ready to accept user commands.
OLED[2]	D3	Write indicator	ON	This LED indicates that the core's write operation is properly working by detecting the datain_rdy signal assertions.
OLED[3]	C2	Read indicator	ON	This LED indicates that the core's read operation is properly working by detecting the read_data_valid signal assertions.
OLED[4]	B1	DDR3 transaction indicator	Blink	This LED indicates that DDR3 Write-then-Read operations are going on. The more read data that comes in, the faster this LED blinks.
OLED[5]	B2	Off-Default indicator	ON	If turned ON, this warning LED indicates that the TP jumper setting is not the default.
OLED[6]	E4	Valid data indicator	Blink	This LED confirms that proper DDR3 read/write transactions are being performed with actual valid data. If the received data is null (all "0" or all "1") this LED will not blink.
OLED[7]	D4	Error indicator	Blink	This LED will start blinking when the first data mismatch error is detected. A system reset must be applied to clear this indicator.

In a normal, error-free operation, it is expected that the output LEDs will show the following status.

Table 6. Expected LED Status from Successful Demo

Name	Expected Status	Remark
OLED[0]	Blink	Blue LED with constant blinking rate.
OLED[1]	ON	Green LED.
OLED[2]	ON	Yellow LED.
OLED[3]	ON	Red LED.
OLED[4]	Blink	Blue LED. Blinking rate changes according to the data rate.
OLED[5]	OFF	Green LED.
OLED[6]	Blink	Yellow LED. Blinking rate changes according to the data rate.
OLED[7]	OFF	Red LED. Begins blinking if a data mismatch error is detected.

Demo Package Directory Structure

The directory structure of DDR3 demo package is shown in Figure 4. The demo package includes three top-level folders: the core folder, resource folder and user_logic folder.

Core Folder

The core folder includes a DDR3 IP core configuration file (ddr3core.lpc). A complete DDR3 IP core can be regenerated using this file through the IPexpress™ tool.

Resource Folder

The resource folder includes the following subfolders:

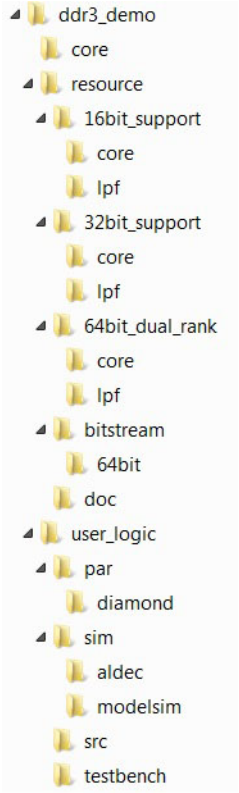
- **16bit_support** – This folder contains a 16-bit DDR3 core configuration file and a corresponding preference file (ecp3_ddr3.lpf).
- **32bit_support** – This folder contains a 32-bit DDR3 core configuration file and a corresponding preference file (ecp3_ddr3.lpf).
- **64bit_dual_rank** – This folder contains a 64-bit DDR3 core dual-rank configuration file and a corresponding preference file (ecp3_ddr3.lpf).
- **Bitstream** – This folder includes a 64-bit demo bitstream. This bitstream is fully tested and can be used to verify the demo setup.
- **Doc** – This folder contains a user document that provides brief information about the demo procedure and setup, which can be used as a concise reference during a demo.

User_logic Folder

The user_logic folder includes the following subfolders:

- **Par** – This folder includes the implementation project files for the Diamond and ispLEVER tools and other necessary files including the place and route (PAR) preference and the post route trace preference files.
- **Sim** – This folder includes the simulation script files for the ModelSim and Active-HDL simulation tools.
- **Src** – This folder includes all RTL source files used for the demo.
- **Testbench** – This folder includes the test bench file for the demo design (ddr3_test_top_tb.v).

Figure 4. DDR3 Demo Package Directory Structure



Demo Procedure

Step 1. Core Generation

A default 64-bit DDR3 core LPC file is located under the **Core** folder. If a different configuration is needed, choose a configuration from the LPC files provided under the **Resource** folder.

a. Open the IPexpress tool and select the **Regenerate** icon. (**Tools > Regenerate IP/Module** for ispLEVER IPexpress).

b. Browse to the core folder where the lpc file is located. Select the lpc file and click **Open**.

c. Make sure the source and target devices are the same (family, package, speed). Click **Regenerate**.

d. Once the DDR3 core configuration GUI is launched, click **Generate**. The DDR3 IP core will be generated inside the folder where the lpc file is located.

*Note: If your DDR3 memory module requires different memory timing parameters, select the **Memory Device Timing** tab and modify the desired parameters. Most DDR3 UDIMM memory modules should not require timing changes.*

Step 2. Running Simulation

The demo package provides the simulation scripts for Active-HDL and ModelSim.

Active-HDL

a. Open the simulation script file (**ddr3_ecp3_demo.do**) and update the Lattice tool path names with your local folder name.

b. Launch Active-HDL Lattice Edition, then click **Cancel** in the **Getting Started** dialog box.

c. Change directory by entering **cd [your_local_path]\ddr3_demo\user_logic\sim\aldec** in the Console window.

d. Select **Tools > Execute Macro**, and then browse to the folder where the Active-HDL script (.do file) is located.

e. Select the **ddr3_ecp3_demo.do** file and then click **Open**.

f. Once the simulation is finished, you should see that the Console window displays "PASS: DEMO FINISHED SUCCESSFULLY, ALL DDR3 READ DATA MATCHED". You can also manually check the result by checking the err_det signal from the waveform. The err_det signal should remain low at all times for a successful demo.

ModelSim

a. Open the simulation script file (**ddr3_ecp3_demo.do**) and update the Lattice tool path names with your local folder name.

b. Launch the ModelSim simulator.

c. Select **File > Change Directory**, and then browse to the folder where the simulation script (**ddr3_ecp3_demo.do**) is located.

d. Select **Tools > Tcl > Execute Macro**, and then select the script file (**ddr3_ecp3_demo.do**) followed by clicking **Open**.

e. Once the simulation is finished, you should see that the Transcript window displays "PASS: DEMO FINISHED SUCCESSFULLY, ALL DDR3 READ DATA MATCHED". You can also manually check the result by checking the err_det signal from the waveform. The err_det signal should remain low at all times for a successful demo.

Step 3. Running Place & Route (PAR)

A design preference file (ecp3_ddr3.lpf) is located in the "user_logic\par\[software]" folder. Using a proper preference file is very important for a successful DDR3 implementation. When a different DDR3 bus size IP core is generated using the provided .lpc files, the corresponding .lpf file must be located in the par folder. The additional .lpc files and their paired .lpf files are found in the "resource" folder.

Diamond

a. Launch the Lattice Diamond design software.

b. Select **File > Open > Project** and browse to the **par** folder (**user_logic\par\diamond**).

c. Select the DDR3 demo project file for Diamond (**ecp3_ddr3.ldf**) then click **Open**.

d. Double-click **Place & Route Design** in the **Process** pane. The software will run synthesis, and place and route (PAR).

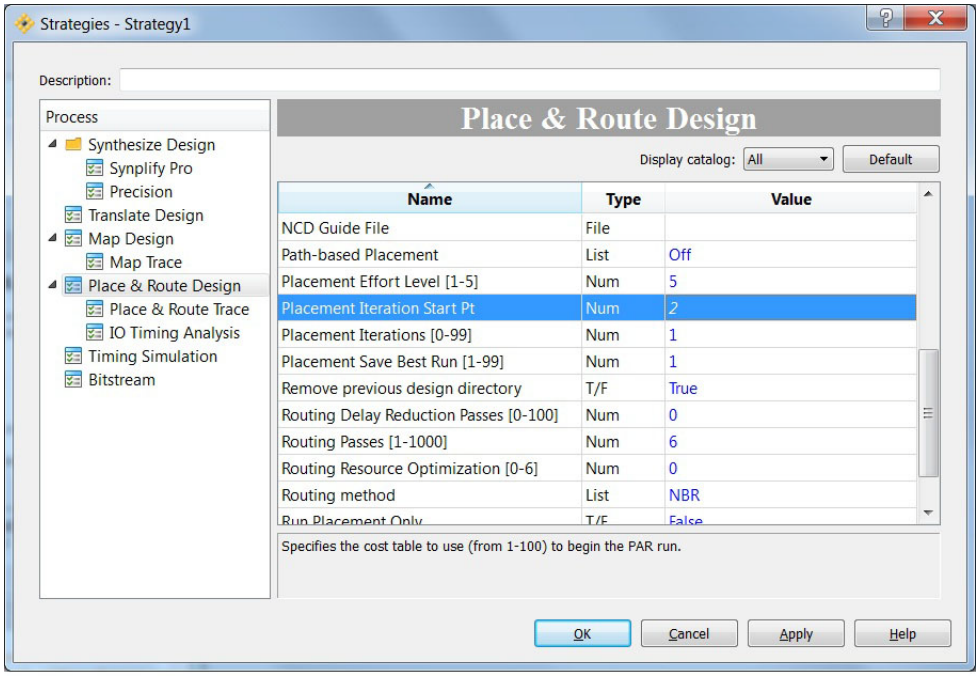
e. Run the Place & Route Trace process if the PAR process has been completed successfully.

f. Check the static timing results from the "Reports" tab. If there is a violation, it means that the PAR result for the current seed run does not meet the all timing requirements.

g. If a violation is reported, change to the next placement seed and check the timing result again. The placement seed can be changed in the provided strategy setting as shown in Figure 5. Select **Place and Route Design** and change the value for the **Placement Iteration Start Pt** entry. Repeat this process until all timing requirements are met.

h. With a successful timing result obtained, double-click on **Bitstream File** in the **Process** pane to generate a bitstream file.

Figure 5. Lattice Diamond Software Strategy Settings



Note: The DDR3 IP core has several timing-critical nets. Their net delays are tightly controlled using the MAX DELAY preference. Therefore, the implementation of a DDR3 core may require a multi-seed PAR run. The "mpartrce" command in the command line flow can also be used for implementation. Below is a command line example that uses the files from the Diamond design software flow. The .p2t file should contain your desired option values for a multi-seed run (-n, -t, -s).

mpartrce -p ecp3_ddr3_impl1.p2t -pr ecp3_ddr3_impl1.prf -tpr ecp3_ddr3.tpf.prf -log ecp3_ddr3.log -o ecp3_ddr3.csv ecp3_ddr3_impl1_map.ncd ecp3_ddr3_impl1.ncd

Step 4. Setting Up the DDR3 Demo

a. Make sure the LatticeECP3 I/O Protocol Board jumper settings follow the default jumper setting guidelines as shown in Figure 2.

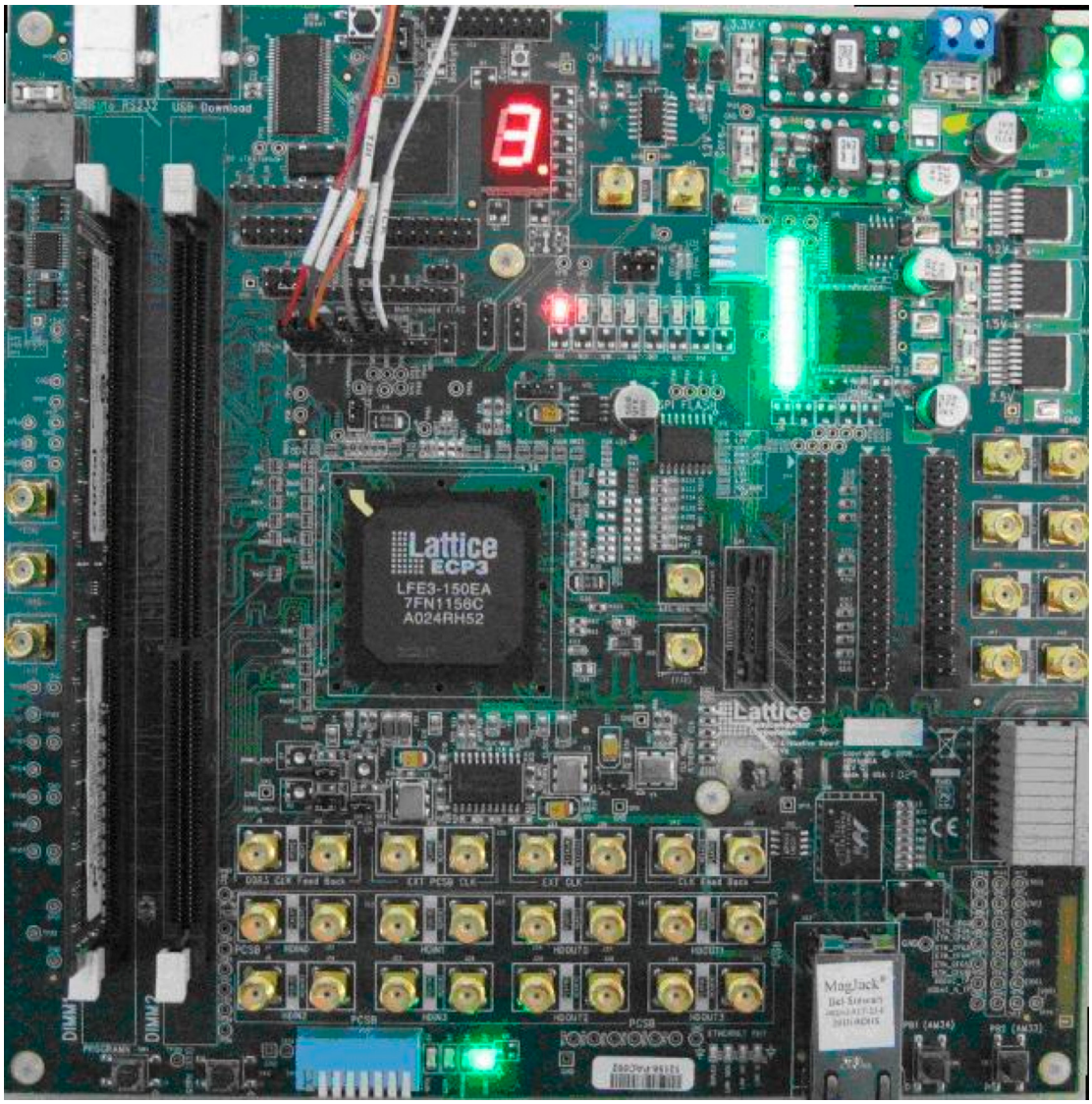
b. Install a DDR3 240-pin UDIMM into the DIMM1 socket that is located in the left-most side of the board.

c. Connect a JTAG download cable to the Local JTAG connector (**J10**) on the board.

d. Connect the USB or parallel connector of the JTAG download cable to a PC that has Lattice Diamond software installed.

e. Turn the board power on by connecting the power adapter plug into the board power jack (**J56**). Proper set-up is shown in Figure 6.

Figure 6. LatticeECP3 I/O Protocol Board Setup for DDR3 Demo



Step 5. Running the Demo

Diamond Programmer

a. Launch the Diamond Programmer tool.

b. Scan the JTAG chain by selecting **Design > Scan**.

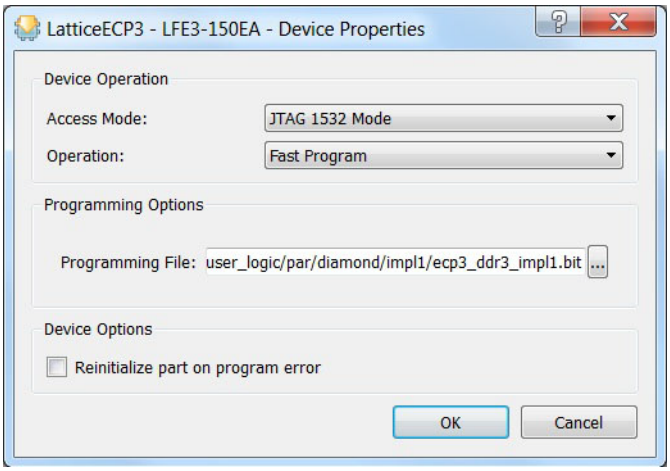
c. Double click the **Status** or **Operation** field to open the Device Properties box.

d. Make sure that the Device Operation mode is set to **JTAG 1532 Mode with Fast Program** (default setting).

e. Select the **File Name** field then click the **Browse** button and browse to the project implementation folder where the generated bitstream file is located. Click **Open** as shown in Figure 7. Then click **OK**.

f. Click on the **Program** button from the toolbar or select **Design > Program** to download the bitstream.

Figure 7. Diamond Programmer Device Properties



g. Configure your demo to a test mode using the DIP switch (**SW4**) setting as described previously.

h. Set the TP jumpers (**J57**) if a different demo configuration is desired other than the default.

i. Press the **GSRN** button (**SW2**) to initialize the core and the demo user logic.

j. Press the **PB1** button (**SW6**) to begin the DDR3 demo transaction.

k. Some of the demo modes are dynamically switchable, as described previously. Experiment with the DIP switch settings to test other modes.

l. Check the output LEDs to see if their outputs match with the expected result.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2010	01.0	Initial release.
January 2011	01.1	Updated for DDR3 IP core version 1.2.
		DIMM support changed to 2GB.
		Corrected LatticeECP3 I/O Protocol Board default jumper settings (Figure 2).
		Added standard USB cable downloading procedure.
March 2011	01.2	Changed document title to “DDR3 Demo for the LatticeECP3 I/O Protocol Board”.
September 2011	01.3	Updated for DDR3 IP core version 1.3.
		Updated for Diamond 1.3 support.
		Aldec Active-HDL simulation flow changed to remove user file copy requirement.
June 2012	01.4	Updated for DDR3 IP core version 1.4.
		Updated for Diamond 1.4 support
		Removed ispLEVER flow
		Dual-rank mode enabled, up to 4GB UDIMM module support
		Improved testbench to notify the simulation result
		Updated document with new corporate logo.