



LatticeECP3 HDMI/DVI Loopback Demo

User's Guide

Introduction

This guide describes how to use the LatticeECP3™ Video Protocol Board and HDMI Mezzanine Card to demonstrate the LatticeECP3 HDMI/DVI Interface Reference Design featuring LatticeECP3 SERDES.

The reference design consists of the HDMI Transmitter and Receiver cores which are compatible with both HDMI and DVI physical layer protocols. You can use this design to evaluate the SERDES-based HDMI/DVI physical layer solution for your specific application.

This guide will familiarize you with the contents of the Display Interfaces Development Kit and walk you through the process of setting up the hardware platform with the LatticeECP3 Video Protocol Board, HDMI Mezzanine Card and accessories. This document assumes that you have already installed ispLEVER® software on your Windows-based system, and are familiar with the basic processes and tools in ispLEVER software. Please be aware that it is not necessary to install ispLEVER software prior to setting up the hardware platform and running the demo, but it is recommended to have the ispLEVER software installed so that you can experiment with the ORCAstra and Reveal™ tools for both debugging and demonstration purposes.

If you are new to ispLEVER software and the LatticeECP3 Video Protocol Board, we recommend that you read each section of this user's guide and follow the instructions in a sequential manner. You may also refer to the ispLEVER Help system.

Learning Objectives

After you complete the steps in this guide, you will be able to do the following:

1. Set up the LatticeECP3 Video Protocol Board and HDMI Mezzanine Card properly for the demo and become familiar with the evaluation board's main features.
2. Establish a HDMI or DVI link and run the LatticeECP3 HDMI/DVI Loopback Demo by displaying the video/audio source on a display such as a PC monitor or flat-panel HDTV.
3. Monitor the HDMI/DVI receiver's status through the user-defined LED lights on the LatticeECP3 Video Protocol Board.
4. Control the HDMI/DVI Transmitter's video and audio outputs through the user-defined switches on the board.
5. Use the ORCAstra tool to monitor the SERDES/PCS status and dynamically adjust the settings if necessary.
6. Become familiar with the reference design flow and approach that will enable you to modify and rebuild the HDMI/DVI physical layer interface for your own purposes.

Contents of the Display Interfaces Development Kit

Documentation and Design Files

Along with this user's guide, you can obtain more detailed information on the design and the demo boards by referring to the following documents:

- RD1097, [LatticeECP3 HDMI/DVI Interface Reference Design](#). Included with the kit, this document provides functional descriptions of the HDMI/DVI transmitter and receiver cores instantiated in the demo design.
- EB52, [LatticeECP3 Video Protocol Board Revision C User's Guide](#). Included with the kit, this user's guide describes the board features, power supplies, device programming, LED/DIP switch pinout and board schematics in detail.
- EB55, [HDMI Mezzanine Card Revision B User's Guide](#). This user's guide, also included with the kit, describes the board features, header settings and board schematics in detail.
- Verilog-HDL source code of the demo design and the ngo netlist files of the HDMI transmitter and receiver cores.

Demo Hardware

- LatticeECP3 Video Protocol Board Revision C featuring the LatticeECP3 LFE3-95EA-7FN1156C FPGA device
- HDMI Mezzanine Card Revision B
- Two sets of HDMI cables
- Optional two sets of HDMI-to-DVI conversion cables
- ispDOWNLOAD™ (USBN-2A) cable
- 12V DC wall adapter
- PC for running programming and debugging tools (not included in the development kit)
- HDMI source, which is not included in the demo kit, must be non-HDCP encrypted (e.g. digital camcorder, laptop with HDMI output etc.). The HDMI source from a DVD player or Blu-Ray player that is HDCP encrypted cannot be used as the source for this demo design.
- HDMI-equipped full high-definition TV or monitor with speakers (not included in the development kit)

Demo Software

- ispLEVER 8.1 or later for compiling the demo design and generating a new bitstream (a demo bitstream file is included in the project directory)
- ispVM™ System 17.8 or later for downloading the bitstream into the FPGA
- ORCAstra software for SERDES/PCS register configuration (included in ispLEVER 8.1 or later)

Demo Overview

Figure 1 shows the LatticeECP3 Video Protocol Board and HDMI Mezzanine Card used for this demo.

Figure 1. LatticeECP3 HDMI/DVI Demo Board Setup

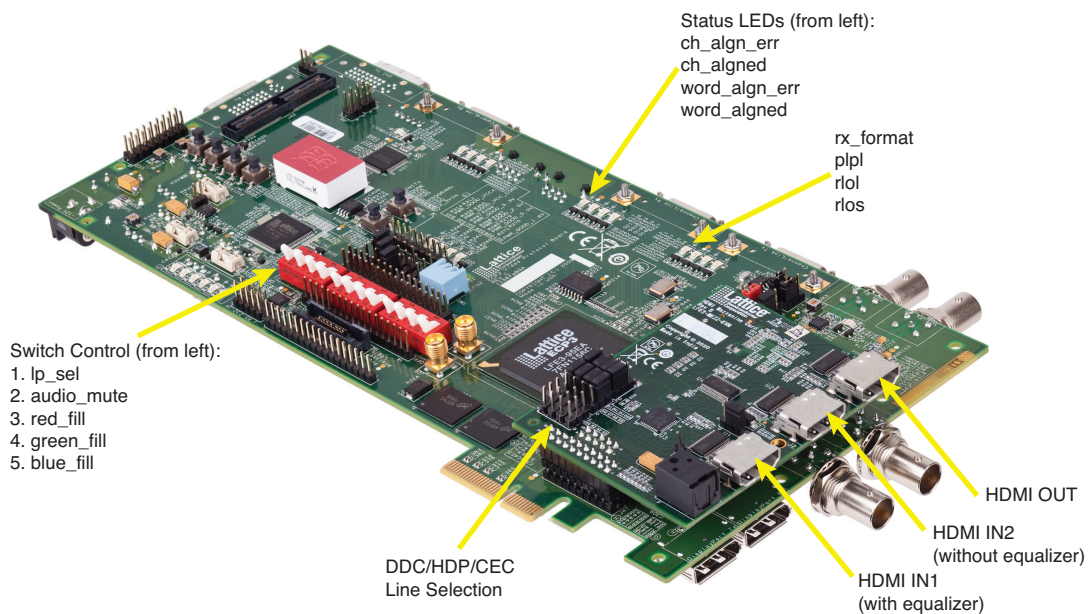
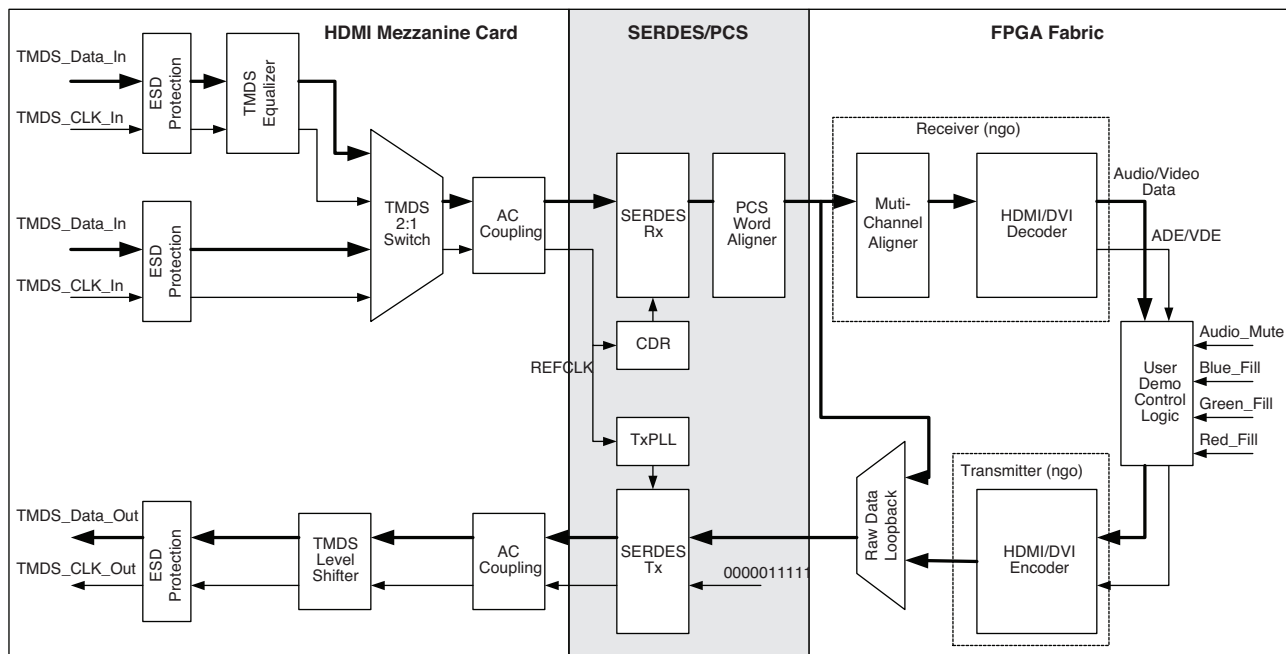


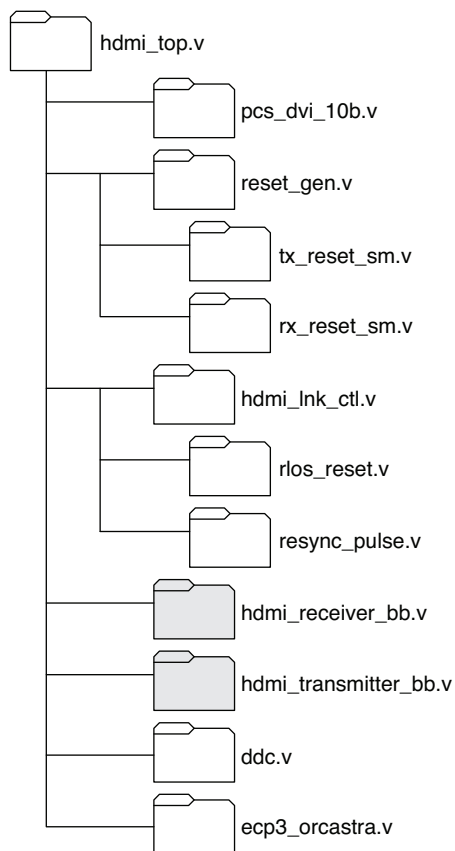
Figure 2 shows the block diagram of the LatticeECP3 HDMI/DVI Loopback Demo based on the HDMI transmitter and receiver cores.

Figure 2. LatticeECP3 HDMI/DVI Loopback Demo Block Diagram



For this demo design, the PCS Quad C is used. It has been generated in 10-bit SERDES mode (10BSER) and the SERDES Tx/Rx Data Rate is set to 1.65Gbps. For the lower-resolution HDMI/DVI display mode, the SERDES Tx/Rx data rate can be adjusted through the ORCAstra GUI. Refer to RD1097 for a detailed functional description of the HDMI transmitter and receiver cores and SERDES/PCS configurations.

Figure 3 shows the hierarchy of the demo design. Due to the complexity of the design, this figure only lists the major functional modules.

Figure 3. HDMI/DVI Loopback Demo Design Hierarchy

The function of each module in Figure 3 is described in Table 1.

Table 1. HDMI/DVI Loopback Demo Functional Block Descriptions

Module	Description
hdmi_top.v	Top-level module of the demo design.
pcs_dvi_10b.v	PCS interface file, customized in IPexpress™.
reset_gen.v	Reset sequence generator, based on recommendations made in TN1176, LatticeECP3 SERDES/PCS Usage Guide .
tx_reset_sm.v	Sub-module of reset_gen, Tx reset sequence state machine.
rx_reset_sm.v	Sub-module of reset_gen, Rx reset sequence state machine.
hdmi_lnk_ctl.v	HDMI Link Controller module, generates internal reset signals.
rlos_reset.v	Sub-module of hdmi_lnk_ctl. Generates internal reset when rlos transmits from high to low, indicating a cable plug-in condition.
resync_pulse.v	Sub-module of hdmi_lnk_ctl. Generates internal reset upon the detection of an error from the HDMI receiver module.
hdmi_receiver_bb.v	Black-box interface file for the HDMI receiver NGO netlist.
hdmi_transmitter_bb.v	Black-box interface file for the HDMI transmitter NGO netlist.
ecp3_orcastra.v	LatticeECP3 ORCAstra GUI interface module.
ddc.v	Emulated DDC Interface for DVI protocol.

LatticeECP3 HDMI/DVI Loopback Demo Procedure

Download the Display Interfaces Development Kit from the Web

You can download and install the Display Interfaces Development Kit from the Display Interfaces Development Kit web page on the Lattice web site.

Demo Hardware Setup

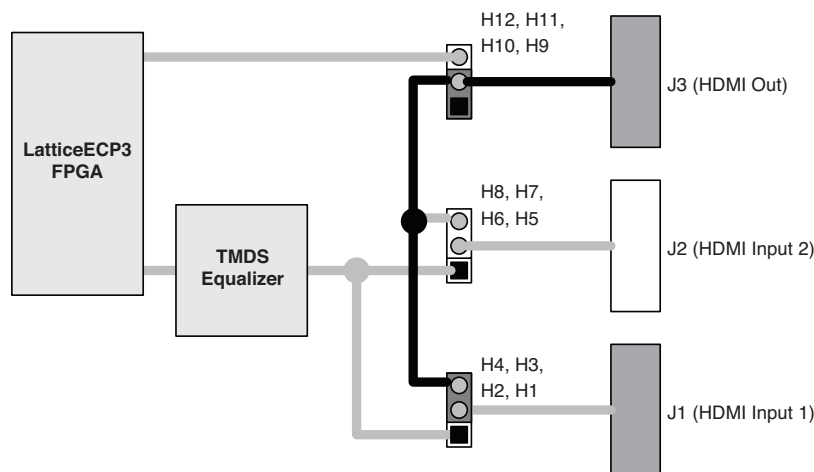
1. Install the HDMI Mezzanine Card on top of the LatticeECP3 Video Protocol Board by plugging the HDMI Mezzanine connector and Control Signal connector into their corresponding sockets.
2. Configure the HDMI Mezzanine Card H13 and H1~H12 headers based on the selection of the HDMI input port (J1 or J2). The J1 HDMI input port has an equalizer. The J2 HDMI input port has no equalizer. Header H13 determines which HDMI input port (J1 or J2) is chosen; header H1~H12 determines how the CEC, HPD and DDC clock and data signals are passed through. Table 2 shows the proper header settings of H13 and H1~H12 based on the selection of HDMI input port and CEC, HPD and DDC pass-through mode.

Table 2. HDMI Mezzanine Card H13 and H1~H12 Header Configuration Table

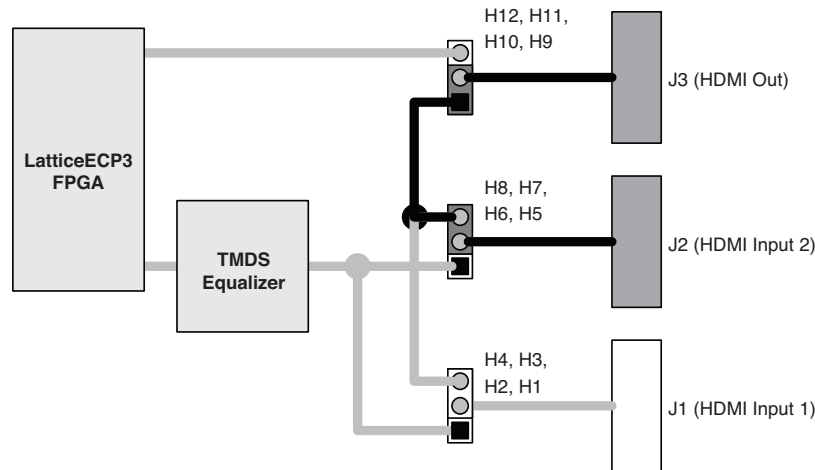
HDMI Input Selection	CEC/HPD/DDC Pass-thru Mode	H13	H9~H12	H5~H8	H1~H4
J1	J1 → J3	Shunt pins 1 and 2	Shunt pins 1 and 2	Open	Shunt pins 2 and 3
J2	J2 → J3	Shunt pins 2 and 3	Shunt pins 1 and 2	Shunt pins 2 and 3	Open

To choose J1 as the HDMI input port, shunt pin1 and pin2 of H13; to pass CEC/HPD/DDC signals from J1 to J3, shunt pin1 and pin2 of H9~H12 headers, leave H5~H8 headers open, and shunt pin2 and pin 3 of H1~H4 headers. Figure 4 shows the conceptual configuration of H1~H12 headers for connecting CEC/HPD/DDC signals from J1 to J3. The square pin is the pin 1 of the header and the shunt is indicated by the darker gray color on the header.

Figure 4. CEC/HPD/DDC Pass-thru From J1 to J3



To choose J2 as the HDMI input port, shunt pin2 and pin3 of H13; to pass CEC/HPD/DDC signals from J2 to J3, shunt pin 1 and pin 2 of H9~H12 headers, shunt pin2 and pin3 of H5~H8 headers, and leave H1~H4 headers open. Figure 5 shows the conceptual configuration of H1~H12 headers for connecting CEC/HPD/DDC signals from J2 to J3. The square pin is the pin 1 of the header and the shunt is indicated by the darker gray color on the header.

Figure 5. CEC/HPD/DDC Pass-thru From J2 to J3

- On the receiver side, plug one end of the HDMI cable into one of the HDMI input connectors (J1 or J2) of the HDMI Mezzanine Card based on the H13 header setting in Step 2. The other end of the HDMI cable is connected to a HDMI or DVI source (e.g. a HD camcorder). The HDCP encrypted source (e.g. DVD or Blu-Ray player) cannot be used for this demo.

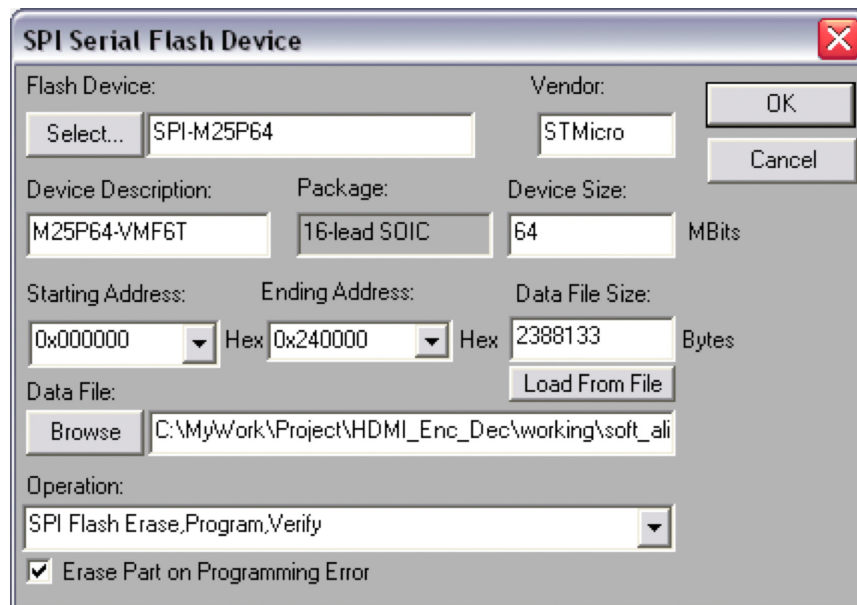
If the demo source is DVI (e.g. laptop DVI output), simply replace the HDMI cable with the HDVI-to-DVI Conversion cable. Plug the HDMI end into the HDMI input port (J1 or J2) of the HDMI Mezzanine Card and plug the DVI end into the DVI source output port.

- On the transmitter side, plug one end of the HDMI cable into the HDMI output connector (J3) of the HDMI Mezzanine Card. The other end of the cable is connected to a HDMI-capable display device such as a LCD HDTV.

If the sink device is a DVI-equipped PC monitor, simply replace the HDMI cable with the HDMI-to-DVI Conversion cable. Plug the HDMI end into HDMI output port (J3) of the HDMI Mezzanine Card, plug the DVI end into the PC monitor's DVI port.

FPGA Device Configuration

- Install the Lattice ispJTAG™ USB download cable on the J28 header of the LatticeECP3 Video Protocol Board. Refer to EB52, [LatticeECP3 Video Protocol Board Revision C User's Guide](#), for the ispVM JTAG connector pin definitions.
- Referring to EB52, [LatticeECP3 Video Protocol Board Revision C User's Guide](#), choose Jumper Setting #5 to include only the LatticeECP3 device on the JTAG daisy chain of the LatticeECP3 Video Protocol Board.
- Plug in the 12V DC wall-mount power supply.
- Launch ispVM System software on the PC. Click the **Scan** button and select the LFE3-95EA device in the **Device Information** window.
- If you choose SPI Flash Background Programming mode, select STMicro's SPI-M25P64 as the on-board 64-Mbit SPI flash device (see Figure 6). Press the **OK** buttons to exit the SPI Serial Flash Device and Device Information windows.

Figure 6. SPI Flash Configuration Window

6. Click the **Go** button in the ispVM System main window. Download the bitstream into the LatticeECP3 device on the LatticeECP3 Video Protocol Board.

PCS Configuration Through the ORCAstra GUI

This section describes the use of the ORCAstra GUI to interactively change or monitor the LatticeECP3 PCS register values. If you decide to keep the original PCS register settings, or if you don't want to dynamically monitor the PCS status registers, you can skip this section.

Ensure the LatticeECP3 HDMI/DVI Loopback Demo bitstream has been loaded into the LatticeECP3 FPGA on the LatticeECP3 Video Protocol Board successfully, then:

1. Launch the ORCAstra GUI by selecting **Tools > ORCAstra** from the ispLEVER Project Navigator menu.
2. In the ORCAstra FPGA Control Center Window, select **Interface > 1 ispVM JTAG Hub USB Interface**.
3. Select **Device > Lattice ECP3**.
4. Click on the **ECP3 PCS 2** option. This will launch the ECP3-PCS 2 window. You can selectively open or close the Main, Pwr Rst Alrms, SERDES Buffer Options, Clocking, Diagnostics and Status tabs. The PCS GUI, as shown in Figure 7, is useful for checking the status of the PCS registers.

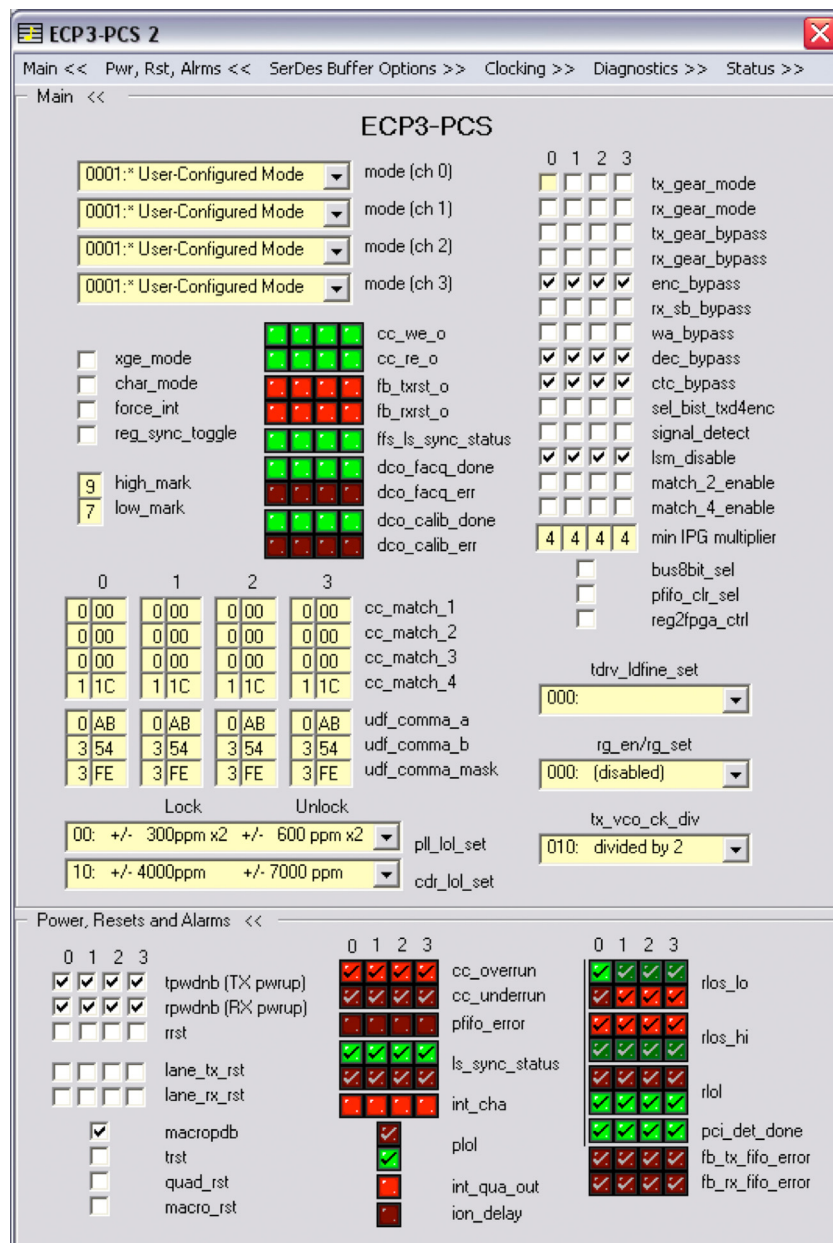
Note that:

- a. The rlos_lo indicator of channel 0 is red, while the other channels are green. This is because the three TMDS data input channels are connected to SERDES channels 1 to 3. SERDES channel 0 is not connected.
- b. The rlol indicators of channel 1 to 3 are all green.
- c. The plol indicator is also green.

This means that the PCS is locking to the clock and the receive section of the channels has properly synchronized to the incoming data.

- For a continuous update of the PCS register status, click on the **Continuous Polling** check-box in the ORCAstra FPGA Control Center window.

Figure 7. ECP3-PCS 2 ORCAstra View



On-board Switches and LEDs

The LatticeECP3 Video Protocol Board provides three SPDT toggle-DIP switches. Each of these switches includes four positions for a total of 12 static input signals for the user to control. Table 3 lists the pin definitions of the DIP switches used for this demo. When the positions of these switches are switched to the edge of the board, as seen in Figure 1, they are in the OFF state.

Table 3. DIP Switch Pin Definitions

Switch Number	Position	Pin Name	LatticeECP3 Pin Number	Description
SW1	1	oen_equ_i	Y5	Equalizer output enable
	2	pre_equ_i	Y4	Equalizer Pre-emphasis enable
	3	equ_boost_i_0	Y9	TMDS input equalization select
	4	equ_boost_i_1	Y10	
SW3	1	Reserved	AD2	Reserved
	2		AD1	
	3		AC6	
	4	blue_fill	AC7	Fill blue pixels with 255
SW4	1	green_fill	AM1	Fill green pixels with 255
	2	red_fill	AM2	Fill red pixels with 255
	3	audio_mute	AE1	Remove audio/aux packets
	4	lp_sel	AE2	Raw data loopback selection

SW1 is used to control the equalizer (STDVE001) of the HDMI Mezzanine Card when the J1 HDMI input is chosen. For this demo, all four positions of SW1 are set to OFF.

SW3 positions 1 to 3 are reserved for future use. They are also set to OFF.

SW4 positions 1 to 4 and SW3 position 4 are defined to control the data flows for the demo:

1. When SW4 position 4 is turned on, the lp_sel input signal enables the raw data loopback from the Rx channels to Tx channels, bypassing the decoder and encoder. If the blue_fill, green_fill and red_fill switches are all OFF, there is no visual difference when this control is switched on or off. This control is useful for debugging purposes to check if the HDMI stream can pass through the SERDES Rx and Tx channel successfully when the decoder and the encoder are bypassed.
2. When SW4 position 3 is turned on, the audio_mute input signal masks the ADE signal. Therefore, it removes the audio and auxiliary data from the decoded TMDS data. You will notice that the audio is muted when it is switched to the ON position.
3. When SW3 position 4 and SW4 positions 1 and 2 are switched ON or OFF independently or in combinations, the corresponding Blue, Green and Red channels will replace the video pixel data with a constant value of 255 (8'hFF). The screen will display different combinations of blue, green and red colors.

By manipulating the SW4 positions 1 to 4 and SW3 position 4, we demonstrate that the RGB pixel data and audio data are properly processed by the HDMI/DVI encoder and decoder.

Note: There are three different pixel encodings that may be sent across an HDMI cable: RGB 4:4:4, YCBCR 4:4:4 and YCBCR 4:2:2. This demo assumes the HDMI video source is in RGB format. If the video source is in the YCBCR color space, when you switch SW3 position 4, SW4 position 1 and 2, you may get unexpected color fill effects, because you are now changing Luminance and Chrominance components instead of Blue, Green and Red pixel data. If you turn on the Audio_Mute (SW4 position 3) switch, you may also notice the color changes, because the Audio_Mute function also filters out the InfoFrame packets which may carry the video format information.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
September 2010	01.0	Initial release.