LatticeECP3 DVI / 7:1 LVDS Video Conversion Demo

User's Guide

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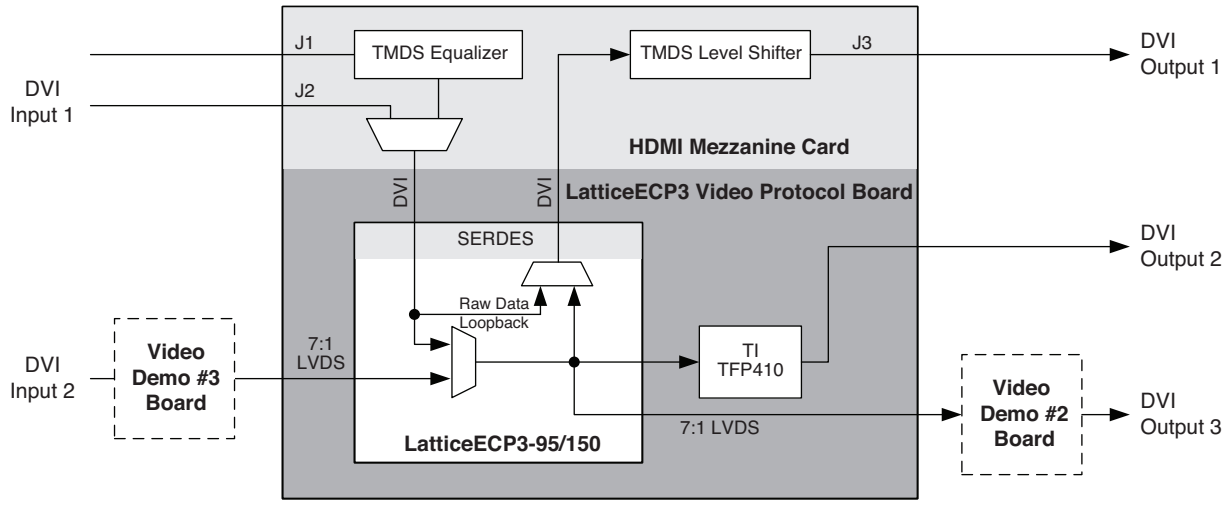
Introduction

The Digital Visual Interface (DVI) is a high-speed digital connection for visual data between a computer and its display device. The interface is simple and low cost, and is used for all segments of the PC industry (workstations, desktops, laptops, etc). For the single-link mode, the data rate can reach 165M pixels per second.

7:1 LVDS is a serial LVDS bus commonly used in embedded LCD displays for products such as laptops or netbooks. ChannelLink is a highly cost-effective video interface that can be used for transfer pixel data through 7:1 LVDS.

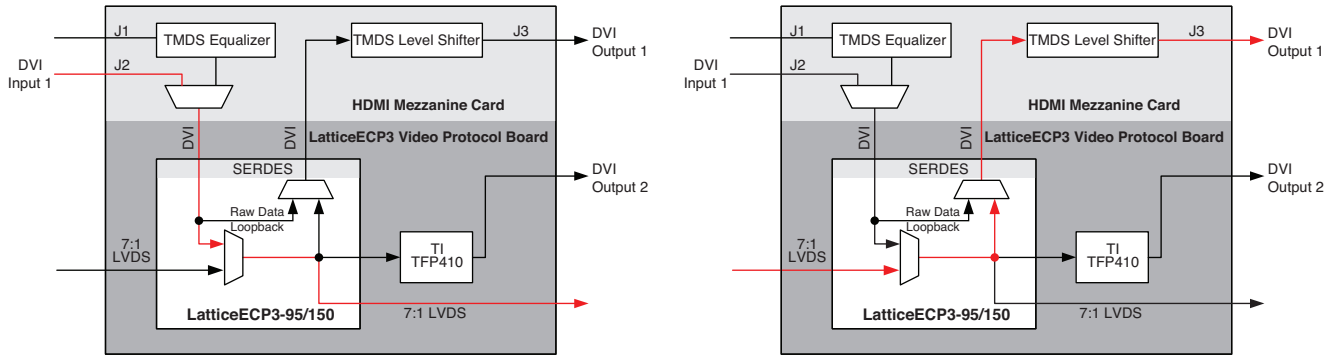
Figure 1. Block Diagram of the DVI / 7:1 LVDS Conversion Demo Setup



This user's guide describes a 2-to-1 video MUX demo. As shown in Figure 1, the MUX output is further rendering out through three different paths. This demo shows the capability of the LatticeECP3™ FPGA in video applications. On the input side, either DVI signals to a SERDES deserializer or LVDS signals to a LVDS receiver can be the input data source. One of the two data sources will be selected as the data input of this demo. Then the selected data will be encoded into the following three formats and the same video will be output through three different connectors. Although this demo uses HDMI connectors, the signals are compatible TMDS DVI only signals.

1. **Parallel RGB signals** – Sent through general purpose I/O pins and the DVI encoder (Texas Instruments TFP410) to a DVI connector on the LatticeECP3 Video Protocol Board.
2. **DVI video payload** – Sent out through SERDES output pins, then AC coupling capacitors and the TMDS Level Shifter to an HDMI connector on the HDMI Mezzanine Card.
3. **7:1 LVDS video signals** – Sent through LVDS pins to the ChannelLink Tx connector on the LatticeECP3 Video Protocol Board.

Figure 2. Data Flow Diagram



With 50-ohm external pull-up resistors, AC coupling capacitors and an optional TMDS Equalizer (on the HDMI Mezzanine Card selected by a jumper), the LatticeECP3 SERDES deserializer is able to receive the TMDS signal. With an external Level Shifter, the LatticeECP3 SERDES serializer acts as a TMDS transmitter. Both of these functions are implemented on a daughter card (HDMI Mezzanine Card) for the LatticeECP3 Video Protocol Board.

The design is synthesized with ispLEVER® 8.1 and has been validated on the LatticeECP3 Video Protocol Board Revision C with the HDMI Mezzanine Card Revision B.

Features

- Supports video data sources of LVDS signals (FlatLink or ChannelLink) and DVI signals
- Supports LVDS signals output to a ChannelLink_Tx port, and DVI signals output to DVI via HDMI ports
- Supports VESA Extended Display Identification Data (EDID) and Display Data Channel (DDC) functions
- Single-Link DVI on both DVI Rx and Tx ports
- Supports various display resolutions up to 1600(H) x 1200(V) x 60(fps)

Functional Description

For this demo, the video source input can be either LVDS signals (input from the ChannelLink_Rx port) or DVI signals (input from the HDMI Rx port on the daughter card). The two serial data groups will be synchronized and decoded into 8-bit parallel RGB data and the related control signals, hsync, vsync and DE. A switch will be used to select a video source as the data input. The selected data will be decoded into parallel data. A DVI encoder will encode the parallel data and send them out through a DVI Tx port. At the same time, the parallel RGB data are also converted to LVDS serial data and DVI serial data, and a LVDS transmitter and a SERDES serializer will send them out.

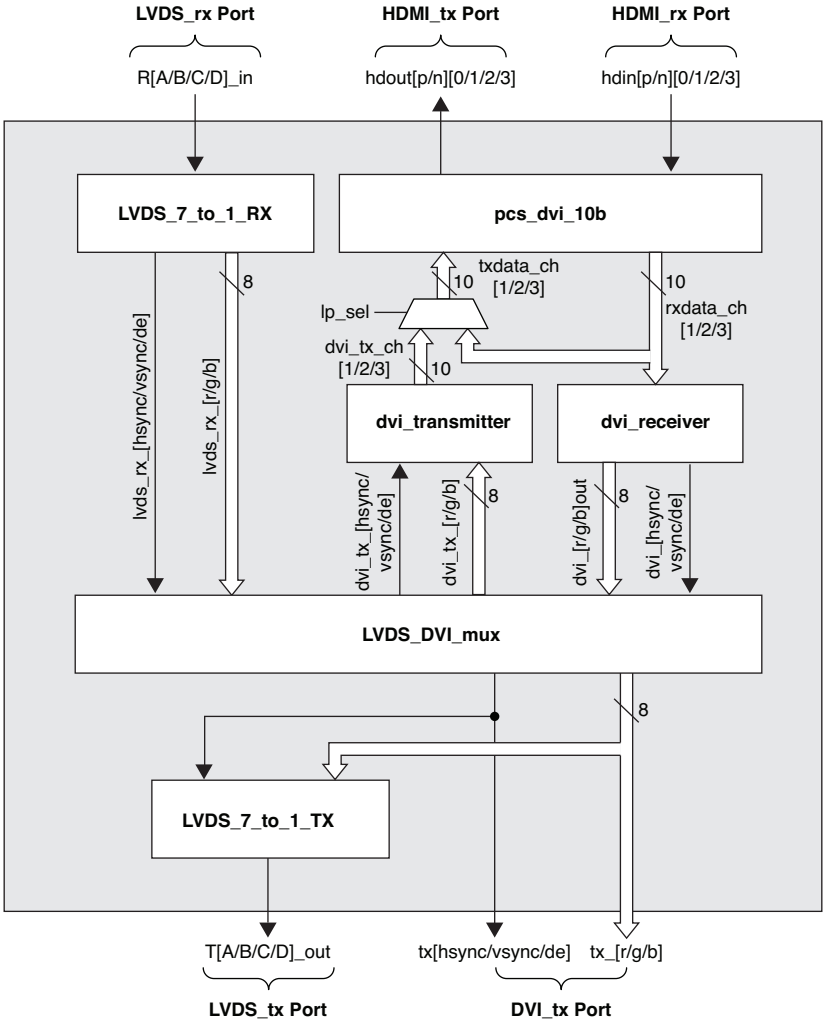
In this demo, the LVDS receiver and transmitter modules are the same as the LatticeECP2/M 7:1 LVDS Video Interface reference design, while the DVI encoder and decoder modules are same as the HDMI/DVI Rx/Tx reference design. For further information, see RD1030, LatticeXP2, LatticeECP2/M and LatticeECP3 7:1 LVDS Video Interface User's Guide and RD1097, HDMI/DVI Rx/Tx User's Guide.

Table 1. Supported Video Formats

Resolution	LVDS_in			DVI_in via HDMI Connector		
	DVI_out via TFP410	LVDS_out	DVI_out via HDMI Connector	DVI_out via TFP410	LVDS_out	DVI_out via HDMI Connector
800*600*60	No	No	No	—	—	—
800*600*75	Yes	Yes	Yes	—	—	—
1024*768*60	Yes	Yes	Yes	Yes	Yes	Yes
1024*768*75	Yes	Yes	Yes	Yes	Yes	Yes
1152*864*75	Yes	Yes	Yes	Yes	Yes	Yes
1280*1024*60	Yes	Yes	Yes	Yes	Yes	Yes
1280*1024*75	No	No	No	Yes	Yes	Yes
1920*1080*60	—	—	—	Yes	No	Yes
1600*1200*60	—	—	—	Yes	No	Yes

The functional block diagram of the demo is shown in Figure 3.

Figure 3. Functional Block Diagram of the Top-Level Design



Note: Signal names such as pre_[a/b][0/1/2] include signals pre_a0, pre_a1, pre_a2, pre_b0, pre_b1 and pre_b2.

Module LVDS_7_to_1_RX

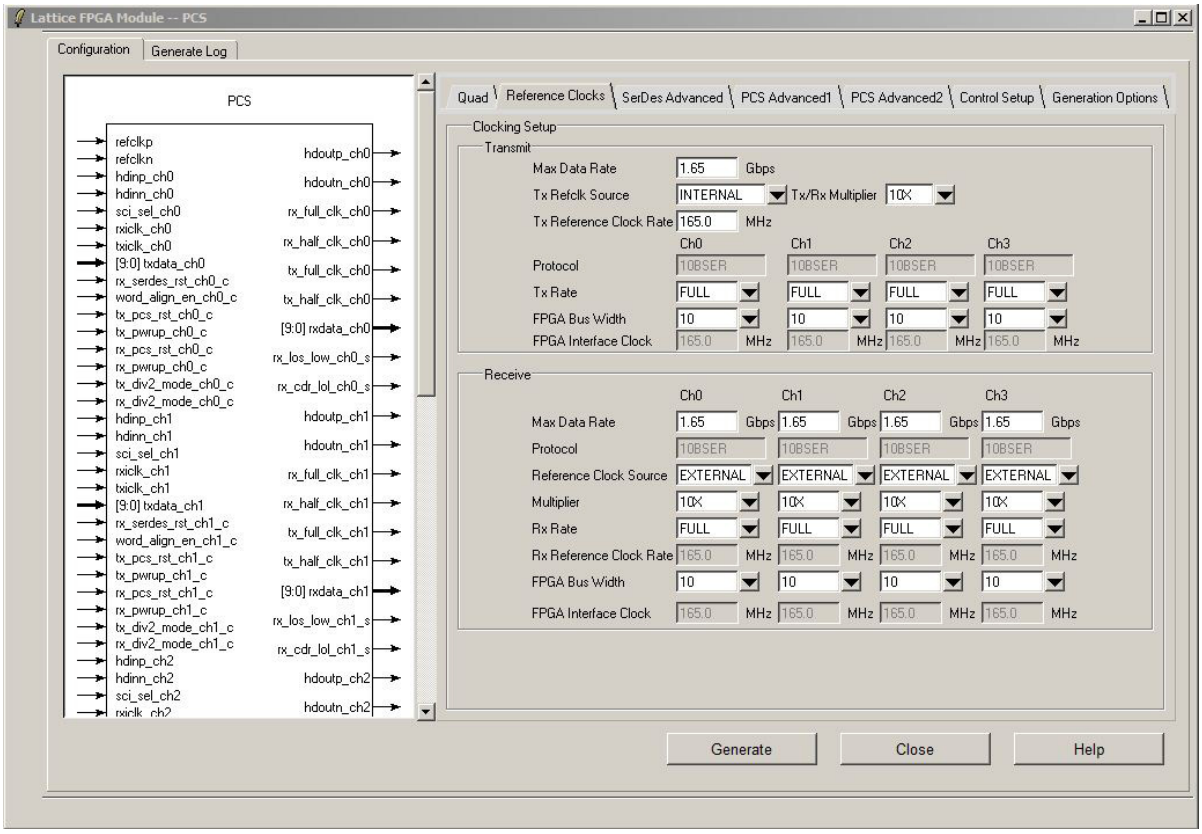
Through the ChannelLink_Rx port on the LatticeECP3 Video Protocol Board, one differential LVDS clock and four differential LVDS data are sent to this module. In this module, the serial data are packed into 8-bit parallel data and the related control signals, hsync/vsync/de, are generated. We can use four switches on the board to do the phase adjustment of the internal PLL, or we can also select the internal phase adjustment.

Module pcs_dvi_10b

pcs_dvi_10b is a PCS module using 10BSER mode which is generated by the IPexpress™ tool. The functions of a SERDES deserializer and a SERDES serializer are integrated into this module.

Figure 4 shows the configuration of the PCS module.

Figure 4. PCS Module Configuration



From the HDMI Rx port on the daughter card, one differential DVI clock and three differential DVI data are input to the SERDES deserializer. The input data will be de-serialized into 10-bit format and sent to the module dvi_dec_top.

Either the 10-bit data from the SERDES deserializer or the encoded 10-bit RGB data from the module dvi_enc_top can be selected as the data source of the SERDES serializer. The SERDES serializer sends out the serialized DVI data to the Level-Shifter on the daughter card. Then the DVI data can be sent out through the HDMI Tx port.

Module dvi_dec_top

According to the DVI specification, 10-bit data are decoded into 8-bit RGB pixels and the related control signals. An NGO file is available for this module.

Module dvi_enc_top

In this module, the selected 8-bit RGB data and the related control signals are encoded into 10-bit TMDS format, and the encoded data are sent to the module pcs_dvi_10b. An NGO file is available for this module.

Module LVDS_DVI_mux

In this module, either the decoded LVDS signals or the decoded DVI signals are chosen as the output data. The selected data and the related control signals, hsync/vsync/de, are sent to the internal modules dvi_enc_top and LVDS_7_to_1_Tx and the external DVI_encoder chip (Texas Instruments TFP410).

Module LVDS_7_to_1_TX

The selected data and related control signals are converted to the 7:1 LVDS data format and the LVDS data are serialized and sent out.

Demo Kit

The Demo Kit for this design includes the following items:

Table 2. Demo Kit Contents

Item	Description	Quantity
1	LatticeECP3 Video Protocol Board	1
2	Video demo board #2 used to convert 7:1 LVDS to DVI	1
3	Video demo board #3 used to convert DVI to 7:1 LVDS	1
4	HDMI Mezzanine Card	1
5	VGA-to-DVI box	1
6	+12V wall mount power adapter (for item 1)	1
7	+5V wall mount power adapter (for item 5)	1
8	+3.3V power supply (for item 2 and item 3)	1
9	MDR-26 Channel-Link cable	2
10	DVI-to-HDMI cable	2
11	DVI cable	2
12	Black banana plug cable	2
13	Red banana plug cable	2

Demo Settings

To run this demo, you need to connect data ports and adjust some switches to make the system work. Figure 5 shows the functions of the connectors, switches, push-buttons and LEDs which are used in the demo.

First, to provide power to PCSC, the SERDES quad, install shunt jumpers across pins 2 and 3 of J18 and J22 on the LatticeECP3 Video Protocol Board. On the daughter card, select the two pins in the J2 group of H1. Install shunt jumpers across pins 1 and 2 of H5/H6/H7/H8 to select the internal EDID function.

Use switch SW3_4 to select a different phase adjustment mode for the LVDS receiver PLL. When the auto-generate mode is selected (SW3_4 is OFF), the phase of the PLL will be generated internally. You can also choose manual-select mode (SW3_4 is ON), and do the phase adjustment by changing the switches SW4_1/SW4_2/SW4_3/SW4_4. For both modes, the current phase is shown by the 16-segment LED in hex mode. The switch SW1_1 is used to choose whether the LVDS data input is used to display.

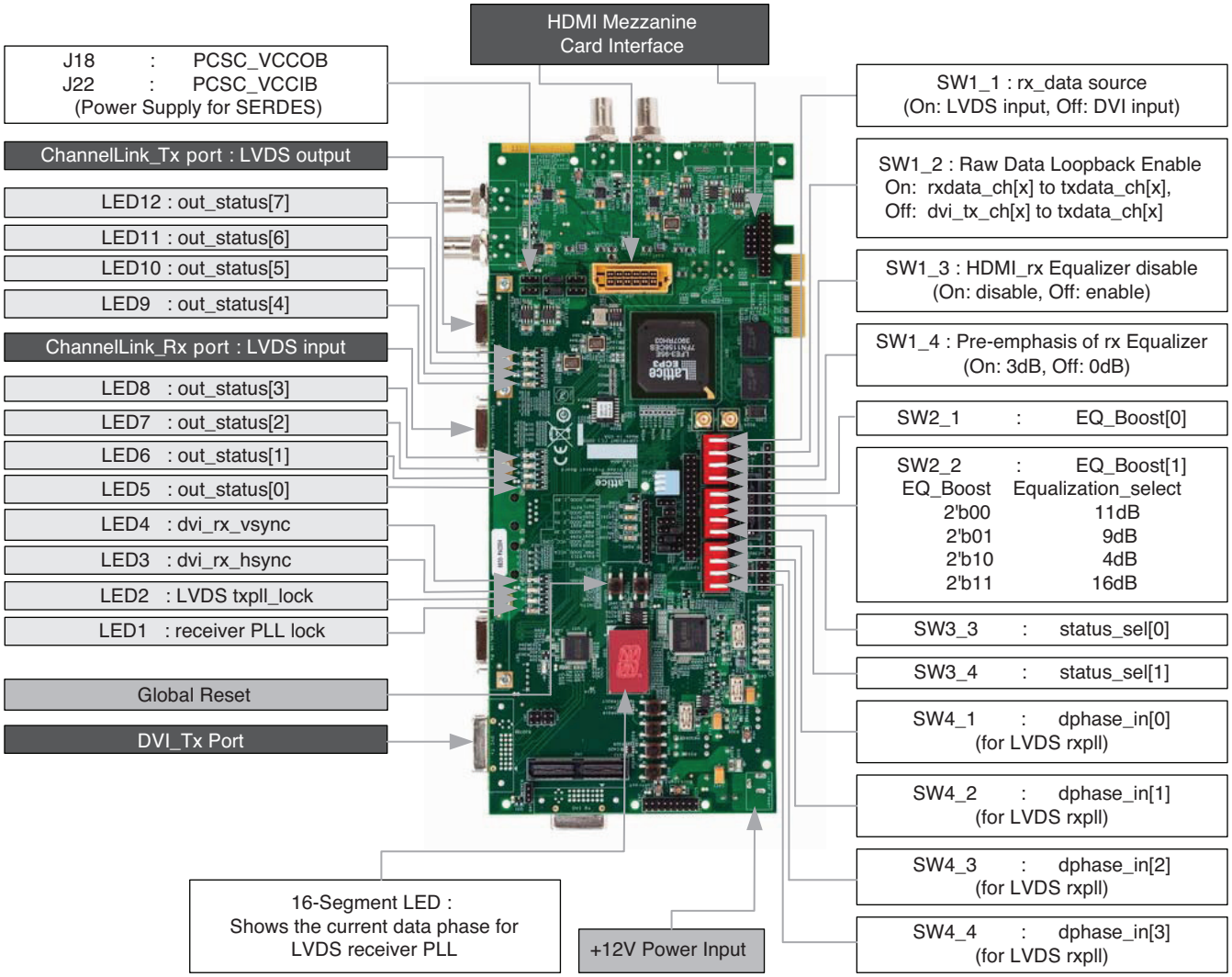
You can also use the switches SW3_3/SW3_4 to select the contents of the output status, and the status is indicated by the eight LEDs including LED5 to LED12. In this design, the pixel rate (f_in) of the input DVI video can be calculated by the formula: f_in = (rclk_cnt[15:0] / 640)MHz. When the DVI data input is selected, the eight LEDs

show the status of signal_lost and lost_lock for the three data channels. When the LVDS data input is selected, the status of dphase_lock and rxpll_lock for the LVDS receiver can be checked.

Table 3. Contents of LED5 to LED12

{SW3_4, SW3_3}	out_status[7:0]
2'b00	rclk_cnt[7:0]
2'b01	rclk_cnt[15:8]
2'b10	{1'bz, lost_lock2, lost_lock1, lost_lock0, 1'bz, sig_lost2, sig_lost1, sig_lost0}
2'b11	{6'bzzzzzz, dphase_lock, lvds_rxpll_lock}

Figure 5. Functions of the Connectors, Push-buttons, Switches and LEDs



Running the Demo

For this demo, you can use LVDS source or DVI source to generate video output to three ports: the DVI_Tx port, ChannelLink_Tx port and HDMI_Tx port.

Connection with the LVDS Source

If you want to use a LVDS input, you should use a VGA cable to connect a video source (such as a graphics card) to the VGA-to-DVI box, then use a DVI cable to connect the box to Video demo board #3, and finally use a MDR-26 Channel-Link cable to connect the board to the ChannelLink_Rx port of the LatticeECP3 Video Protocol Board.

Connection with the DVI Source

If you want to use a DVI input, insert the HDMI Mezzanine Card onto the LatticeECP3 Video Protocol Board, and use a DVI-to-HDMI cable to connect a video source (such as a graphic card) to the port J2 (HDMI_Rx port) of the HDMI Mezzanine Card.

Connection with the LVDS Output

If you want to use a LVDS output, use a MDR-26 Channel-Link cable to connect the ChannelLink_Tx port of the LatticeECP3 Video Protocol Board to Video demo board #2, then use a DVI cable to connect the board to a DVI sink (such as a monitor).

Connection with the DVI Output

If you want to use a DVI output, use a DVI cable to connect the DVI_Tx port to a DVI sink (such as a monitor).

Connection with the HDMI Output

If you want to use a HDMI output, use a DVI-to-HDMI cable to connect port J3 (HDMI_Tx port) of the HDMI Mezzanine Card to a DVI sink (such as a monitor).

Run

To begin this demo, power on the LatticeECP3 Video Protocol Board, Video Demo Board #2 and Video Demo Board #3, then download the bitstream file for the demo, and select the input video with a supported resolution.

If you want to use a LVDS input, set SW1_1 to ON. Now the input video should be shown on the DVI sinks. If no picture is displayed on the screen, or the quality of the picture is not acceptable, or the picture is not stable, etc., you may set SW3_4 to ON. Then you may change the four bits of the switch SW4 to select the related phase of the receiver PLL. A global reset may be helpful.

If you want to use a DVI input, you can set the all bits of the switches SW1 and SW3 to OFF. Now the input video should be shown on the DVI sinks. If no picture is displayed on the screen, or the quality of the picture is not acceptable, or the picture is not stable, etc., you may set the switch SW1_2 to ON to select the loopback mode, or a global reset may be helpful.

References

- RD1030, LatticeXP2, LatticeECP2/M and LatticeECP3 7:1 LVDS Video Interface
- RD1097, LatticeECP3 HDMI/DVI Interface Reference Design
- EB55, HDMI Mezzanine Card User's Guide

Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2010	01.0	Initial release.
February 2011	01.1	Updated introductory text.
		Updated Supported Video Formats table.
		Updated the following figures: - Block Diagram of the DVI / 7:1 LVDS Conversion Demo Setup - Data Flow Diagram - Functional Block Diagram of the Top-Level Design - Functions of the Connectors, Push-buttons, Switches and LEDs