Low-Cost Serial RapidIO to TI 6482 Digital Signal Processor Interoperability with LatticeECP3

October 2010 Technical Note TN1214

Introduction

The RapidIO Interconnect Architecture is an industry-standard, packet-based interconnect technology that provides a reliable, high-performance interconnect between NPUs (network processing units), CPUs (central processing units), and DSPs (digital signal processors). It is a switch-based interface targeted to replace microprocessor buses and has widespread acceptance in the wireless infrastructure market as the primary interconnect for DSP clusters in baseband processing for 3G, LTE, and WiMAX.

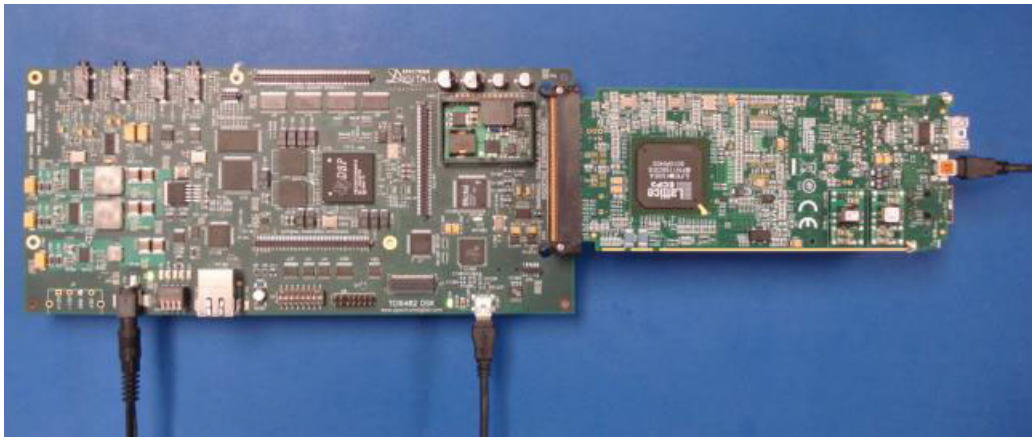
Serial RapidIO is the interface of choice for Texas Instruments (TI) DSP families, which are widely used in the wireless world. Lattice has worked to develop and demonstrate interoperability between the LatticeECP3™ Serial RapidIO IP core and the TI 6482 DSP. This technical note documents the interoperability platform and tests that have been performed.

This interoperability report is based on a single hardware setup and is not available as a distributable demo. A Lattice AMC Interface Card-based demo is available for user-based demos supporting the LatticeECP3 in loopback and/or interoperability with a third-party SRIO-based AMC card.

Interoperability Platform

The interoperability platform consists of a Spectrum Digital TCI 6482 EVM board containing the DSP and the LatticeECP3 AMC Evaluation Board. A LatticeMico32™ processor in the LatticeECP3 was utilized to initiate transactions through the Serial RapidIO IP core to the DSP as the target. The TI 6482 DSP, using Code Composer Studio, is utilized as an initiator with the LatticeECP3 device acting as the target. Figure 1 shows the hardware interoperability platform.

Figure 1. LatticeECP3 and TI 6482 Interoperability Platform



Interoperability Items

Interoperability tests were performed with different link rates, widths, and packet transfers. Operations were performed in both directions, initiated from the LatticeECP3 Serial RapidIO as well as the TI 6482.

Link Rates and Widths

- 1.25 Gbps 1x
- 3.125 Gbps 1x

- 2.5 Gbps 4x

Note: The TI 6482 implements revision 1.3 of the RapidIO specification and does not support the 2x configuration supported in revision 2.1. Therefore, 2x configurations are not covered in this interoperability report.

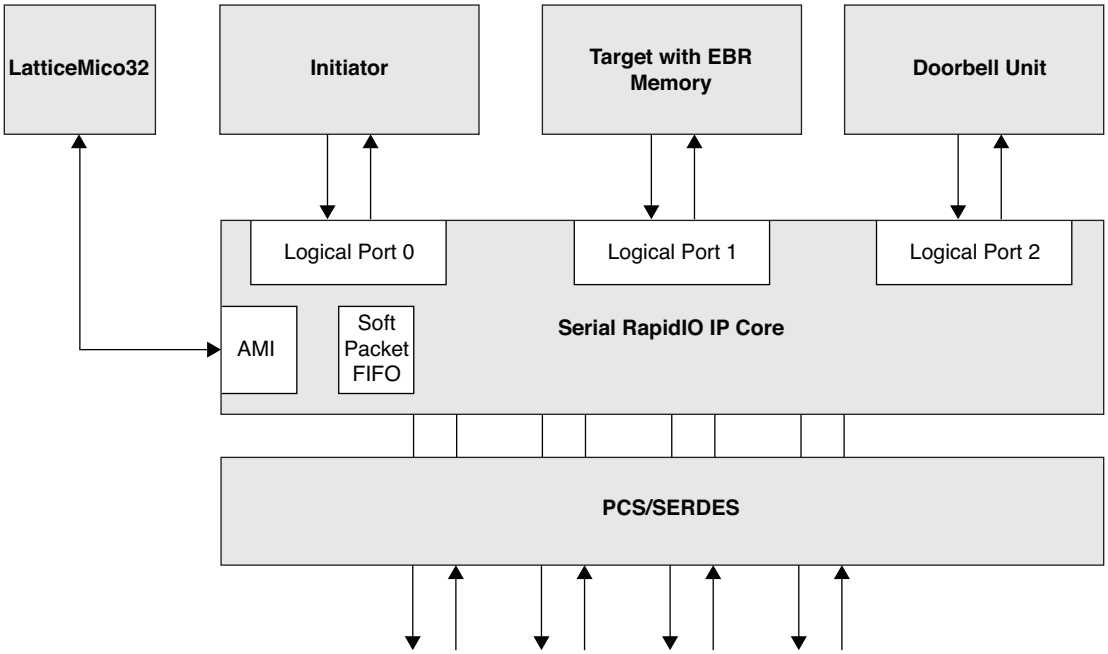
Packet Types

- NWRITE (Type 5)
- NREAD (Type 2) with RESPONSE (Type 13)
- SWRITE (Type 6)
- Maintenance (Type 8)
- Doorbell (Type 10)

LatticeECP3 Interoperability FPGA Design

A block diagram of the LatticeECP3 interoperability FPGA design is provided in Figure 2. This section provides a high-level description of each of the major blocks in the design.

Figure 2. LatticeECP3 Interoperability FPGA Design Block Diagram



LatticeECP3 Serial RapidIO IP Core

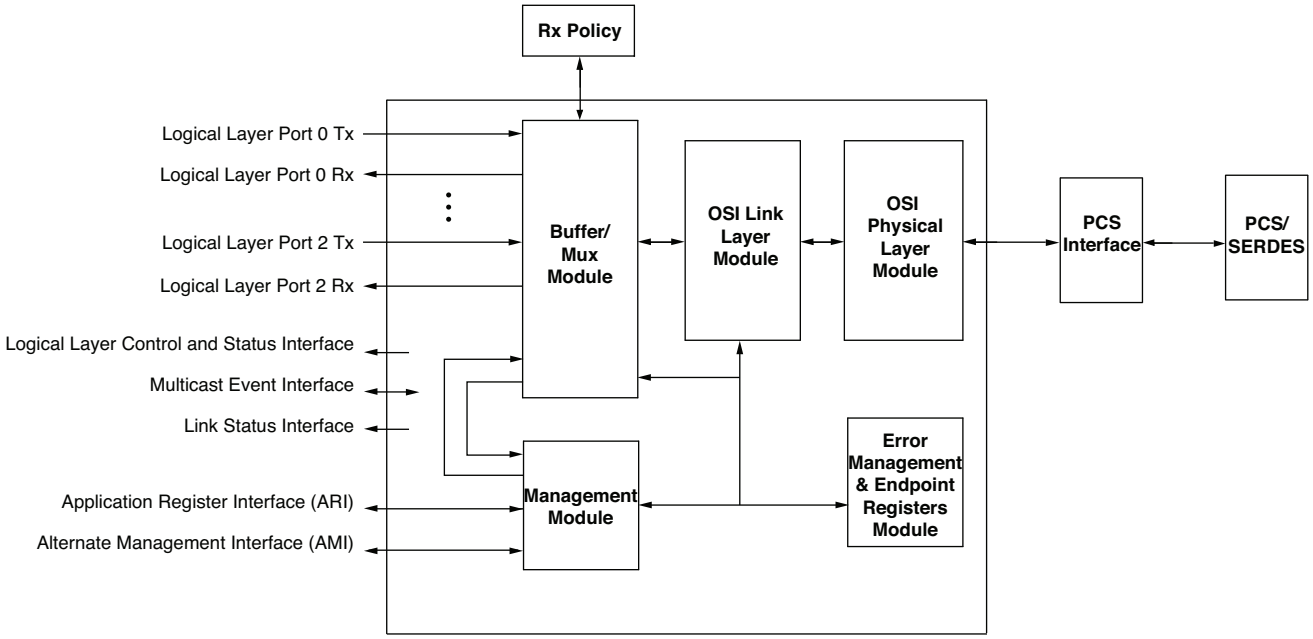
The LatticeECP3 Serial RapidIO IP core is a complete high-performance solution that implements required serial physical layer (PHY) and common transport functionality defined in the RapidIO Specification Revision 2.1. The physical layer supports the following line rate and width configurations.

- 1.25 Gbps at 1x, 2x, and 4x
- 2.5 Gbps at 1x, 2x, and 4x
- 3.125 Gbps at 1x and 2x

In addition to PHY layer functions, the IP core's Management Module supports access to Physical, Transport, and Logical Layer CSRs through Maintenance transactions or through the built-in Alternate Management Interface (AMI). The Management Module includes a Soft-Packet FIFO (SPF) which enables a processor to transmit or

receive RapidIO packets, and permits system-level testing, or easy implementation of logical layer functions in software. Figure 3 provides a block diagram for the Serial RapidIO IP core.

Figure 3. LatticeECP3 Serial RapidIO IP Core



The IP core is designed for performance and optimal resource utilization. As a result, the solution leaves many device resources available for user applications such as bridging to data plane or control plane interfaces such as CPRI or PCI Express. Further information on the LatticeECP3 Serial RapidIO IP core can be found in IPUG84, RapidIO 2.1 Serial Endpoint IP Core User's Guide.

LatticeMico32

The LatticeMico32 is Lattice's open-source soft processor. The LatticeMico32 is used to drive the control plane of the interoperability design and performs the following functions.

- Menu user interface via UART interface
- Local access of the CSR space in the Serial RapidIO IP core
- Program the initiator for memory transfer
- Send and receive doorbells
- Maintenance read and write packets through the Soft-Packet FIFO
- NREAD transactions through the Soft-Packet FIFO

Soft-Packet FIFO

The Soft-Packet FIFO consists of a transmit and receive FIFO inside the Serial RapidIO IP core. Through the AMI the LatticeMico32 can create RapidIO packets in software and then write the packet into the transmit FIFO to send over the link. In the receive direction packets can be captured in the receive FIFO and then read via the LatticeMico32. The Soft-Packet FIFO is utilized for two different functions in this interoperability test. The Soft-Packet FIFO is used to verify the TI DSP memory contents. It is also used to issue maintenance read requests to the TI 6482 to explore the CSR/CAR space of the DSP.

Initiator

The initiator block emulates the behavior of a DMA controller and generates streams of memory write request packets from the LatticeECP3 device through the Serial RapidIO IP core to the TI 6482. Using the LatticeMico32 the initiator is programmed to transmit 16 256-byte NWRITE packets to the TI 6482 L2 memory.

Target

The target block terminates read and write request packets and maps them to an on-chip 8 KB EBR memory pool.

Doorbell Unit

The doorbell unit block sends Type 10 doorbell messages when instructed by the LatticeMico32. It can also receive doorbell messages which can then be collected by the LatticeMico32.

Interoperability Tests

The interoperability tests were performed using a menu system controlled via the UART interface of the LatticeMico32. Similar tests were performed from the TI 6482 accessing the LatticeECP3 device using Code Composer Studio.

Display Link Status

This menu item displays some of the information of the physical layer link status found in Lane n Status CSR. This is performed by the LatticeMico32 reading the local CSR register through the AMI.

Display Near-End CSRs

This menu item displays the entire logical and common transport CSR space and portions of the physical layer CSRs of the LatticeECP3. This is performed by the LatticeMico32 reading the local CSRs in the Serial RapidIO IP core through the AMI.

Display Far-End CSRs

This menu item displays the entire logical and common transport CSR space and portions of the physical layer CSRs of the TI 6482. This is performed by the LatticeMico32 creating Maintenance read packets and utilizing the Soft-Packet FIFO to send these packets over the link to the TI 6482. The response from the TI 6482 is captured in the receive FIFO of the Soft-Packet FIFO and then collected by the LatticeMico32 for display on the screen.

NWRITE/SWRITE Test

This menu item uses the initiator and the Soft-Packet FIFO to perform a block memory transfer from the LatticeECP3 to the TI 6482. The LatticeMico32 first kicks off the initiator to transfer 16 256-byte NWRITE packets to the TI 6482 L2 memory space. Once complete, the LatticeMico32 uses the Soft-Packet FIFO to send NREAD request packets to the TI 6482 to verify the memory contents and confirm the memory transfer.

Doorbell Test

This menu item instructs the LatticeMico32 to program the doorbell unit to send three doorbell messages to the TI 6482. It also waits for a response doorbell message from the TI 6482 which is then displayed on the screen with the timestamp and data payload information.

References

- IPUG84, RapidIO 2.1 Serial Endpoint IP Core User's Guide
- EB44, LatticeECP3 Serial Protocol Board - Revision D User's Guide
- TMS320TCI6482 Evaluation Module Technical Reference (included in the Spectrum Digital TCI6482 EVM kit)
- TMS320TCI6482 Quick Start Installation Guide (included in the Spectrum Digital TCI6482 EVM kit)
- RapidIO The Embedded System Interconnect – by Sam Fuller published by John Wiley & Sons Ltd.
- RapidIO Specification Revision 2.1 – www.rapidio.org

Technical Support Assistance

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Revision History

Date	Version	Change Summary
July 2010	01.0	Initial release.
October 2010	01.1	Updated to show utilization of the LatticeECP3 AMC Evaluation Board.