Wake on LAN

June 2010 — Reference Design RD1096

Introduction

The Wake on LAN (WoL) is a feature that allows a load/client on a network to be turned on by a message sent via the network. The idea behind WoL is that devices on the network will consume less power in stand-by mode and only “wake up” when required, thus making the system green or environmentally friendly. Having a separate network monitor that scans network packets to look for special data sequences is required under such conditions. This reference design implements the portion that scans network packets for a special data sequence and transmits an interrupt signal to the system controller.

Overview

The green client (usually a computer) will put itself in a sleep (or hibernate) mode during inactive states. However, in order to get out of this mode, a part of the circuit must stay active to scan the network traffic for relevant packets. While listening to the network, the circuit that is awake must check the network traffic for a special packet called the magic packet. If a magic packet is received, it must further check to see if the magic packet’s content has the correct information. If the magic packet’s contents are correct, the circuit will issue an interrupt to the system controller to wake up the rest of the circuitry and get the client out of the sleep or hibernate mode.

The magic packet is a broadcast frame with a payload containing 48 ‘1’s followed by 16 repetitions of the client’s 48-bit MAC address. A sample magic packet for a client MAC address of 01-23-45-67-89-AB is given below.

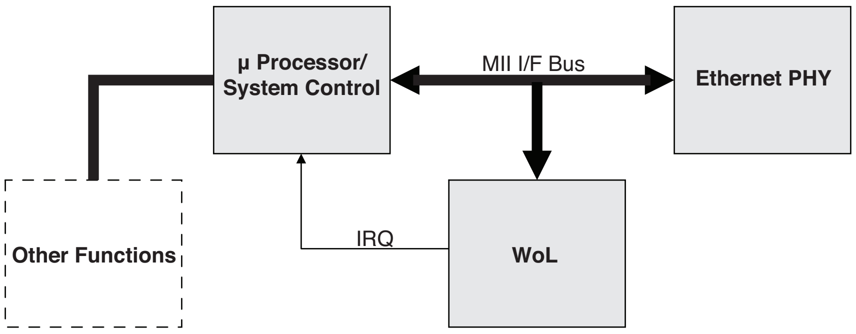
Figure 1. Sample Magic Packet

	1	2	3	4	5
FFFFFFFFFFFF	0123456789AB	0123456789AB	0123456789AB	0123456789AB	0123456789AB

6		14	15	16
0123456789AB	....	0123456789AB	0123456789AB	0123456789AB

Figure 2 shows a block diagram of a system with Wake on LAN capability.

Figure 2. WoL Capable System



Signal Descriptions

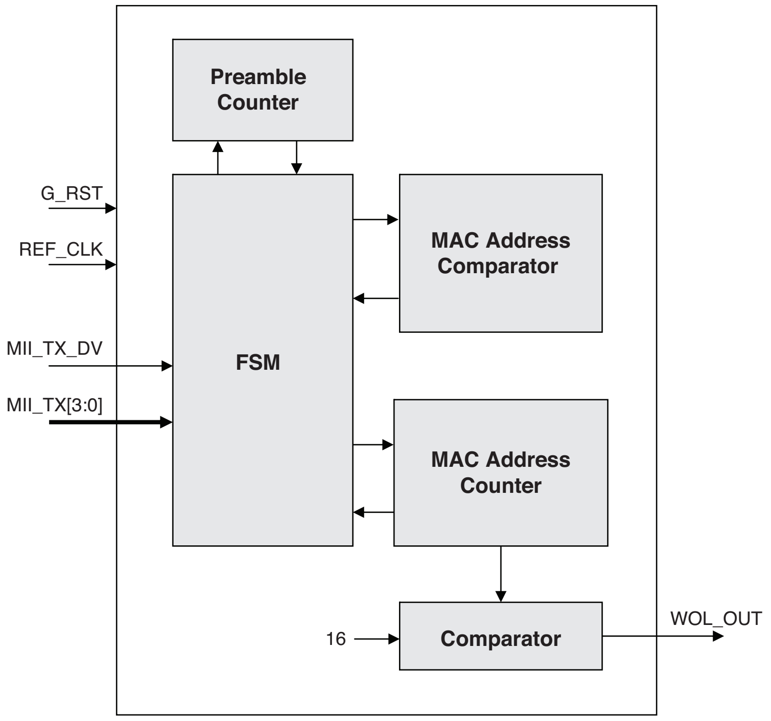
Table 1. Reference Design Signal List

Signal Name	Direction	Description
G_RST	Input	Global reset (active low)
REF_CLK	Input	System reference clock
MII_TX[3:0]	Input	Media independent interface transmit data
MII_TX_DV	Input	Media independent interface transmit data enable
WOL_OUT	Output	Magic packet found interrupt signal to system controller

Functional Description

The Wake on LAN reference design, as shown in Figure 3, sits on the Media Independent Interface (MII) bus. It monitors all packets transmitted from the Ethernet PHY. However, only the magic packet relevant to its client creates an interrupt signal.

Figure 3. Functional Block Diagram



Upon reset, the state machine monitors the data bus when the MII_TX_DV is asserted high ('1') and captures data transmitted on MII_TX[3:0]. To capture a magic packet, the state machine must capture a data sequence as illustrated in Figure 1. To do this, the state machine, upon noticing that the MII_TX_DV is asserted, captures the first four bits of data received and compares it to "1111". It does this comparison for 12 consecutive nibbles to validate the preamble stream of 48 '1's. If any nibble comparison fails, the state machine moves to the idle state.

Once the first 48 '1's are verified, the MAC address is captured nibble-wise and compared. After an entire MAC address is captured and verified, the MAC address counter is incremented by one. As illustrated in Figure 1, to ensure a true magic packet is received, 16 consecutive MAC addresses must be received after the 48 '1's. To keep track of the 16 consecutive MAC addresses a counter is employed. After 16 addresses are received, the counter comparator creates an interrupt by pulsing the WOL_OUT output for one clock period.

Assigning of the MAC address can be done in two ways:

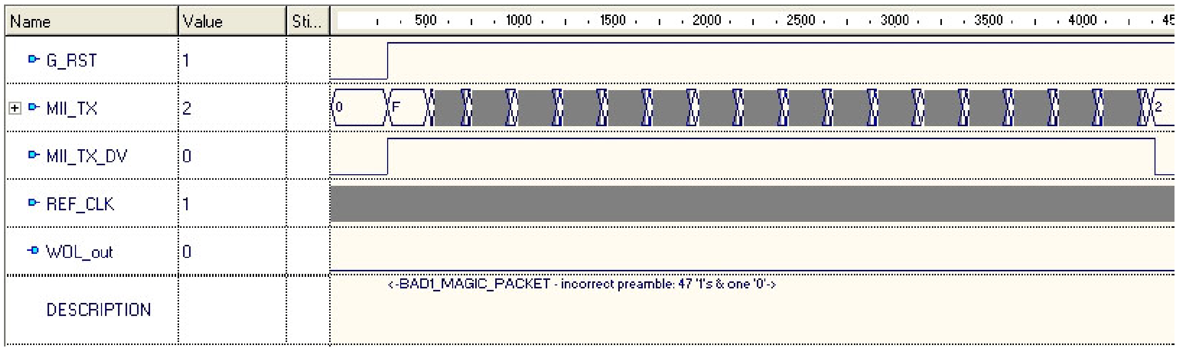
1. If a pre-assigned MAC address will be used, it should be hard-coded in the HDL, or
2. The system controller can assign the MAC address via a serial I^{2}C or SPI back-end interface during system power-up. The I^{2}C or SPI back-end interface is not implemented in this reference design. However, users can add the SPI interface using reference design RD1075, Serial Peripheral Interface, or the I^{2}C interface using reference design RD1054, I^{2}C Slave/Peripheral.

Test Bench

The test bench simulates three different scenarios. The RTL simulation results are used in the description below.

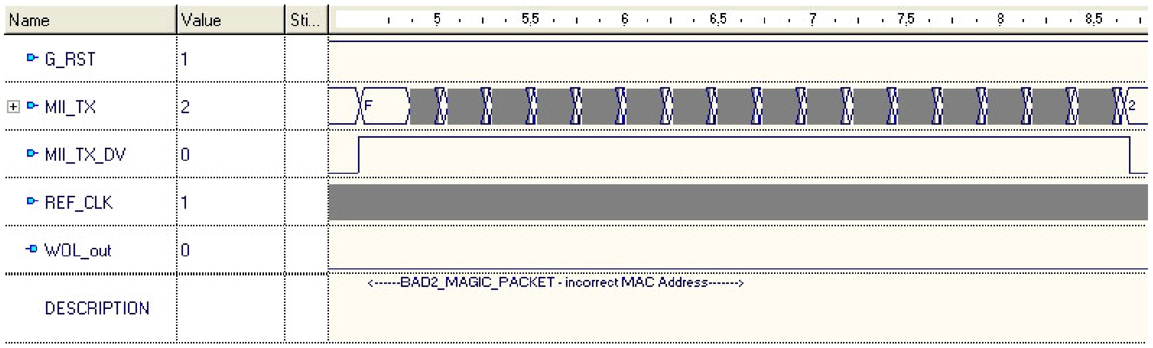
1. In the first one, the MAC address is correct but the preamble is incorrect. Instead of 48 ‘1’s, the test bench sends 47 ‘1’s followed by a ‘0’. Figure 4 is a waveform highlighting this transaction. In the test bench, this task is called bad1_magic_packet. Notice that the WOL_out interrupt signal does not get asserted.

Figure 4. Bad1 Magic Packet



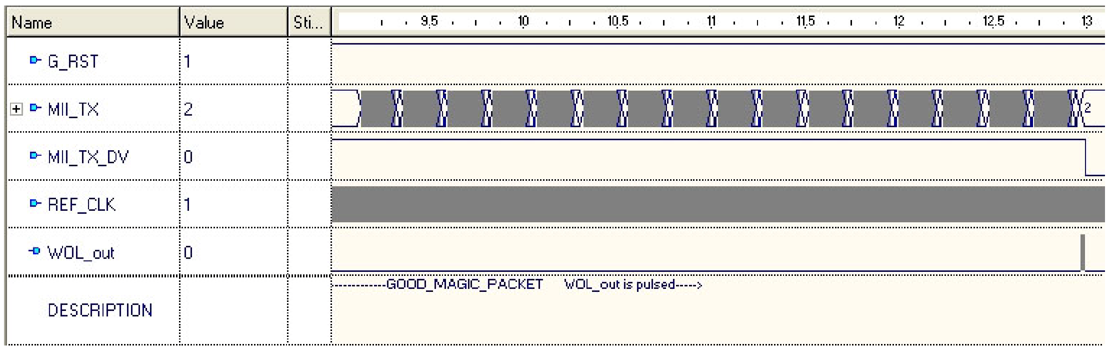
2. In the second scenario, the preamble is correct but the MAC addresses are incorrect. Figure 5 is a waveform highlighting this transaction. In the test bench, this task is called bad2_magic_packet. Notice that the WOL_out interrupt signal does not get asserted.

Figure 5. Bad2 Magic Packet



3. In the third scenario, the preamble and the MAC addresses are correct. Figure 6 is a waveform highlighting this transaction. In the test bench, this task is called good_magic_packet. Notice that the WOL_out interrupt signal pulses for one clock cycle after the correct magic packet is received.

Figure 6. Good Magic Packet



Implementation

Table 2. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization	f_{MAX} (MHz)	I/Os	Architecture Resources
ispMACH® 4000ZE[1]	Verilog	-7.5 (ns)	21 Macrocells	>80	8	N/A
	VHDL	-7.5 (ns)	22 Macrocells	>80	8	N/A
MachXO™ [2]	Verilog	-3	49 LUTs	>150	8	N/A
	VHDL	-3	47 LUTs	>150	8	N/A

1. Performance and utilization characteristics are generated using LC4032C-75T44C, ispLEVER® Classic 1.3 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMX0256E-3T100C ispLEVER 8.1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
June 2010	01.0	Initial release.