12V Hot Swap Controller with ispPAC-POWR1220AT8

April 2010 **Reference Design RD1068**

Introduction

A hot swap controller is used to limit the inrush current when a circuit board is plugged into a powered backplane. In addition, a hot swap controller may offer some or all of the following features: over-current protection (electronic circuit breaker), over-voltage protection, and under-voltage protection. Hot swap controllers are also required to isolate the board from the backplane which is useful in troubleshooting, maintenance, and upgrade activities. The power-down request may come from the backplane (remote) or an on-board switch (manual).

This document describes how a Lattice Power Manager II ispPAC®-POWR1220AT8 can be used to implement the functions required for 12V hot swap applications. This reference design is targeted to operate on the Power Manager Hercules Development Kit (PAC-POWR1220AT8-HS-EVN – Standard or PAC-POWR1220AT8-HA-EVN – Advanced).

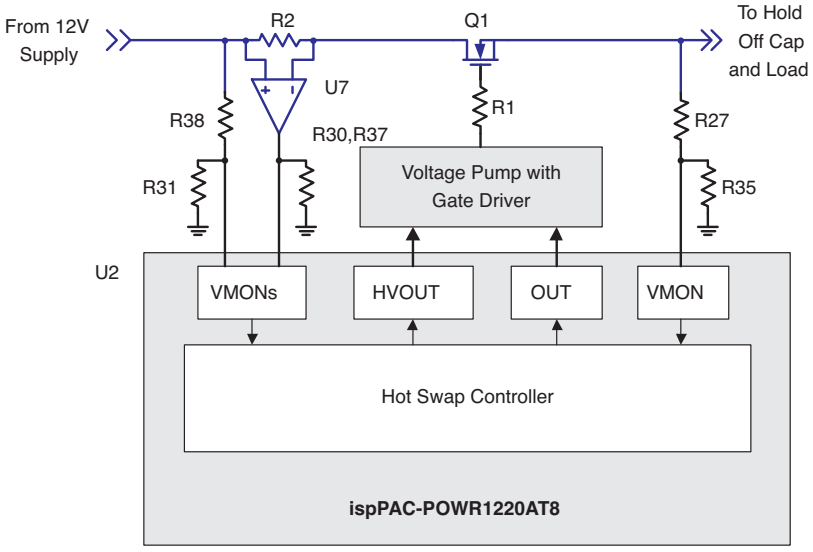
Features

- Programmable inrush current limit (default 2 amps)
- Programmable de-bounce delay (default 30ms)
- Programmable over-current limit (default 15 amps)
- Over and under-voltage limits both at source and load
- Short circuit protection
- Programmable SOA drive of N-channel MOSFET
- Power supply OR'ing

Functional Description

Figure 1 shows the top level view of the 12V Hot Swap design. Q1 is a power N-MOSFET that functions as the 12V power switch; when it is on, 12V is supplied to the board and when it is off the board is disconnected from the 12V source.

Figure 1. 12V Hot Swap Block Diagram



R2 is a current shunt that senses the 12V current. The small voltage drop across R2 is amplified by U2 and converted into a current. This output current returns to a ground referenced voltage as it passes through resistors R30 and R37. Thus, the amplifier U7 combined with appropriate values of resistors generates a voltage that can be read by the ispPAC-POWR1220AT8 VMON input that is proportional to the 12V current.

Resistor dividers (R38:R31 and R27:R35) are used to reduce the 12V to a safe level for the ispPAC-POWR1220AT8 VMON inputs. One divider is used to sense the 12V level at the source and the second divider is used to sense the 12V level on the load side of Q1. The divider ratio is 4:1 such that a 12.0V level will read 3.0V at the VMON pin. The exact value of the lower resistor takes into account the parallel loading of the VMON input impedance.

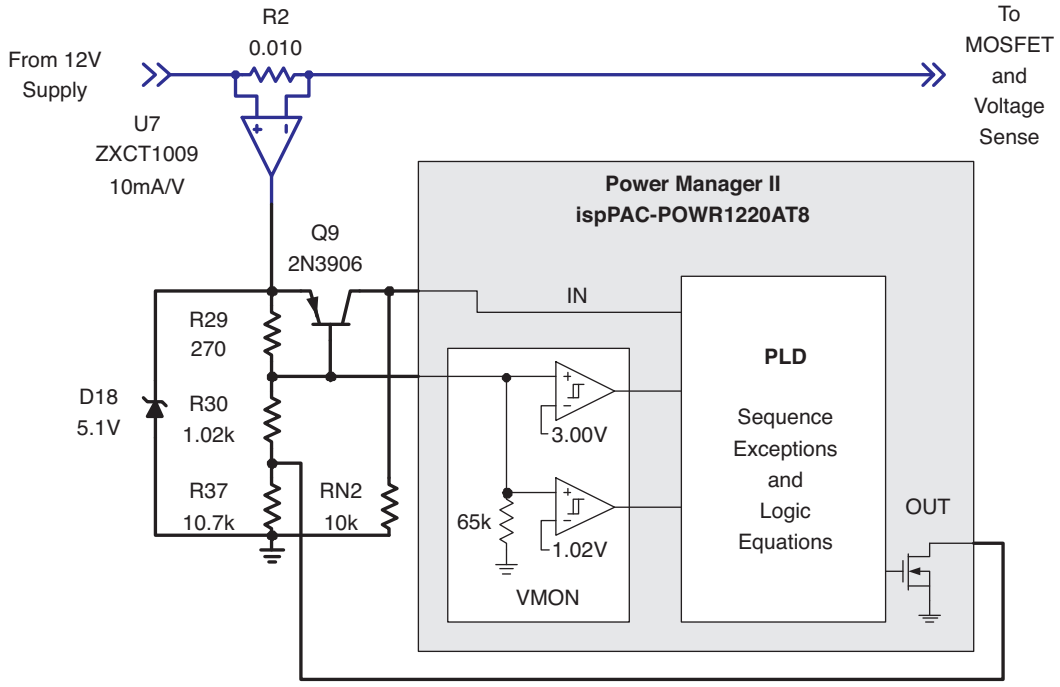
Q1 must be fully turned-on in order to minimize the voltage drop from drain to source. This means the gate voltage needs to be driven to a level of about 18V. This will assure there is enough gate-to-source bias on top of the 12V level of the source and load. As the HVOUT pins can only drive to 12V (10V for non -02 devices) a voltage-pump circuit is used to generate the 18V. This circuit essentially adds the HVOUT voltage to the incoming 12V, minus a few diode drops, to provide the roughly 18V required to bias on Q1.

The Hot Swap Controller is implemented in the PLD portion of the ispPAC-POWR1220AT8 and provides many functions. First and foremost is the hysteretic control of Q1 to limit the inrush current. A feedback loop is used to control Q1 based on the current sensed in R2. The limits in this loop are adjusted dynamically to operate the power MOSFET Q1 within its safe area (SOA). Additional limits on the current sensed in R2 are used for over-current protection or an electronic circuit-breaker.

Design Description

Figure 2 provides complete details of the 12V current monitor circuit. The significant change from the block diagram of Figure 1 is the string of resistors and components driven from the output of the amplifier U7. Starting on the left, the Zener diode D18 protects the inputs of the ispPAC-POWR1220AT8 from voltage spikes that may result from current or voltage spikes on the 12V supply.

Figure 2. 12V Current Monitor Circuit



R29 and Q9 provide an over-current signal that is routed to a digital input to provide a faster response than the VMON path. One of the 10k resistors in the array RN2 provides a pull-down on the over-current input. When the

current through R29 is about 2.6mA there is enough voltage to bias the base-emitter junction of Q9 to turn it on and present the voltage at the emitter to the over-current input. In all cases, this voltage will be enough to register as logic high at the digital input of the power manager. Using the gain of amplifier U7 (10mA/V) and the sense resistor R2 value, this corresponds to an over-current threshold of 25.9 Amps on the +12V supply. Other current limits are provided in Table 1 for some common values of R2 and R29. Or can be calculated using Equation 1.

Table 1. Over Current Limit for Common Resistor Values

I-Limit	R2		
R29	0.005	0.01	0.02
50	280	140	70
100	140	70	35
150	93	47	23
220	64	32	16
270	52	26	13
330	42	21	11
390	36	18	9
470	30	15	8
510	27	14	7
630	22	11	6
680	21	10	5
720	19	10	5

$$I_{LIM} = \frac{0.7}{(R29 * R2) * 0.01} \quad (1)$$

The bottom resistors R30 and R37 combined with the two VMON trip points provide four separate current limits for the hot swap controller. The open drain output of the ispPAC-POWR1220AT8 is used to short out R37 to change the scale of the current sensing circuit about 10:1. Both R30 and R37 take into consideration the parallel path of the VMON input impedance for the purpose of calculating the current limit.

The initial conditions for hot-swap control uses both R30 and R37 in series to sense the +12V in-rush current. The effective impedance to ground at the VMON input results in 9930 ohms. When this impedance is combined with the gain of the amplifier U7 and the value of the sense resistor R2 the resulting VMON voltage is about 1V per Amp. Thus, the lower trip-point of 1.02V corresponds 1 Amp and the higher 3.00V trip-point corresponds to 3 Amps on the +12V supply. Initially, when the voltage drop across Q1 is high, the lower trip-point is used in the hot-swap control to limit the current to 1 Amp. After the load capacitance has charged for some time, the voltage drop across Q1 is less and the hot-swap controller uses the upper trip-point to limit the current to 3 Amps. This does several things; 1) minimize the time that Q1 is in the switching transition to lower the power dissipated, 2) provides a quicker hot-swap, 3) operates Q1 within the SOA.

After the hot-swap is complete and the load is resting at +12V, the lower resistor in the current sense circuit is shorted out by the open-drain output. The effective impedance to ground at the VMON input is 1004 ohms. When this impedance is combined with the amplification of U7 and the sense resistor R2 the resulting VMON voltage is about 1V per 10 Amps. The two VMON trip-points now provide over-current detection at 10 A and 30 A respectively.

This design is easily modified to address a variety of loading and current limit settings. Simply changing the resistor values and VMON trip-points allows the designer to customize this design for any particular application. Table 2

provides several example values for reference or Equation 2 can be used to calculate the current limit. The value of R in the parenthesis represents either R30 in high current mode or the sum of R30 plus R37 in low current mode.

Table 2. High and Low Current Limits for Common Resistor Values

R2	R30	R37	Current Limit		
			Low (A)	VMON (V)	High (A)
0.005	1020	10.7k	3	1.5	30
0.005	1020	1020	15	1.5	30
0.010	1020	10.7k	1	1.0	10
0.010	1020	1020	5	1.0	10
0.020	1020	10.7k	1	2.0	10
0.020	1020	1020	5	2.0	10

$$I_{LIM} = \frac{VMON}{0.01 * R2 * \frac{1}{\left(\frac{1}{R} + \frac{1}{65000}\right)}} \quad (2)$$

Figure 3. 12V Voltage Monitoring Circuit

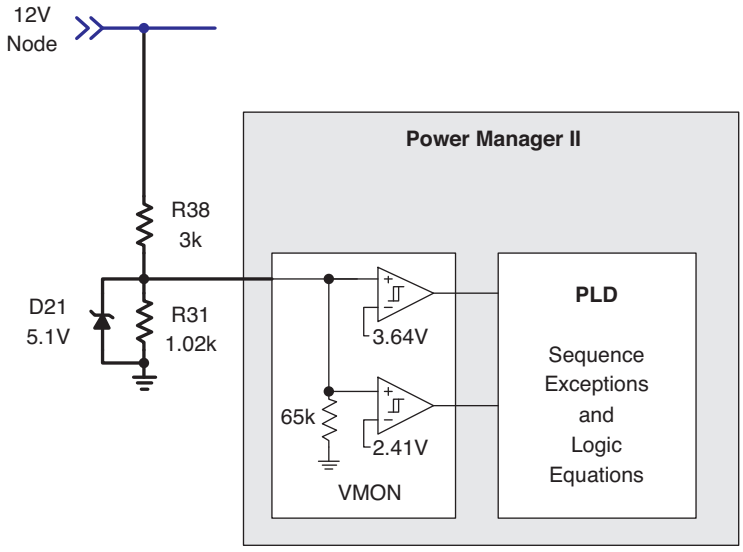


Figure 3 shows the details of the voltage monitoring circuit for the 12V nodes. The lower resistor in the divider has the value of 1020 ohms so that the parallel impedance at the VMON input is about 1k. This forms a very nice 4:1 divider. The upper and lower VMON trip points correspond to a voltage range of 14.4V to 9.6V or 12V +/- 20%.

The next circuit block from Figure 1 to discuss is the Voltage Pump with Gate Driver. This circuit provides the means to generate a voltage high enough to turn on the N-Channel MOSFET Q1. Figure 4 shows the details of this circuit. The HVOUT of the Power Manager is programmed to oscillate at about 22kHz swinging from zero to 10V with about an 80% duty cycle. When the HVOUT is low, D1 charges C1 to 11V from the 12V supply; shown by the voltage markers under C1. When HVOUT is high the voltage across C1 is elevated to 10V and the resulting voltage at the emitter of Q2 is 21V as shown by the voltage markers above C1. The 21V can now bias on Q2 and D2 to charge up C2. Q2 is a bipolar PNP that functions as a voltage controlled rectifier. It only passes current when the emitter is higher than the 12V supply. After several cycles from HVOUT the voltage on C2 will be enough to bias the gate of Q1 to turn it on. The resistor R3 is located close to the gate of Q1 to prevent parasitic oscillations on Q1.

The resistor R2 slowly drains the voltage on C2 when the HVOUT oscillation is stopped: in situations such as in-rush current limiting or SOA control. To quickly turn Q1 off and isolate the 12V supply from the load, Q3 is biased on to bring the voltage on C2 to ground. The open drain output (Fast Shut Down) of the Power Manager and the pull-up resistor R4 are used to control Q3.

Figure 4. Voltage Pump Circuit

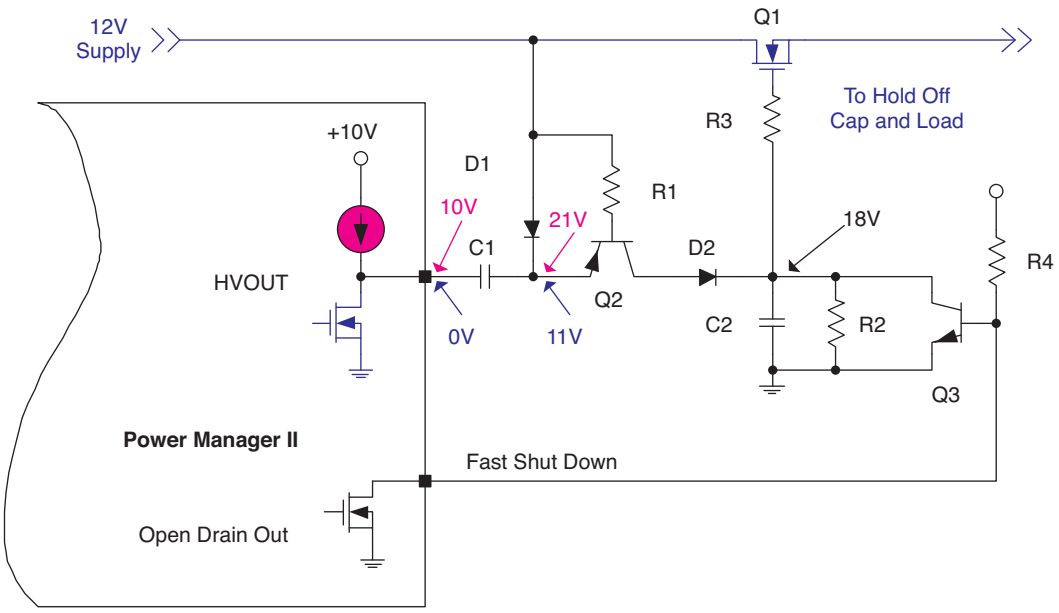
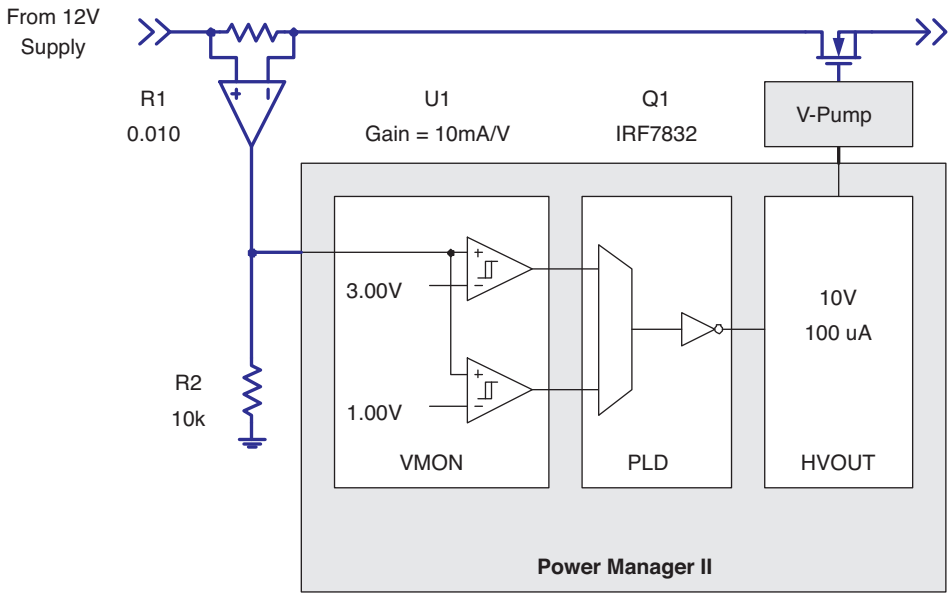
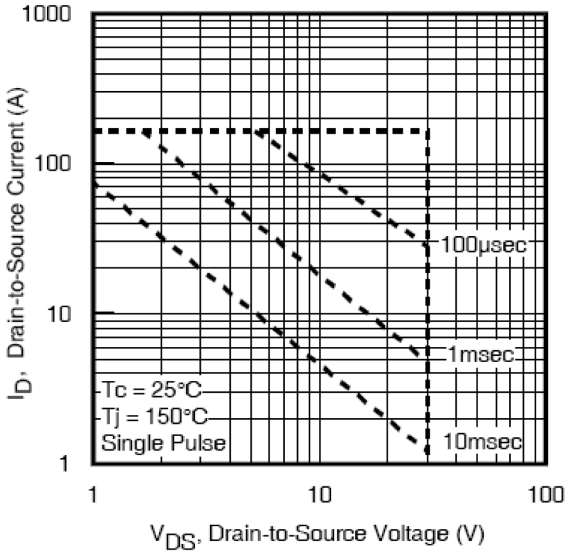


Figure 5. Hysteretic Current Control for 12V



For 12V hot swap control of the in-rush current a hysteretic circuit is used with two current settings. The initial current limit is 1A set by the lower VMON in Figure 5. After the MOSFET has turned on and the voltage across it is only around 4V to 5V the current limit can be increased to 3A by using the upper VMON. This keeps the power dissipated in the MOSFET to a minimum and operates it in the SOA. The SOA curve for the MOSFET use in this design is shown in Figure 6 overlaid with the current limits of 1A and 3A.

Figure 6. Safe Operation Area for MOSFET



Listing 1. LogiBuilder Sequence

```
// Reset, turn off Power Good LED and disable the charge pump.
// Set the current mode to Low, turn off the redundant supply
// MOSFET Q2, and wait for AGOOD (internal calibration)
// and the input voltage to reach 9.6V.
Step 0    Wait for  AGOOD AND INPUT_12V_MIN
           OUT10_LowCurrent_ENA = 1,
           OUT11_Shut_12V_Down = 1,
           Out12_PRI_12V_OR = 1,
           PWR_GOOD = 1

// Delay to allow for contact or connector bounce.
Step 1    Wait for 53.25ms using timer 3

// Enable the 12V charge pump and turn the Power Good LED on.
Step 2    OUT11_Shut_12V_Down = 0, OUT15_PWR_GOOD = 0,

// If load side of MOSFET does not reach 9.6V in 15ms
// there must be a problem, so shut down.
Step 3    Wait for  HS_12V_HIGH or 15.36ms using timer 1;
           on timeout Goto 7

// Switch the current sense to High Current mode.
Step 4    OUT10_LowCurrent_EN = 0, OUT12_PRI_12V_OR = 0

// Wait for final charging of hold-off cap and
// Current Mode change-over to settle.
Step 5    Wait for 15.36ms using timer 1

// Hot Swap Complete: wait for a fault to occur.
Step 6    Wait for  NOT INPUT_12V_OK OR V10_12V_CURRENT_HIGH
           OR IN2_Over_Current_12V
```

```
// Target step for shutdown branch.
Step 7    Begin Shutdown Sequence

// Turn off the 12V and the Power Good LED.
Step 8    OUT11_Shut_12V_Down = 1, OUT15_PWR_GOOD = 1,

// End of program.
Step 9    Halt (end-of-program)
```

Listing 2. Supervisory Logic

```
// Internal Node used to extend the duration of the low
// portion of the charge pump oscillation.
EQ 0:    Extend_T2_TC.D =  TIMER2_TC

// Charge pump oscillator with feedback from internal node
// 32us high 8us low (25kHz).
EQ 1:    TIMER2_GATE.D =  NOT Extend_T2_TC

// Charge pump output control provides soft start.
// Output is based on 25kHz oscillation AND
// SOA-control (if the load voltage under 6V use 1A current limit)
// (if the load voltage is over 6V use 3A current limit)
// (if the load voltage is over 9.6V no current limit)
EQ 2:    HV1_Charge_Pump.D =  NOT Extend_T2_TC AND
          (( NOT HS_12V_LOW AND NOT V10_12V_CURRENT_LOW ) OR
           ( HS_12V_LOW AND NOT V10_12V_CURRENT_HIGH ) OR
             HS_12V_HIGH )
```

Simulation and Verification

The value of Timer 3 is reduced from 53.25 ms to 5.12 ms to reduce the simulation time. In Figure 7 the hot swap sequence and supervisory equations are simulated showing the low current and high current hysteretic control around 10,000 µs. In Figure 8 an over-current situation is simulated which results the shut-down sequence.

Figure 7. 12V Hot Swap Simulation

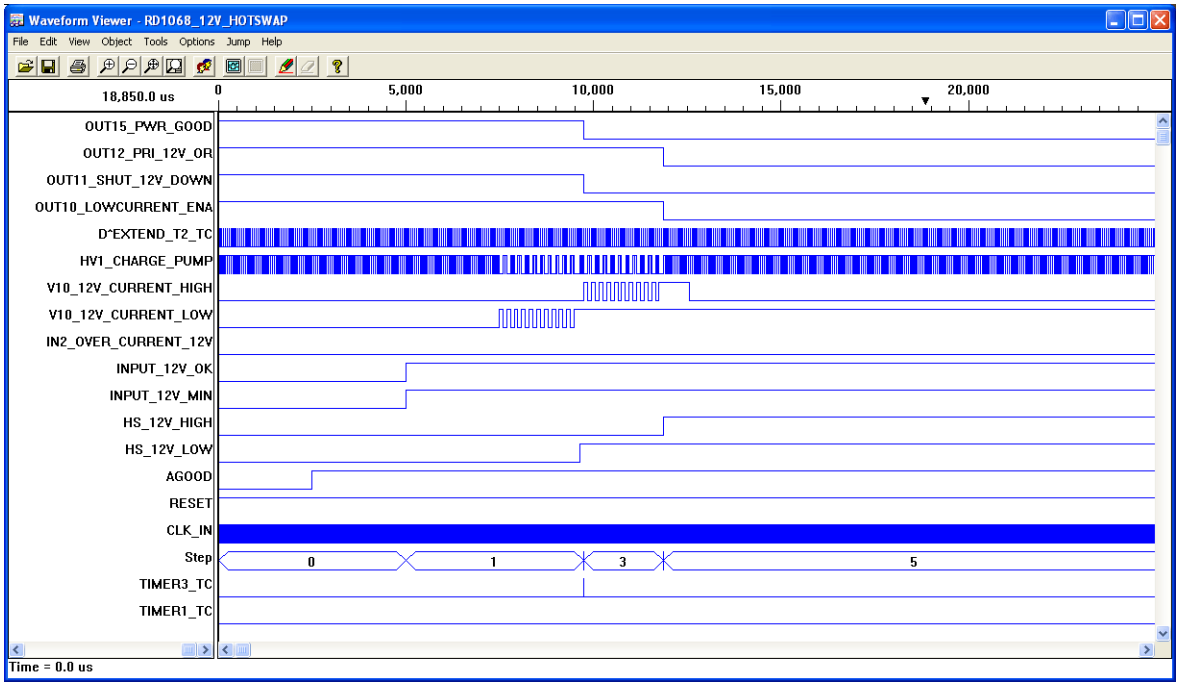
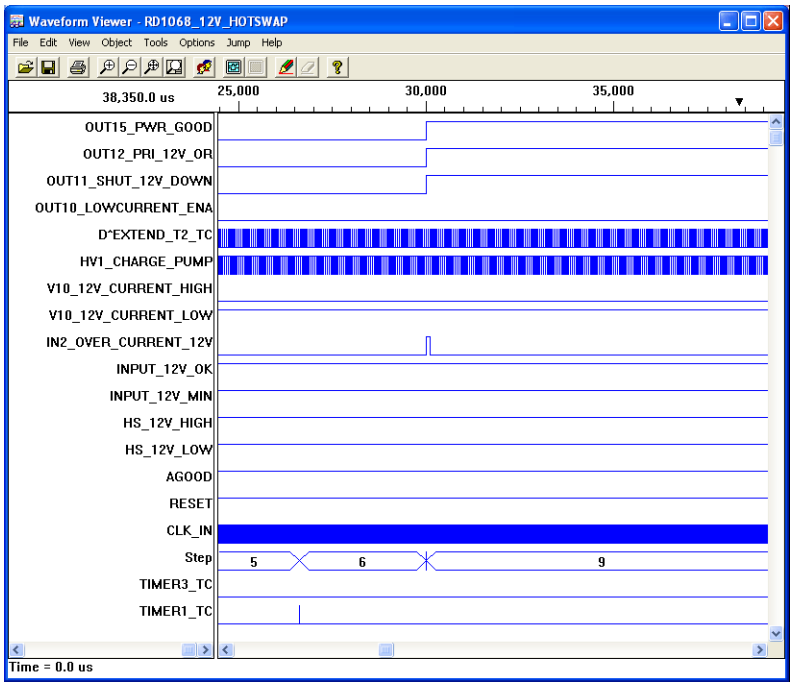


Figure 8. 12V Over-Current Simulation



Implementation

Table 3. Resource Utilization[1, 2]

Device	Macrocells	Product Terms	VMONs	In	Out	HVOUT	Timers
ispPAC-POWR1220AT8	14	57	3	1	1	1	3

1. Resource utilization characteristics are generated using PAC-Designer 5.2 software. When using this design in a different device, utilization characteristics may vary.
2. The number of VMONs, Outputs, Inputs, and Timers listed in the table are those used in the reference design. The remaining VMONs, Outputs, Inputs, and Timers are available for customer use though some may have labels assigned in the reference design.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2010	01.0	Initial release.

Appendix A. Schematic

The schematic in this section provides an example of how the ispPAC-POWR1220AT8 device should be connected in a typical system. It also demonstrates a typical example of how the current sense and voltage divider networks function and should be arranged.

On sheet 1 of the schematic the ispPAC-POWR1220AT8 device is shown. Note how the VCCA and VCCD pins have been tied together on this board and that the VCCPROG pin is left unconnected as recommended in the data sheet. The VCCPROG pin should only be connected if it is desired to program the ispPAC-POWR1220AT8 device when VCCA and VCCD are not powered up. Also note that the RESETB pin is left unconnected as it should be except when cascading two or more POWR1220AT8 devices.

The pull-up resistor sizes for the I^2C connection (SCL & SDA) are adequate for an application where there is only one or two other devices connected and the PCB run length is not excessive. If these conditions are not met then the pull-up resistors may need to be stronger (lower resistances). This is also true for the pull-up on the TMS pin and the pull-down on the TCK pin.

Sheet 2 of the schematic shows the current sense and voltage divider circuits. The voltage dividers use a 3k and 1k resistor circuit to ground to sense the 12V supply. This divider circuit is required to keep the voltage input at the VMON input below the data sheet recommended operating condition limit of 5.9V at the input pin. For this circuit the VMON input will see approximately 3V since three-fourths of the total voltage drop will be across the 3k resistor. It is good design practice when connecting to voltages that can exceed the operational specifications of the Power Manager II to use a Zener diode as shown in the schematic (with a Zener voltage of 5.1V) connected between the VMON input and ground to protect the VMON input from surges or voltage spikes. For more information about this type of circuit see application note AN6041, Extending the VMON Input Range of Power Manager Devices.

Also shown on sheet 2 is the current sense circuit. A shunt resistor, R14, is added to the main power supply to monitor the current flowing. This resistor should be kept small to prevent a power loss that would affect the operation of the system. For this design a 0.01 ohm, 3 watt resistor is used. In order for the voltage sensing to be detected by a VMON input of the Power Manager II device it must be amplified. This design uses a high-side current monitor, U2 in the schematic. This device creates a current output that is proportional to the input voltage, in this case the voltage across the shunt resister. The current passes through three resistors in series to produce a voltage level that the VMON input can sense. One of the voltages created is used to drive a digital input of the Power Manager, IN3. This input is used to sense an over-current condition and provide a fast shut-down of the MOSFET circuit (Q1 & Q2) using the output OUT3. The VMON and digital inputs are both protected by a Zener diode as mentioned above.

The current monitor output produces a voltage drop across resistors R24 and R25 which generates the input for the VMON. The two resistors are used in series to generate two different trip points depending upon the where the system is operating. Initially, when the card is first powering up the current is limited to approximately 1.5 amps by the trip point in the VMON and the hysteretic and SOA control of the MOSFET driver circuit (see Equation 2 of the Supervisory Equations). Once the voltage across the MOSFETs drops the trip point is changed and the current is limited to approximately 3 amps. During this phase the current is passing through both resistors R24 and R25.

The Tranzorb D22 on the 12V supply protects the hot-swap circuitry both from spikes on the supply and from any inductive spike that might result from quickly turning off the 12V load. The 10V Zener diode on the Charge_Pump node protects the HVOUT of the ispPAC-POWR1220AT8 from both voltage spikes on the input 12V and marginally high 12V supplies.

After the 12V supply reaches approximately 9V (determined by the SOA_LEV_2_9V trip point setting of 2.254V) the start-up phase is considered to be completed and the current limit is raised to 15 amps by driving low the digital output OUT4, which will ground that point of the circuit effectively removing R25 from the circuit. At this time the circuit is considered to be in an operational state and the remaining functions become active as determined by the sequence control.

When the Power Manager II commands a power supply to turn on it will drive the output low and base of the transistor will also be pulled down. This will decrease the base-to-emitter voltage to a zero thus turning off the transistor and creating an open on the power supply inhibit pin and turning On the power supply. For more information about this type of circuit see application note AN6046, Interfacing Power Manager Devices with Modular DC-to-DC Converters.

Figure 9. Power Manager POWR1220AT8

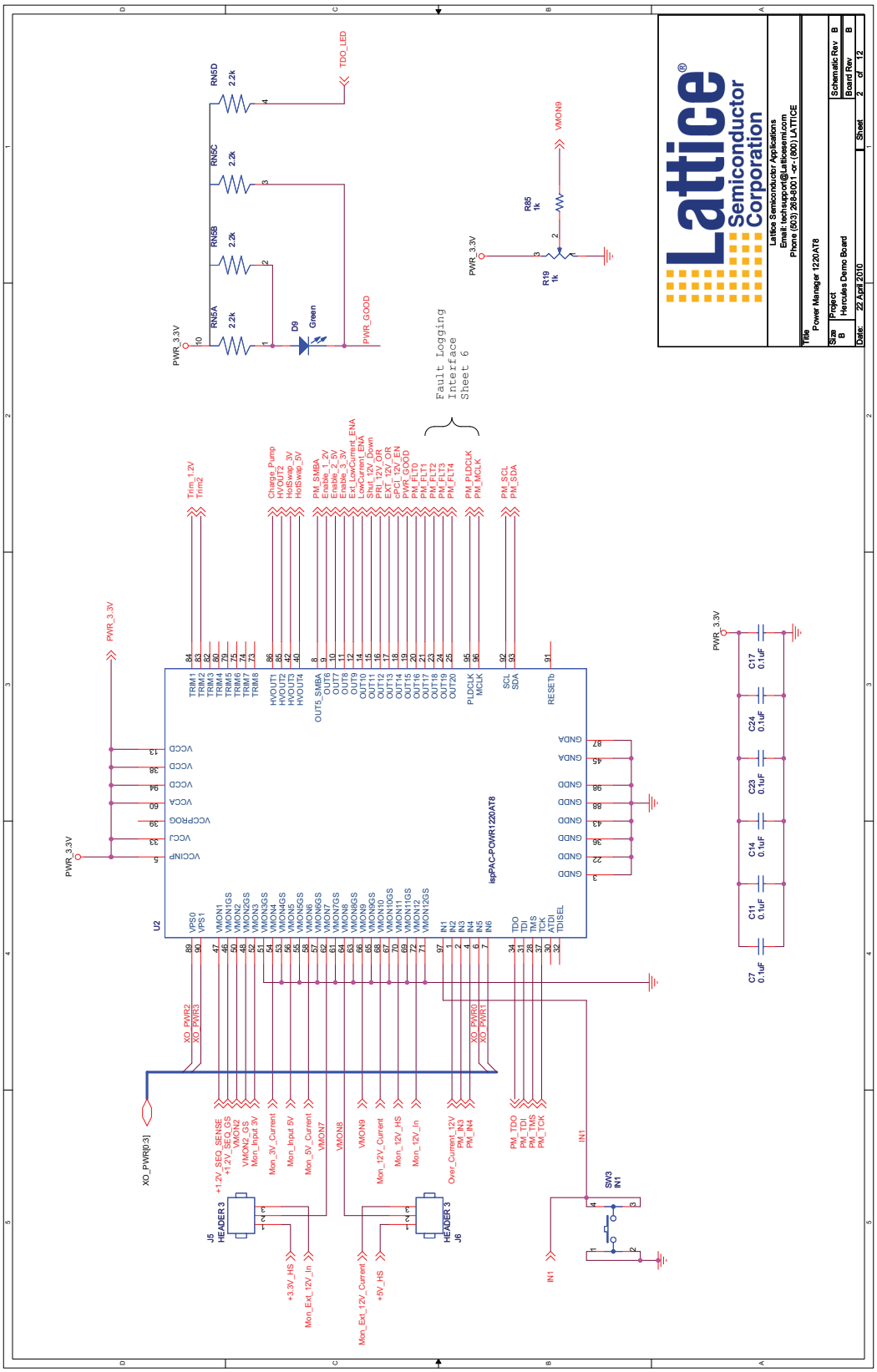

Figure 10. Hot Swap 12V