AMC Module Power Management

April 2010 **Reference Design RD1070**

Introduction

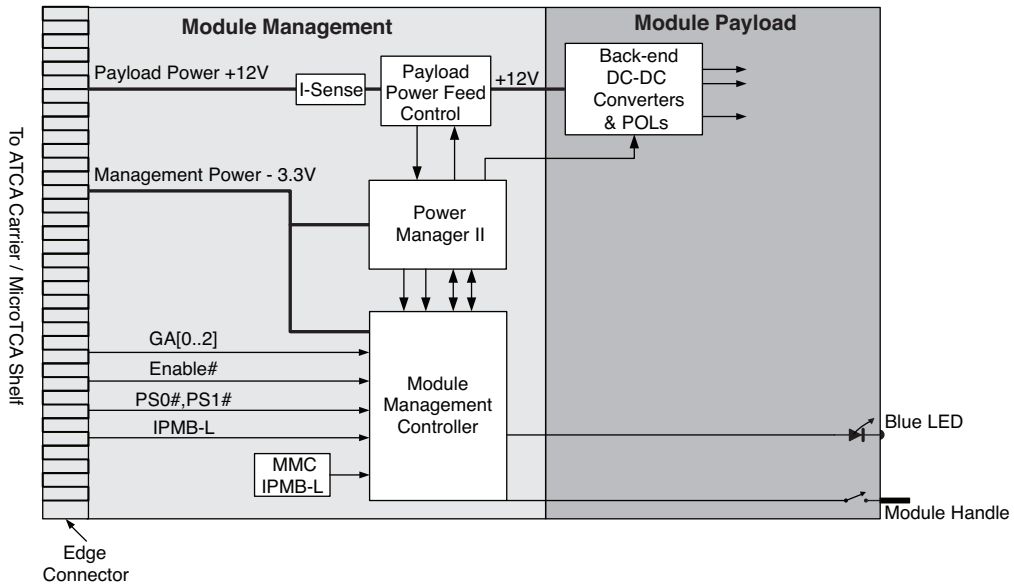
This reference design describes the use of a Lattice Power Manager II device as a Payload Power Management Coprocessor in an Advanced Mezzanine Card (AMC) system. The Advanced Mezzanine Card is intended to be plugged into a carrier system, either a card or a shelf, and supports the hot swapping of the Mezzanine card in the carrier system without affecting the operation of the host carrier system. The electrical and mechanical specifications for the AMC system are specified by the PICMG 3.0 subcommittee, AMC.0 R2.0.

The AMC specifications incorporate a system management section that is an extension of the hierarchical ATCA (Advanced Telecommunication Computing Architecture) shelf management scheme. A processor in the Mezzanine card module management section, called the Module Management Controller (MMC), sends the details of the payload circuitry along with the power requirements to the host system processor and also receives commands from the host system processor. The system uses a payload power rail (+12V) and a management power rail (+3.3V) so that when the AMC module is plugged in, only the module management section is powered on. When the MMC receives the command from the host system processor it will then turn on the payload power rail and the AMC card will become active in the system.

By using a Lattice Power Manager II device as the Payload Power Management Coprocessor, the design of the MMC can be simplified since it is used to supply the Module Management section functions which are defined by the AMC.0 R2.0 specification. The Power Manager II device can provide the monitoring and control functions of the payload power supplies and provide this information to the MMC over an I^2C link and several status signals.

A block diagram of the AMC card using the Power Manager II device is shown in Figure 1.

Figure 1. Block Diagram of AMC Card Using the Power Manager II



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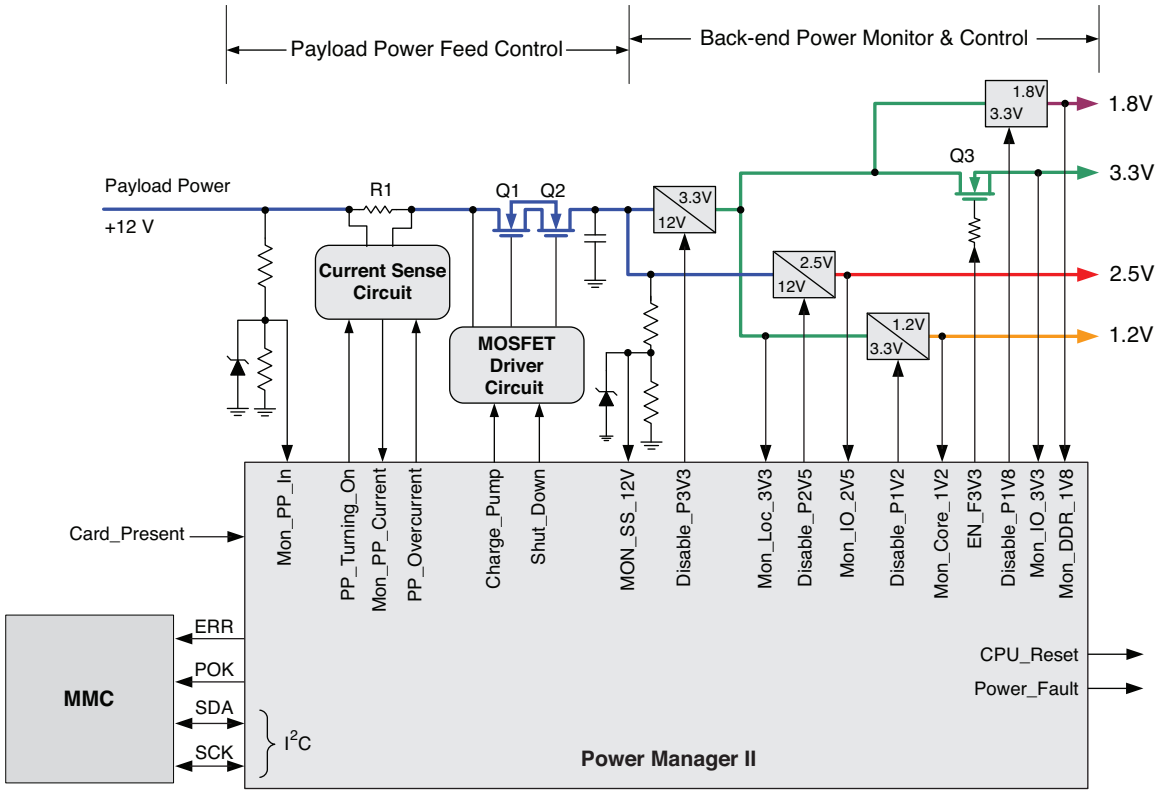
Features

- 12V hot swap controller
  - Operate MOSFETs in Safe Area of Operation (SOA)
  - Provide over-current and short-circuit protection
  - Programmable SOA and over-current levels
- Six supply monitors
  - 3.3V I/O, 2.5V, 1.8V, and 1.2V monitors
  - Two unassigned VMON inputs available to the user
- CPU reset
- Power fault output
- I^2C interface between the MMC and the Power Manager II

Functional Description

A block diagram of the AMC card Power Manager II is shown in Figure 2.

Figure 2. AMC Card Power Manager II Block Diagram



This reference design provides the hot swap function required for the AMC card. The MMC will send a command across the I^2C bus to the Power Manager II to tell it when to turn on and off the power supplies. In addition to the I^2C interface there are two status outputs from the Power Manager II to the MMC: POK and ERR. When the AMC card is removed the 12V supply is normally shut down by a command from the MMC prior to removal of the card to reduce the possibility of arcing on the card connectors. The Card_Present input is also used to detect when the card has been inserted or removed from the shelf or host and will cause the 12V supply to be shut down when not present.

The 12V supply line has a small series resistor (R1) to monitor the current and two N-channel MOSFETs (Q1 & Q2) to switch the voltage to the load. The Q1 MOSFET is used to turn on and off the 12V power rail to the card. The Q2 MOSFET is used to prevent reverse current flow from the capacitor back to the supply rails when the AMC card is being powered down.

The voltage across the current shunt is amplified in the Current Sense circuit so that the VMON input can sense the value. An output (PP_Turning_On) is used to change the range of the Current Sense circuit so it can be used during both start-up and normal operation. There is a discrete input (PP_Overcurrent) from the Current Sense circuit in addition to the VMON input (MON_PP_Current) which is used to measure current. The discrete input is used to provide a fast indication of over-current and immediately shut down the MOSFETs (Q1 & Q2). The fast shut down is accomplished by an output (Shut_Down) to the MOSFET Driver circuit which turns off both MOSFETs (Q1 & Q2).

The 12V supply voltage is sensed both before and after the MOSFETs (Q1 & Q2) with VMON inputs of the Power Manager II. The VMON inputs are labeled Mon_PP_In and Mon_SS_112V in Figure 1 and both require a resistor divider network to keep the voltage at the VMON input within the device specifications. The Power Manager II PLD contains the sequence that enables the hot swap functions.

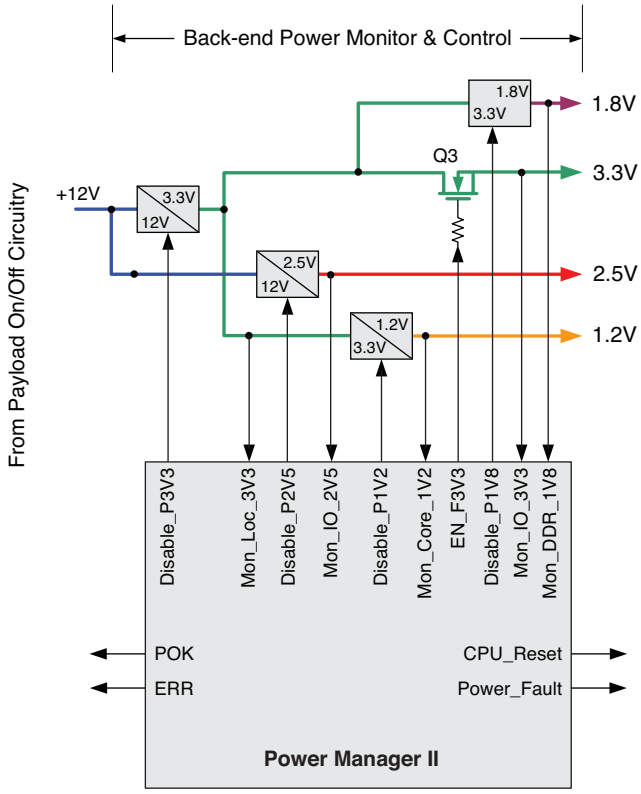
See Appendix A for a schematic diagram and detailed discussion of the current sense and voltage divider circuits.

The PLD also implements the logic for hysteretic and SOA control of the MOSFETs (Q1 & Q2) and short-circuit detection. When the voltage drop across the MOSFETs (Q1 & Q2) is large (initial turn-on) it is controlled using the SOA mode of operation. When the voltage drop across the MOSFETs (Q1 & Q2) is relatively small it is no longer under SOA control and is turned on fully. If the 12V supply does not reach 9V within 8 ms then the MOSFETs (Q1 & Q2) are turned off and the system awaits a restart command from the MMC.

The circuit and logic used to implement the hot swap functions is discussed in more detail in RD1068, Power Feed and Hot Swapping 12V Supplies with Power Manager.

The back-end Power Monitor and Control functions are shown in Figure 3. There are two power supplies which use 12V as a source; a 3.3V and a 2.5V supply. The 3.3V is used to supply two additional power supplies; a 1.8V and a 1.2V supply. A MOSFET (Q3) driven by HVOUT2 of the Power Manager II is used to isolate and sequence a 3.3V I/O supply. Each of the power supplies and the 3.3V I/O supply are monitored by VMON inputs.

Figure 3. AMC Card Power Manager II Back-end Power Monitor and Control



Design Description

Once the AMC card has been plugged into the host or shelf, the Power Manager II resets the output signals and insures that all the power supplies are turned off. Then it waits for the analog circuitry check to pass which is indicated by AGOOD being asserted and for the MMC to set the Turn_On_Payload input via the I^2C bus. When the Turn_On_Payload input is asserted, then the Power Manager II begins to turn on the 12V supply through the MOSFETs Q1 and Q2. This is accomplished by turning on the Charge_Pump output which is HVOUT1 in this design. The supervisory equations accomplish the task of keeping the MOSFETs in the SOA by limiting the current in each phase of the start-up. If an over-current is detected the output will be turned off until the over-current condition is cleared. If the 12V does not reach the correct level within 8 milliseconds (Timer2) then the process is halted until the MMC clears the Turn_On_Payload input and resets it.

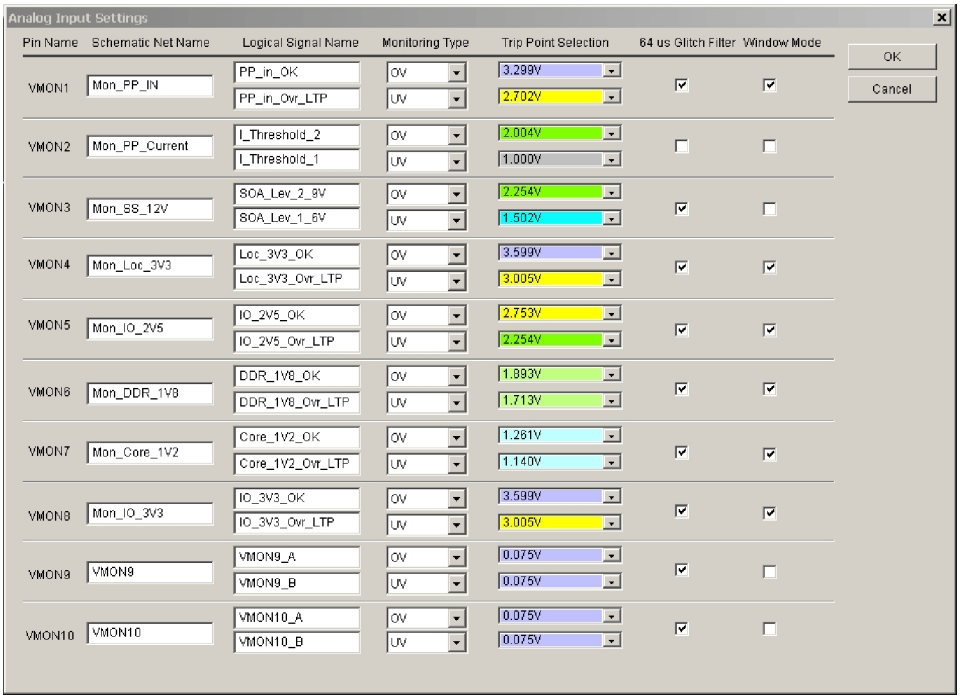
Once the 12V supply is stable the 3.3V and 1.2V power supplies will be enabled and the output voltages monitored using the VMON inputs. These supplies are monitored to insure they reach the proper voltage settings then the 2.5V and 1.8V power supplies are enabled and the 3.3V I/O supply is turned on using MOSFET Q3. These three voltages are also monitored using VMON inputs to insure they reach the proper voltage settings. The voltage settings are adjustable using the VMON settings window shown in Figure 4.

Once all the voltages have reached the proper values the design waits for an additional 147 ms before asserting the CPU_Reset signal to allow the CPU time to power up. The Power_Fault and POK signals are also asserted at this time.

Once the design has completed the startup functions it goes into a monitoring state. During this state if a voltage signal strays outside the limits, or if the MMC requests a system shutdown, or the card is removed from the shelf or host, then the system goes into a controlled shutdown mode. The shutdown mode turns off the CPU_Reset and POK signals, then waits 2 ms, then turns off the 2.5V and 1.8V power supplies and the 3.3V I/O supply using MOSFET Q3. There is another 2 ms delay followed by turning off the 1.2V and 3.3V power supplies. The MOSFETs Q1 and Q2 will also be disabled by asserting the Shut_Down output signal.

The power supplies used in this reference design have an Inhibit input which is used to keep them off. Since the power supply is off when the Inhibit signal is shorted to ground, this reference design uses an NPN transistor with the base pulled up to 3.3V to keep the power supplies turned off when the card is first inserted. This is shown on sheet 3 of the schematic diagram in Appendix A. The outputs of the Power Manager II device are open drain outputs so they are compatible with the external pull-up resistor. In order to insure that this circuit works correctly the outputs of the Power Manager II device are configured using the PINS window to use a reset state of High and are driven low when the power supply is scheduled to be turned on.

Figure 4. AMC Card Power Manager II Design VMON Settings



The program in the Power Manager II PLD is listed below with explanations for each step. The program is divided into three sections. The first section is the Sequencer Instructions which consist of 15 steps. These Sequencer Instructions are executed in order beginning with step 0. Sequence Instructions 2-8 contain the basic start-up sequence and steps 10-15 contain the basic shut-down sequence. Once the start-up is complete the sequence waits in step 9 monitoring the system and if a shutdown condition is detected it begins the shutdown sequence. Sequence Instruction step 0 sets the initial conditions for the design while step 1 waits for a start-up instruction from the MMC.

The second section is the Exception conditions. The Exception condition will cause an interrupt to the start-up sequence if the exception condition is true. The Sequencer Instructions are conditionally interruptible so an exception will only interrupt those instructions which the user specifies as interruptible (see the column labeled Int.. in Figure 5). The Exception condition will cause the Sequence to jump to step 10 as specified in the exception condition.

The third section is the Supervisory Logic Equations. The Supervisory Logic Equations are always active independent of which step the Sequencer Instructions are in. The Supervisory Logic Equations in this design are used to implement the logic for hysteretic and SOA control of MOSFET Q1. The Power_Fault and Shut_Down logic is also included in the Supervisory Logic Equations for this design.

Listing 1. Main Sequence (State Machine 0)

```
Step 0   EN_F3V3= 0, Shut_Down = 0, PP_Turning_on = 1, Disable_P3V3= 1,
         Disable_P2V5 = 1, Disable_P1V2 = 1, Disable_P1V8 = 0,
         ERR = 1, POK = 0, CPU_Reset = 0
         //  Turn-off supplies, reset output signals.

Step 1   WAIT for AGOOD AND Turn_on_Payload
         //  Wait for Analog Calibration and turn payload on signal from
             MMC.

Step 2   WAIT for SOA_Lev_2_9V or 8.19 ms using Timer 2
             on Timeout Then GOTO 14
         //  If the Soft started voltage does not reach 9V within 8 ms,
             shut the FET down.

Step 3   PP_Turning_on = 0, Disable_P3V3 = 0, Disable_P1V2 = 0,
         //  Enable 1.2V Core supply and Local 3.3V supply, Change
             Current Limit to Normal Operation.

Step 4   WAIT for Loc_3V3_OK AND Core_1V2_OK
         //  Wait until Core voltage and local 3.3V is OK.

Step 5   EN_F3V3 = 1, Disable_P2V5 = 0, Disable _P1V8 = 0,
         //  Turn on 1.8V, 2.5V supplies and 3.3V MOSFET.

Step 6   WAIT for IO_2V5_OK AND DDR_1V8_OK AND IO_3V3_OK
         //  Wait until all supplies are fully on.

Step 7   WAIT for 147.46 ms using Timer 3
         //  This delay is used to stretch the CPU Reset.

Step 8   ERR = 0, POK = 1, CPU_Reset = 1,
         //  This Flags normal operating condition.

Step 9   WAIT Card_Present OR NOT Turn_on_Payload OR NOT PP_in_OK OR
         I_Threshold_1 OR NOT Loc_3V3_OK OR NOT IO_2V5_OK OR
         NOT DDR_1V8_OK OR NOT Core_1V2_OK OR NOT IO_3V3_OK OR
         PP_Overcurrent
         //  Wait for any voltage or current faults or card extraction.
             This step monitors the state of normal operations.

Step 10  POK = 0, CPU_Reset = 0,
         //  Flag that there is a supply fault.

Step 11  WAIT for 2.05 ms using Timer 4
         //  Allow CPU processing time.

Step 12  EN_F3V3 = 0, Disable_P2V5 = 1, Disable_P1V8 = 1,
         //  Turn off 3.3V, 2.5V and 1.8V supplies.

Step 13  WAIT for 2.05 ms using Timer 4
         //  Wait for supplies to turn off.
```

```
Step 14  Shut_Down = 1, Disable_P3V3 = 1, Disable_P1V2 = 1, ERR = 1,
         //  The MOSFETs are Shut down if there was a fault in the
             supply.

Step 15  IF NOT Turn_on_Payload
             Then GOTO 0  Else GOTO 15
         //  The supply can be restarted by toggling the Turn-on payload
             signal.
```

Step 16(end-of-program)

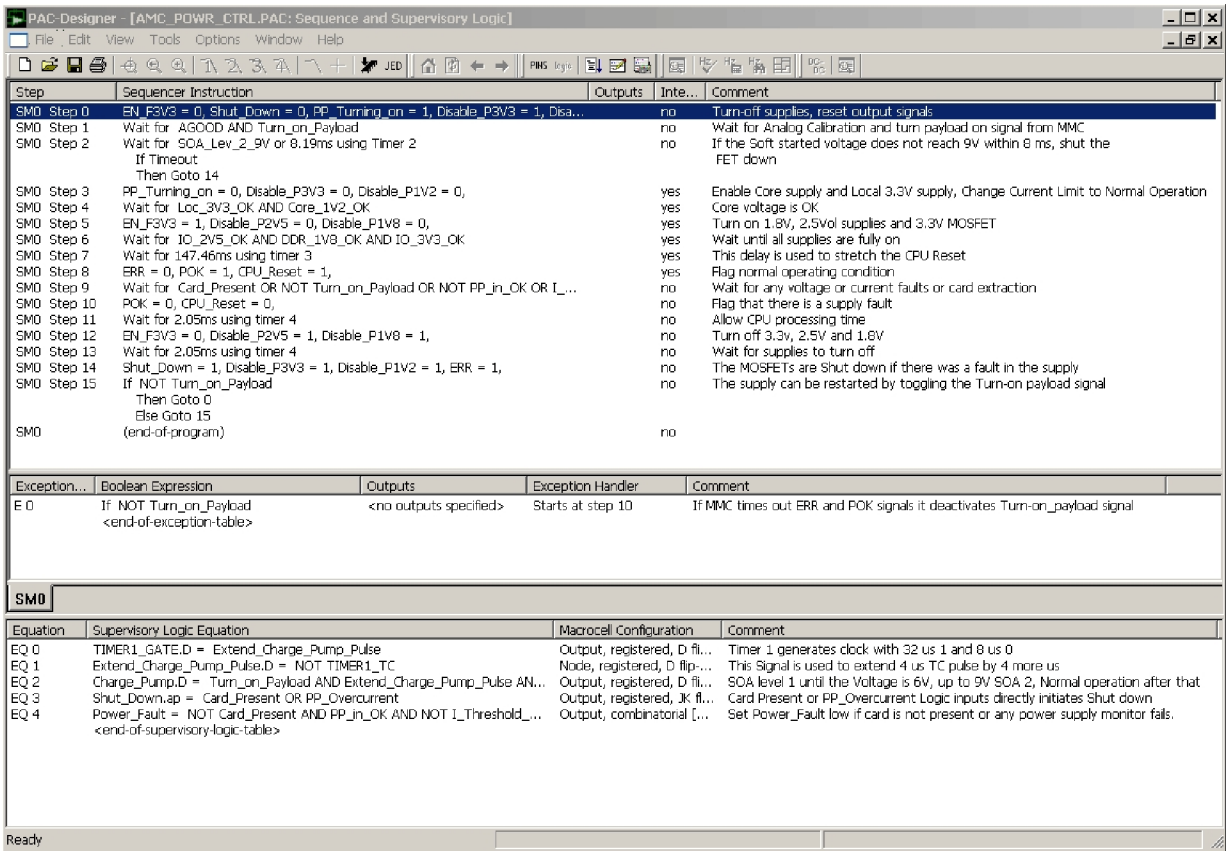
Listing 2. Sequencer Exception

```
E0       If NOT Turn_on_Payload, Starts at Step 10
         // If the start-up times out, the MMC turns off the
            Turn_On_Payload signal when ERR is asserted. This exception
            causes the Power Manager II to halt the sequence whenever
            the MMC turns off this signal.
```

Listing 3. Supervisory Logic Equations

```
EQ 0     TIMER1_GATE.D = Extend_Charge_Pump_Pulse
         //  Timer 1 generates clock with 32 us 1 and 8 us 0

EQ 1     Extend_Charge_Pump_Pulse.D = NOT TIMER1_TC
         //  This Signal is used to extend 4 us TC pulse by 4 more us

EQ 2     Charge_Pump.D = Turn_on_Payload AND Extend_Charge_Pump_Pulse AND
         ( ( NOT I_Threshold_1 AND NOT SOA_Lev_1_6V ) OR
         ( NOT I_Threshold_2 AND NOT SOA_Lev_2_9V AND SOA_Lev_1_6V ) OR
         ( SOA_Lev_2_9V ) )
         //  SOA level 1 until the Voltage is 6V, up to 9V SOA 2, Normal
             operation after that.

EQ 3     Shut_Down.ap = Card_Present OR PP_Overcurrent
         //  Card Present or PP_Overcurrent Logic inputs directly
             initiates Shut down.

EQ 4     Power_Fault = NOT Card_Present AND PP_in_OK AND NOT I_Threshold_1
         AND Loc_3V3_OK AND IO_2V5_OK AND DDR_1V8_OK AND Core_1V2_OK AND
         IO_3V3_OK OR PP_Overcurrent
         //  This Sets Power_Fault low if card is not present or any power
             supply monitor fails.
```

Figure 5. AMC Card Power Manager II Design



Design Simulation

For the purposes of simulation the value of Timer3 was changed to 12.29 ms to allow the simulation to run in a shorter time frame. The simulation results are shown in Figure 6.

The simulation shows a start-up sequence beginning at 10 ms (indicated by the left cursor at 10,000 µs) when the Turn_on_Payload signal is asserted by the MMC. There is a brief interruption in the start-up sequence when the I_Threshold_1 signal is asserted high indicating an over-current condition in the SOA region 1. There is another when the I_Threshold_2 signal is asserted high indicating an over-current condition in the SOA region 2. The start-up sequence continues in each case when the over-current indication is de-asserted.

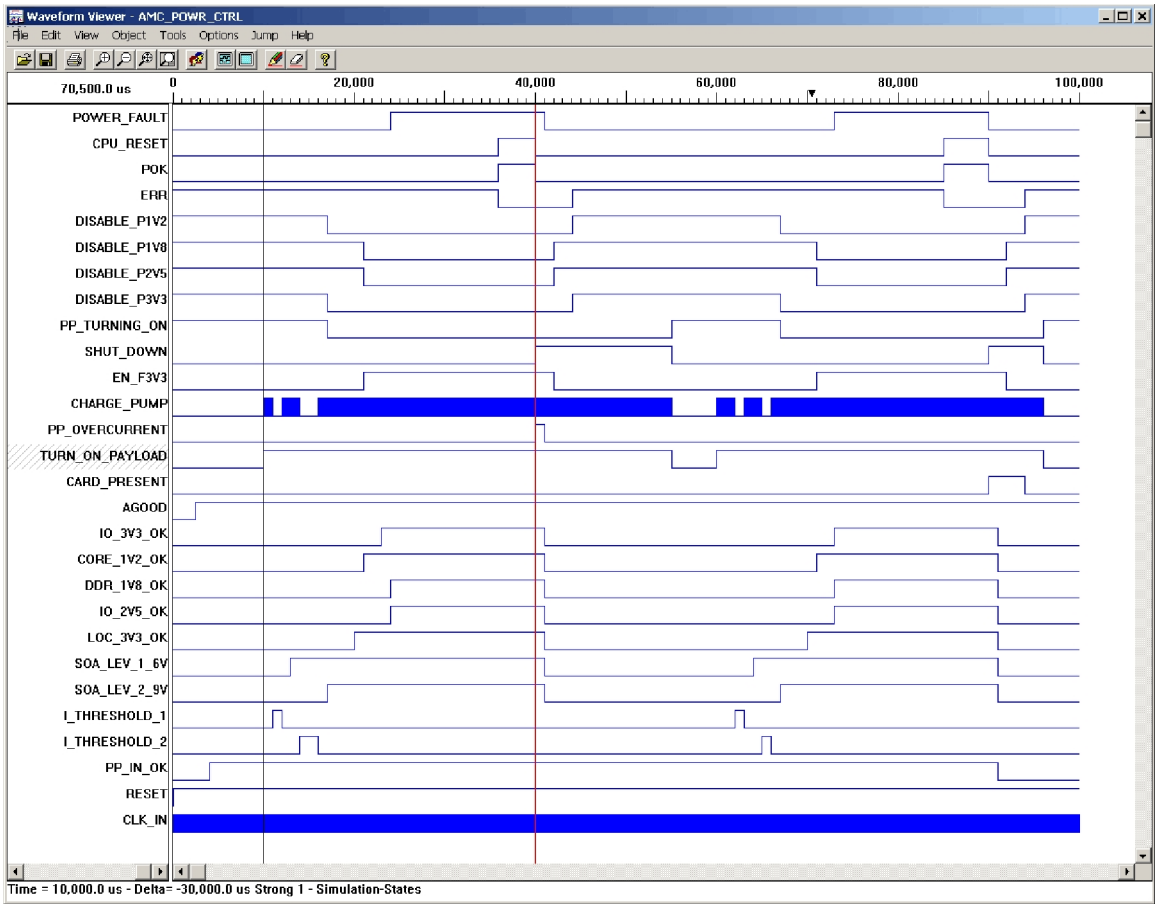
The remainder of the start-up is completed normally and the back-end power supplies are sequenced on; the first group at approximately 17 ms and the second group at 21 ms. The start-up then completes and the system goes into a monitoring state once the Power_Fault, CPU_Reset, and POK signals are asserted and the ERR signal is de-asserted. Notice how there is a delay from the time Power_Fault is asserted until CPU_Reset is asserted. This delay is used to allow the microprocessor to complete its power-up sequence. This delay was shortened from 147 ms to 12 ms for the purposes of making the simulation easier to read.

At 40 ms (the right cursor) an over-current condition is signaled by the PP_Overcurrent signal and the Power Manager II shuts down the back-end supplies and the payload power (+12V). The back-end power supplies are turned off by the sequence control as indicated by the individual outputs driving low. The payload power is turned off by driving the Shut_Down signal high which forces the MOSFET Q1 control circuit off.

A second start-up event is initiated at 60 ms when the Turn_on_Payload signal is asserted by the MMC. Notice how the MMC must first de-assert the signal before the start-up can continue. This insures that the AMC card does not go into a start-up condition earlier than intended. The second start-up sequence is similar to the first but is termi-

nated at 90 ms when the Card_Present signal is asserted indicating that the card was removed for the host or shelf improperly.

Figure 6. AMC Card Power Manager II Design Simulation Results



Implementation

Table 1. Performance and Resource Utilization[1]

Device	Macrocells	Product Terms	VMONs	I/Os	Timers
ispPAC-POWR1014A	22	98	8	15	4

1. Resource utilization characteristics are generated using PAC-Designer® 5.2 software. When using this design in a different device, utilization characteristics may vary.

References

- ispPAC-POWR1014/A Data Sheet
- Zetex ZXCT1009 Data Sheet

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2010	01.0	Initial release.

Appendix A. Schematic

The schematic in this appendix provides an example of how the ispPAC®-POWR1014A device should be connected in a typical system. It also demonstrates a typical example of how the current sense and voltage divider networks function and should be arranged.

On sheet 1 of the schematic (Figure 7) the ispPAC-POWR1014A device is shown. Note how the VCCA and VCCD pins have been tied together on this board and that the VCCPROG pin is left unconnected as recommended in the data sheet. The VCCPROG pin should only be connected if it is desired to program the ispPAC-POWR1014A device when VCCA and VCCD are not powered up. Also note that the RESETB pin is left unconnected as it should be except when cascading two or more POWR1014A devices.

The pull-up resistor sizes for the I^2C connection (SCL & SDA) are adequate for an application where there is only one or two other devices connected and the PCB run length is not excessive. If these conditions are not met then the pull-up resistors may need to be stronger (lower resistances). This is also true for the pull-up on the TMS pin and the pull-down on the TCK pin.

Sheet 2 of the schematic (Figure 8) shows the current sense and voltage divider circuits. The voltage dividers use a 3k and 1k resistor circuit to ground to sense the 12V supply. This divider circuit is required to keep the voltage input at the VMON input below the data sheet recommended operating condition limit of 5.9V at the input pin. For this circuit the VMON input will see approximately 3V since three-fourths of the total voltage drop will be across the 3k resistor. It is good design practice when connecting to voltages that can exceed the operational specifications of the Power Manager II to use a Zener diode as shown in the schematic (with a Zener voltage of 5.1V) connected between the VMON input and ground to protect the VMON input from surges or voltage spikes. For more information about this type of circuit see application note AN6041, Extending the VMON Input Range of Power Manager Devices.

Also shown on sheet 2 is the current sense circuit. A shunt resistor, R14, is added to the main power supply to monitor the current flowing. This resistor should be kept small to prevent a power loss that would affect the operation of the system. For this design a 0.01 ohm, 3 watt resistor is used. In order for the voltage sensing to be detected by a VMON input of the Power Manager II device it must be amplified. This design uses a high-side current monitor, U2 in the schematic. This device creates a current output that is proportional to the input voltage, in this case the voltage across the shunt resister. The current passes through three resistors in series to produce a voltage level that the VMON input can sense. One of the voltages created is used to drive a digital input of the Power Manager II, IN3. This input is used to sense an over-current condition and provide a fast shut-down of the MOSFET circuit (Q1 & Q2) using the output OUT3. The VMON and digital inputs are both protected by a Zener diode as mentioned above.

The current monitor output produces a voltage drop across resistors R24 and R25 which generates the input for the VMON. The two resistors are used in series to generate two different trip points depending upon the where the system is operating. Initially, when the card is first powering up, the current is limited to approximately 1.5 amps by the trip point in the VMON and the hysteretic and SOA control of the MOSFET driver circuit (see Equation 2 of the Supervisory Equations). Once the voltage across the MOSFETs drops the trip point is changed and the current is limited to approximately 3 amps. During this phase the current is passing through both resistors R24 and R25.

After the 12V supply reaches approximately 9V (determined by the SOA_LEV_2_9V trip point setting of 2.254V) the start-up phase is considered complete and the current limit is raised to 15 amps by driving low the digital output OUT4, which will ground that point of the circuit effectively removing R25 from the circuit. At this time the circuit is considered to be in an operational state and the remaining functions become active as determined by the sequence control.

For more information about this hot-swap circuit see RD1068, Power Feed and Hot Swapping 12V Supplies with Power Manager.

Sheet 3 of the schematic (Figure 9) shows the power supply circuits and how these can be connected to prevent the power supplies from being turned on before the Power Manager II device commands them to. The power sup-

plies shown have an inhibit pin which is shorted to ground to turn it off and is left open to turn it on. A transistor is used to short the inhibit pin to ground and keep each power supply turned off unless commanded to turn on by the Power Manager II device. The base of the NPN transistor is pulled up to the 3.3V Management Power with a 3.3k resistor. This Management Power is supplied by the host or shelf and will be present as soon as the AMC card is plugged in. The Power Manager II digital outputs are open drain outputs which require an external pull-up resistor so this arrangement is compatible with the outputs.

When the Power Manager II commands a power supply to turn on it will drive the output low and base of the transistor will also be pulled down. This will decrease the base-to-emitter voltage to a zero thus turning off the transistor and creating an open on the power supply inhibit pin and turning on the power supply. For more information about this type of circuit see application note AN6046, Interfacing Power Manager Devices with Modular DC-to-DC Converters.

Figure 7. Power Manager II POWR1014A

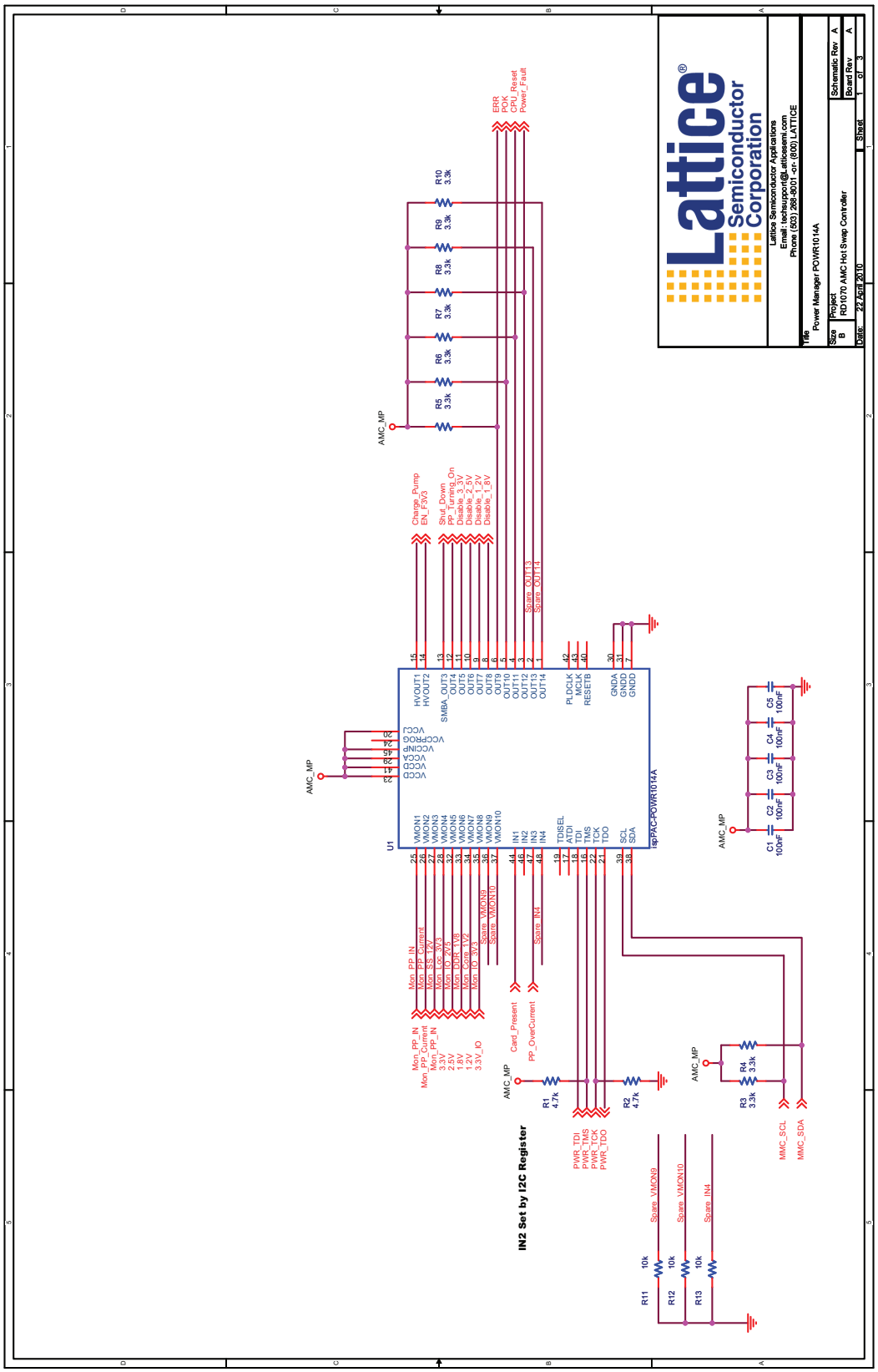

Figure 8. 12V Hot Swap

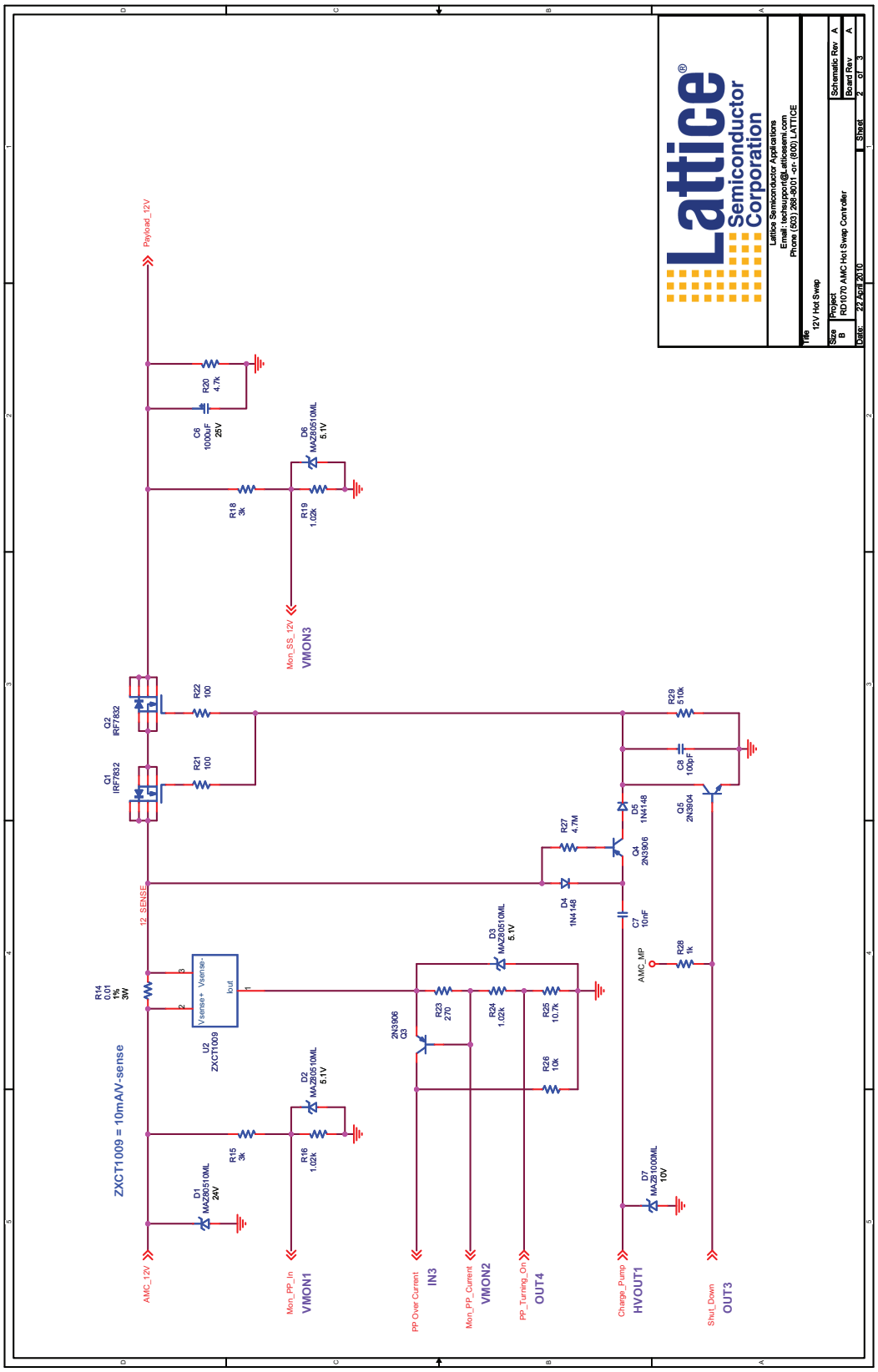

Figure 9. DC-DC Converters