



NOR Flash Memory Controller with WISHBONE Interface

Reference Design

FPGA-RD-02096-1.2

December 2019

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1. Introduction

NOR Flash memory provides random access capabilities to read and write data in specific locations in the memory without having to access the memory in sequential mode. Its high-speed read capacity allows the NOR Flash memory to be the first choice for code storage and direct execution in a variety of systems from computer BIOS to portable electronic devices.

In today's NOR Flash market, most NOR Flash memory devices share common basic design concepts. These memory devices are controlled by chip enable (CE_n), output enable (OE_n) and write enable (WE_n). Device operations are executed by a standard set of command codes. These command codes are supported by most NOR Flash memory devices in the market. The command codes are combined with addresses and data, and are written sequentially to the command registers using microprocessor write timing.

This reference design describes the use of Lattice programmable devices to implement a NOR Flash memory controller through a WISHBONE bus. It supports several common operational modes of a NOR Flash, including reset operation, autoselect manufacturer ID operation, read operation, program operation, chip erase operation and sector erase operation. It is available in both Verilog and VHDL languages.

2. Features

- WISHBONE host interface
- Supports reset operation, autoselect manufacturer ID operation, read operation, program operation, chip erase operation and sector erase operation of NOR Flash memory
- Supports both Word configuration Flash memory and Byte configuration Flash memory
- Address width of NOR Flash memory configurable from 1 to 32 bits
- Read/write cycle access time can be optimized for a specific NOR Flash memory through the setting of timing parameters in the design

3. Functional Description

The functional block diagram of the NOR Flash Memory controller with WISHBONE interface is shown in [Figure 3.1](#). This design has a standard WISHBONE slave bus that connects the NOR Flash memory device with a microprocessor and other on-chip components. From the WISHBONE bus, this design appears as a set of addressable registers that can be read from or written to. Through these registers, the WISHBONE master can transmit and receive data and control the operation of the NOR Flash memory. The control Finite State Machine (FSM) is used to enter the appropriate operational modes of NOR Flash based on the WISHBONE code (wb_code) register which is set by the WISHBONE master. For every operational mode of NOR Flash, the control_FSM calls a timing FSM to generate appropriate control signals to access the NOR Flash based on the NOR Flash memory timing specification.

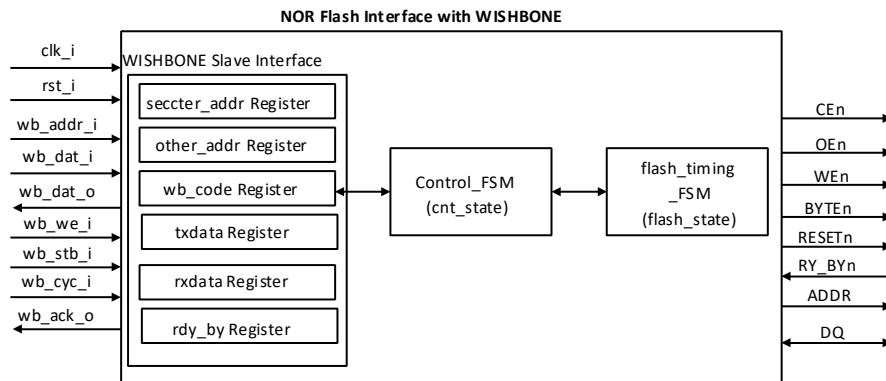


Figure 3.1. NOR Flash interface with WISHBONE Block Diagram

4. Interface

Table 4.1. NOR Flash Interface with WISHBONE I/O Interface Descriptions

Signal Name	Signal	Active State	Definition
WISHBONE Slave Interface			
clk_i	Input	N/A	System clock signal.
rst_i	Input	High	Asynchronous system reset signal.
wb_addr_i[3:0]	Input	N/A	Slave address bus.
wb_dat_i[15:0]	Input	N/A	Slave data input bus.
wb_dat_o[15:0]	Output	N/A	Slave data output bus.
wb_we_i[3:0]	Input	1 write; 0 read	Slave write/read signal.
wb_stb_i	Input	High	Slave strobe signal.
wb_cyc_i	Input	High	Slave cycle signal.
wb_ack_o	Output	High	Slave acknowledge signal.
NOR Flash Memory Interface			
CEn	Output	Low	Chip enable signal.
OEn	Output	Low	Output enable signal.
WEn	Output	Low	Write enable signal.
BYTEn	Output	1 word; 0 byte	Word/Byte selection.
RESEt_n	Output	Low	Hardware reset signal.
RY_BYn	Input	1 ready; 0 busy	Ready/Busy signal.
ADDR[addr_width-1:0]	Output	N/A	Address signal.
DQ[15:0]	Input/Output	N/A	Data inputs/outputs.

4.1. WISHBONE Interface

The WISHBONE slave interface consists of six registers which are used to interact with the WISHBONE master. A description of each of these addressable registers is shown in [Figure 4.2](#).

Table 4.2. Register Descriptions

Register	Width	WISHBONE Access	Address	Description
sector_addr	SECTOR_ADDR_WIDTH	Read/Write	0x0	Sector address.
other_addr	OTHER_ADDR_WIDTH	Read/Write	0x1	Least significant bits of the ADDR.
txdata	16	Read/Write	0x2	Data to be sent to the NOR Flash.
rxdata	16	Read Only	0x3	Data to be received from the NOR Flash.
rdy_by	1	Read Only	0x4	Ready/Busy status register.
wb_code	4	Read/Write	0x5	Code in this register indicates the operation the WISHBONE master initiates.

The address (defined by the ADDR signal) of a NOR Flash is divided into two parts. The most significant bits of ADDR indicate the address of a sector/bank/block. Different manufacturers may use any of these terms to describe this. The least significant bits of ADDR indicate a certain address in the specified sector. The sector_addr register contains the most significant bits of ADDR and the other_addr register contains the least significant bits. The width of the sector_addr register and other_addr register is defined by the parameters SECTOR_ADDR_WIDTH and OTHER_ADDR_WIDTH, respectively. The width of the ADDR signal is defined by the parameter ADDR_WIDTH. These parameters are described in [Figure 4.3](#).

Table 4.3. Parameter Descriptions

Parameter	Description	Active Value	Default Value
SECTOR_ADDR_WIDTH	Specifies the sector address width.	1 to 16	8
OTHER_ADDR_WIDTH	Specifies the address width in a certain sector.	1 to 16	8
ADDR_WIDTH	Specifies the width of the ADDR signal. Equals to the sum of SECTOR_ADDR_WIDTH and OTHER_ADDR_WIDTH.	1 to 32	16
WORD_BYTEn	'1' indicates Flash in Word configuration. '0' indicates Flash in Byte configuration.	0, 1	1

The txdata register contains the data that is written to the Flash memory and the rxdata register contains the data that is read from the Flash memory.

The wb_code register contains the code that indicates the operation the WISHBONE master initiates. Table 4.4. lists the coding of wb_code register. The rdy_by register indicates whether the NOR Flash finishes the current operation. '1' means the NOR Flash is ready for the next operation and '0' means the NOR Flash is busy.

Table 4.4. Coding of wb_code Register Descriptions

Coding of wb_code Register	Description
"0001"	WISHBONE master initiates the reset operation to the Flash.
"0010"	WISHBONE master initiates the read manufacturer ID operation to the Flash.
"0011"	WISHBONE master initiates the sector erase operation to the Flash.
"0100"	WISHBONE master initiates the chip erase operation to the Flash.
"0101"	WISHBONE master initiates the read operation to the Flash.
"0110"	WISHBONE master initiates the program (write) operation to the Flash.

4.2. WISHBONE Master Command Sequence

Each operation to the NOR Flash memory has its own event sequence initiated by the WISHBONE master. This section details the command sequence for each operation.

Reset operation:

1. Write code "0001" to the wb_code register.
2. Read the rdy_by register until the value of this register is '1'.

Read manufacturer ID:

1. Write code "0010" to the wb_code register.
2. Read the rdy_by register until the value of this register is '1'.

Sector erasure:

1. Write the sector address to the sector_add register.
2. Write code "0011" to the wb_code register.
3. Read the rdy_by register until the value of this register is '1'.

Initiating chip erase:

1. Write code "0100" to the wb_code register.
2. Read the rdy_by register until the value of this register is '1'.

Read operation:

1. Write the sector address (most significant bits of ADDR) to the sector_addr register.
2. Write to the other_address with the least significant bits of ADDR.
3. Write code "0101" to the wb_code register.
4. Read the rdy_by register until the value of this register is '1'.
5. Read the rxdata register which contains the data from the Flash.

Program/write operation:

1. Write the sector address (most significant bits of ADDR) to the sector_addr register.
2. Write to other_address with the least significant bits of ADDR.
3. Write to the txdata register with the data to be written to the Flash.
4. Write code "0110" to the wb_code register.
5. Read the rdy_by register until the value of this register is '1'.

4.3. Operational Mode of the NOR Flash

Once the wb_code register is set to the appropriate value, the control_FSM is forced to the corresponding state. Figure 4.1. shows the state diagram of the control_FSM.

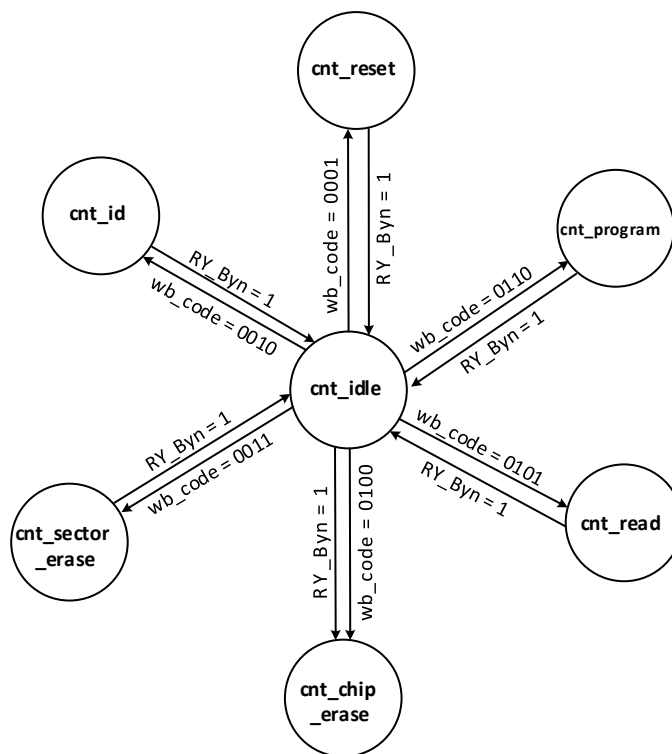


Figure 4.1. State Diagram of the control_FSM

For every operational mode of the NOR Flash, control_FSM calls timing_FSM (flash_timing_FSM) to generate the appropriate control signals to access the NOR Flash based on the NOR Flash timing specification. Each operational mode has its own command set. A proper command with specific address and data sequences must be written into the NOR Flash. The defined command set sequences are shown in Table 4.5. This design supports both Word configuration and Byte configuration of Flash memory. The parameter WORD_BYTEN defines the Word or Byte configuration (listed in Table 4.5.).

Table 4.5. NOR Flash Command Sequence

Command Sequence		Cycle	First Cycle		Second Cycle		Third Cycle		Fourth Cycle		Fifth Cycle		Sixth Cycle	
			Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
Reset	Addr	1	xxx											
	Data		0xf0											
Manufacturer ID	Addr	4	0x555	0xaaa	0x2aa	0x555	0x555	0xaaa	0x00					
	Data		0xaa		0x55		0x90		ID from Flash					
Sector Erase	Addr	6	0x555	0xaaa	0x2aa	0x555	0x555	0xaaa	0x555	0xaaa	0x2aa	0x555	SA	
	Data		0xaa		0x55		0x80		0xaa		0x55		0x30	
Chip Erase	Addr	6	0x555	0xaaa	0x2aa	0x555	0x555	0xaaa	0x555	0xaaa	0x2aa	0x555	0x555	0xaaa
	Data		0xaa		0x55		0x80		0xaa		0x55		0x10	
Read	Addr	1	RA											
	Data		RD											
Program	Addr	4	0x555	0xaaa	0x2aa	0x555	0x555	0xaaa	PA					
	Data		0xaa		0x55		0xa0		PD					

Notes:

1. RA: Read Address, located in the sector_addr register and the other_addr register.
2. RD: Read Data, located in the rxdata register.
3. PA: Program /Write Address, located in the sector_addr register and the other_addr register.
4. PD: Program/Write Data, located in the txdata register.
5. xxx: Don't care.
6. SA: Sector Address, located in the sector_add register.

The flash_timing_FSM is used to generate every write command and read data cycle timing. In order to write the command or data to the Flash, CEn and WEn must be low and OEn must be high. Addresses are latched on the falling edge of WEn and data are latched on the rising edge of WEn. Figure 4.2. shows the Flash write timing. To read the data from the Flash memory, the CEn and OEn must be low while WEn is high. Figure 4.3. shows the Flash read timing.

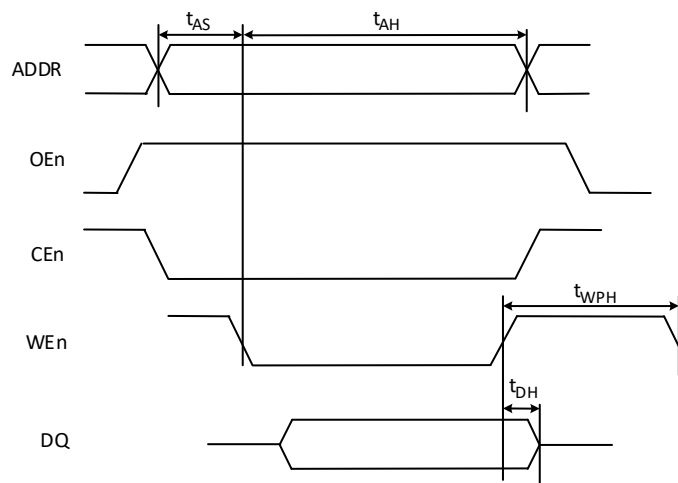


Figure 4.2. Flash Write Timing

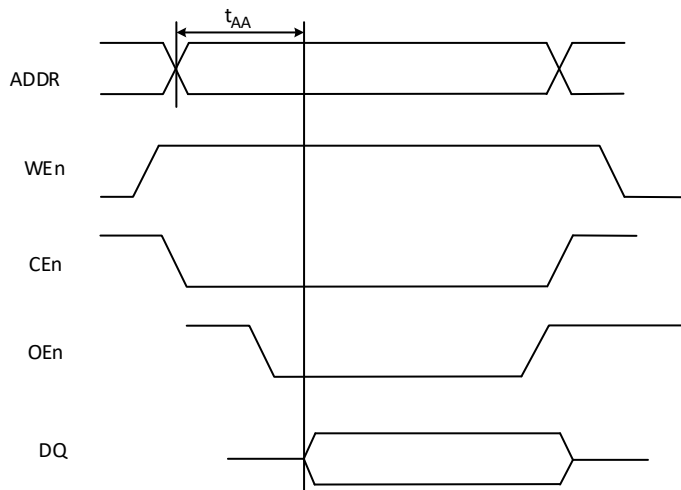


Figure 4.3. Flash Read Timing

Table 4.6. Parameter Descriptions

Symbol	Parameter
tAS	Address Setup Time
tAH	Address Hold Time
tDH	Data Hold Time
tWPH	Write Pulse Width High
tAA	Address Access Time

The access timing requirements are different for different NOR Flash devices. These timing parameters are defined as constants in the source file. They can be modified accordingly to meet the timing of a specific NOR Flash memory device.

5. Test Bench Description

The test bench simulates every operational mode of NOR Flash timing supported in this design.

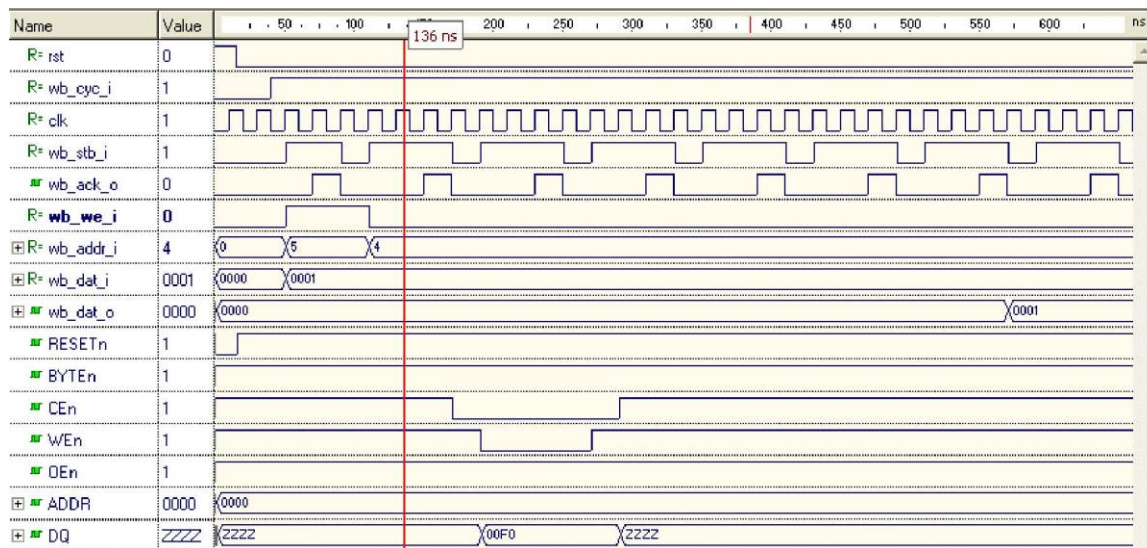


Figure 5.1. Reset Operation of NOR Flash

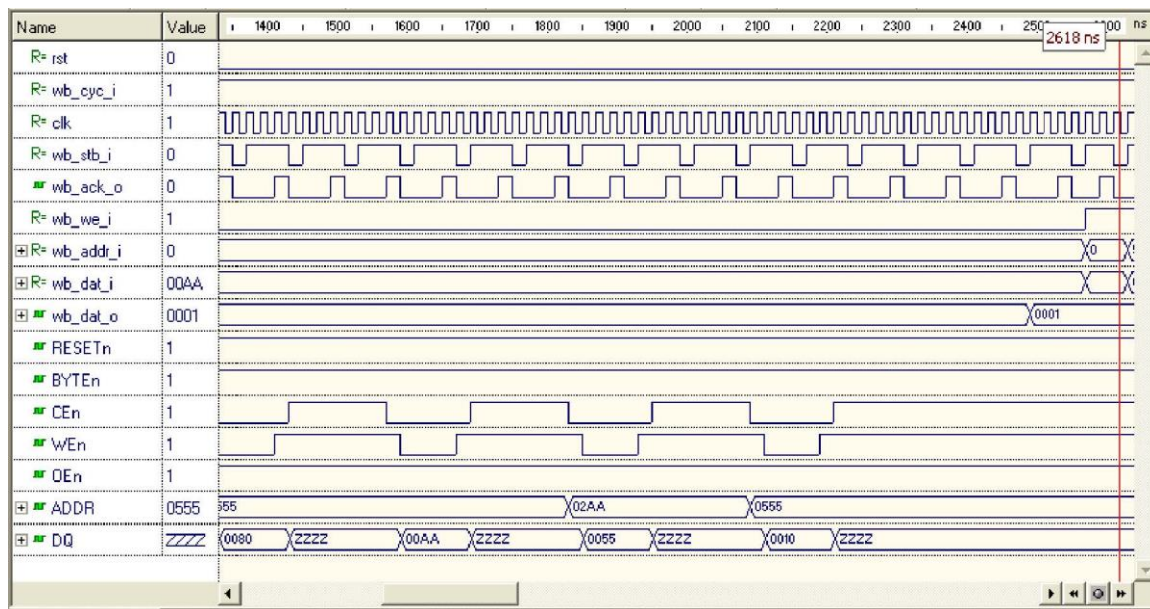


Figure 5.2. Chip Erase Operation of NOR Flash

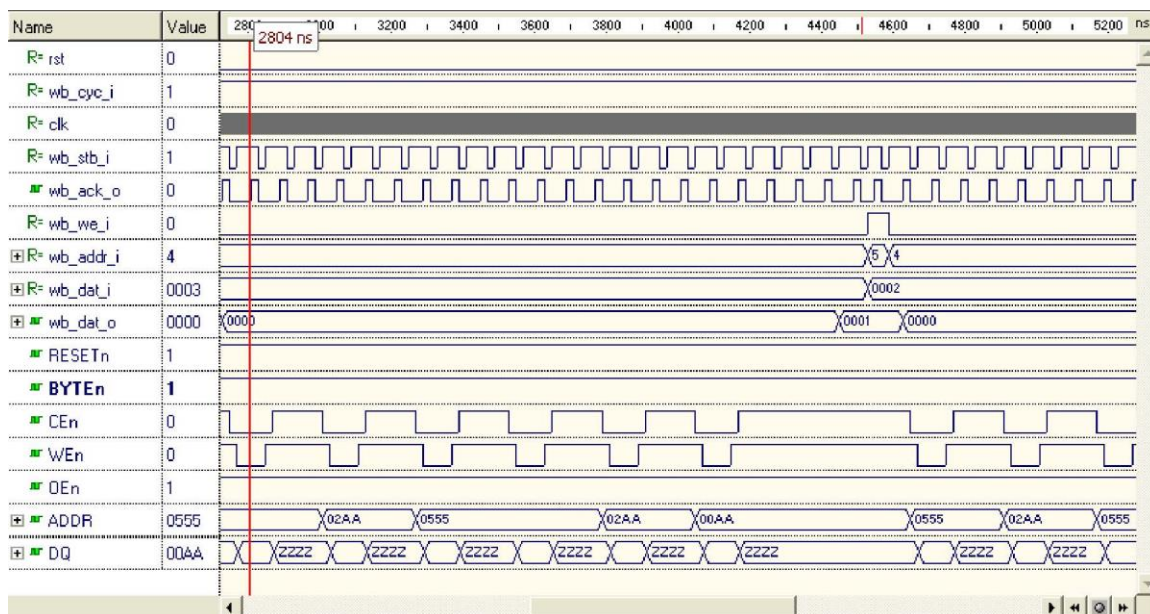


Figure 5.3. Sector Erase Operation of NOR Flash

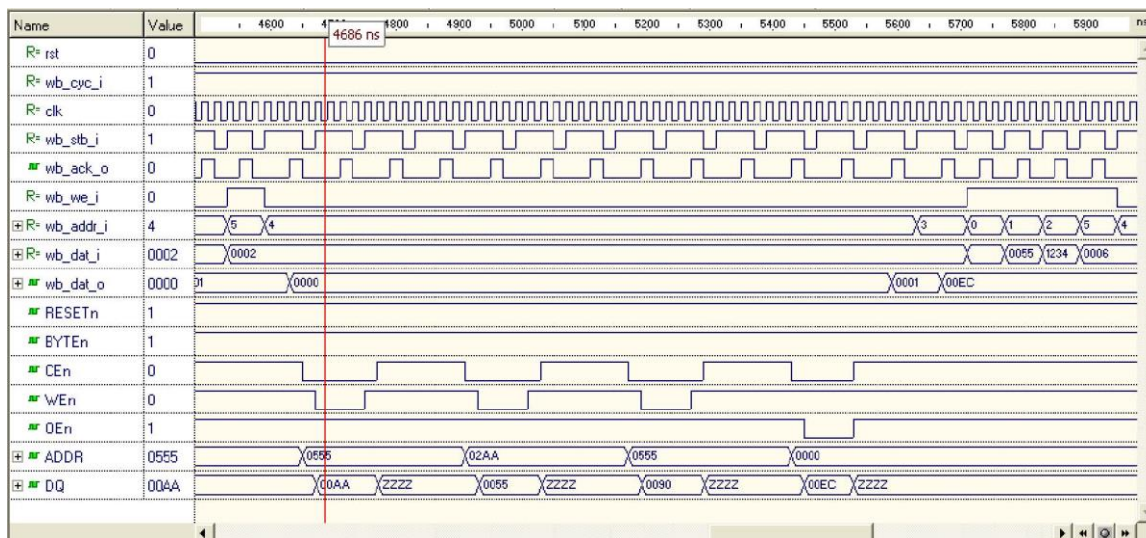


Figure 5.4. Read Manufacturer Operation of NOR Flash

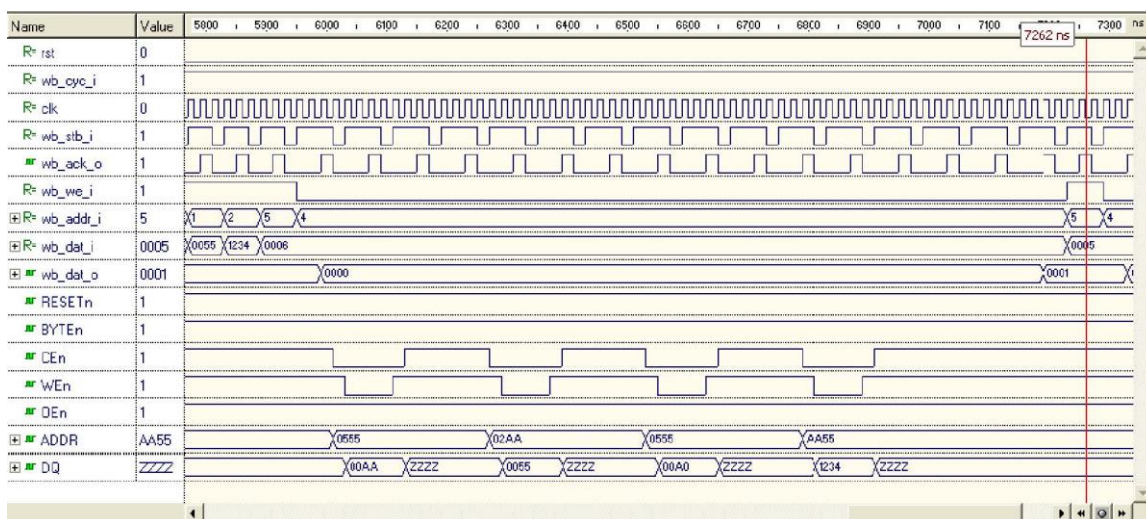


Figure 5.5. Program Operation of NOR Flash

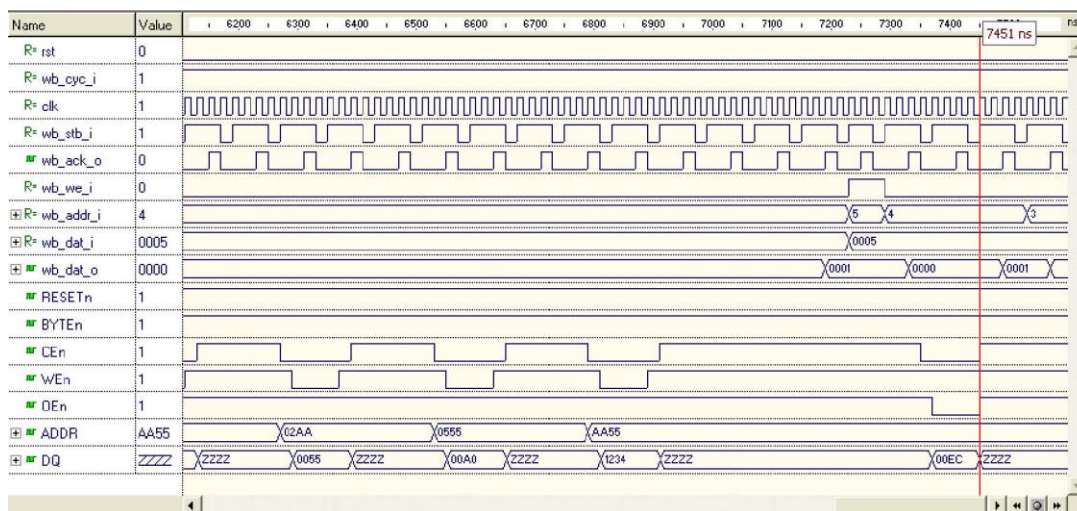


Figure 5.6. Read Operation of NOR Flash

6. Implementation

Table 6.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f _{MAX} (MHz)	I/Os	Architecture Resources
MachXO2™ 1	Verilog	-6	185	>80	80	N/A
	VHDL	-6	190	>80	80	N/A
MachXO™ 2	Verilog	-3	182	>80	80	N/A
	VHDL	-3	187	>80	80	N/A

Notes:

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-6TG144CES, with Lattice Diamond™ 1.1 or ispLEVER® 8.1 SP1. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO1200C-3T144C, with Lattice Diamond 1.1 or ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, December 2019

Section	Change Summary
All	- Changed document number from RD1087 to FPGA-RD-02096. - Updated document template.
Disclaimers	Added this section.

Revision 1.1, November 2010

Section	Change Summary
Implementation	Added support for MachXO2 device family and Lattice Diamond design software.

Revision 1.0, April 2010

Section	Change Summary
All	Initial release.



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