LatticeECP3 I/O Protocol Board to Texas Instruments ADC/DAC Adapter Board

User Guide

November 2014
EB54_1.3

Introduction

The LatticeECP3™ I/O Protocol Board to TI ADC/DAC Adapter provides a convenient platform to evaluate, test and debug user designs and IP cores targeted for the LatticeECP3-150 FPGA on the LatticeECP3 I/O Protocol Board, that are designed to interface directly with the Texas Instruments (TI) ADS6425 and DAC5682Z EVM boards. Other TI EVM boards may also be compatible with the LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter board. See Table 6 for a list of other compatible TI EVMs. When connected, the Lattice and TI evaluation boards lay out flat on the desktop in a mechanically stable test configuration.

Important: This document (including the schematic and mechanical drawings in Appendix A) describes the LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter marked as Revision A. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo.

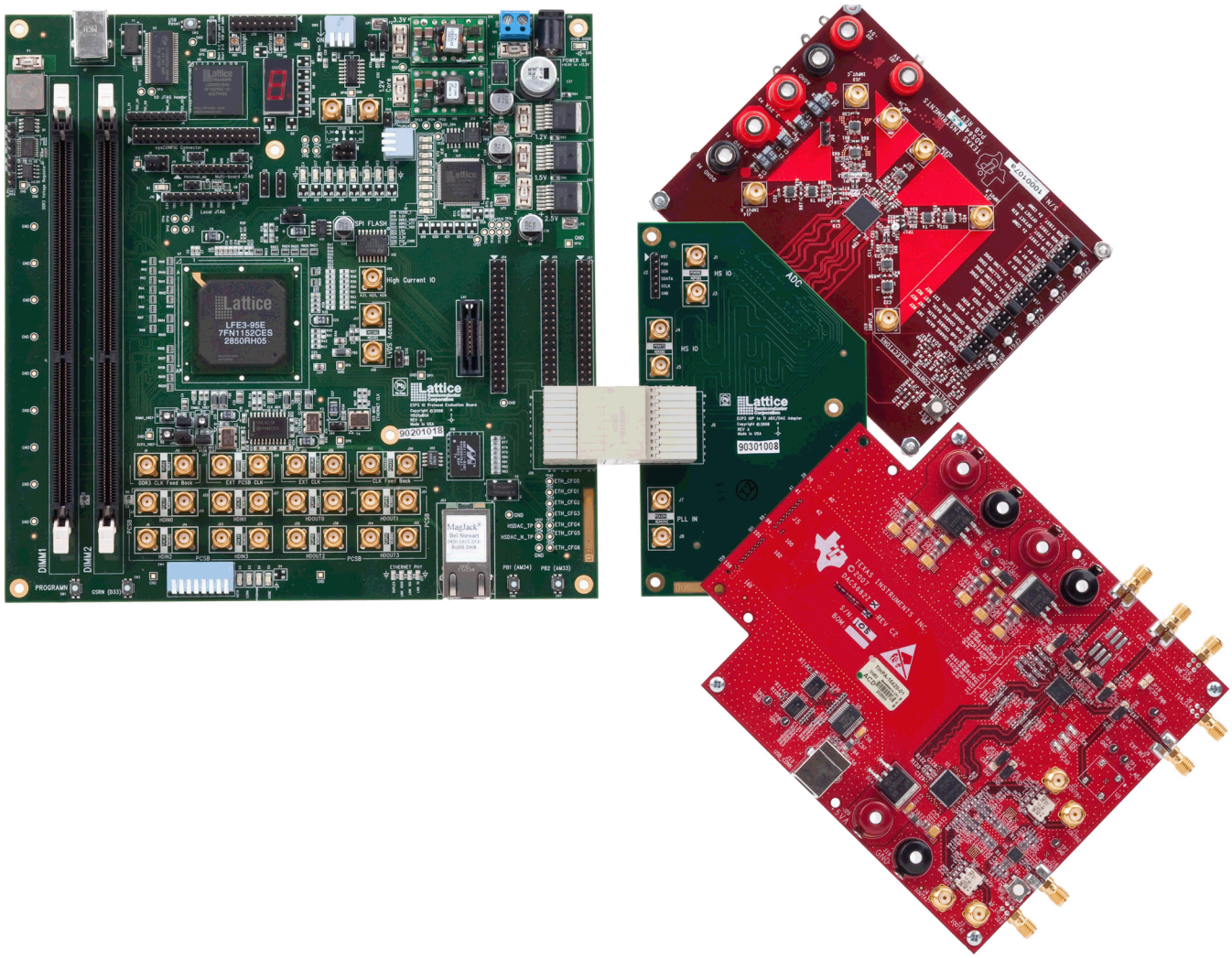
The LatticeECP3 is a third-generation device utilizing reconfigurable SRAM logic technology optimized to deliver high-performance features such as an enhanced DSP architecture, high-speed SERDES and high-speed source synchronous interfaces in an economical FPGA fabric. The LatticeECP3 devices also provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), and advanced configuration support, including encryption, multi-boot capabilities and TransFR™ field upgrade features. The LatticeECP3 SERDES-dedicated PCS functions, high jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII), SATA I/II, OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

For a full description of the LatticeECP3 FPGA, see the Lattice web site for the LatticeECP3 Family Data Sheet, technical notes and more: http://www.latticesemi.com.

For a full description of the LatticeECP3 I/O Protocol Board, see the LatticeECP3 I/O Protocol Board User's Guide.

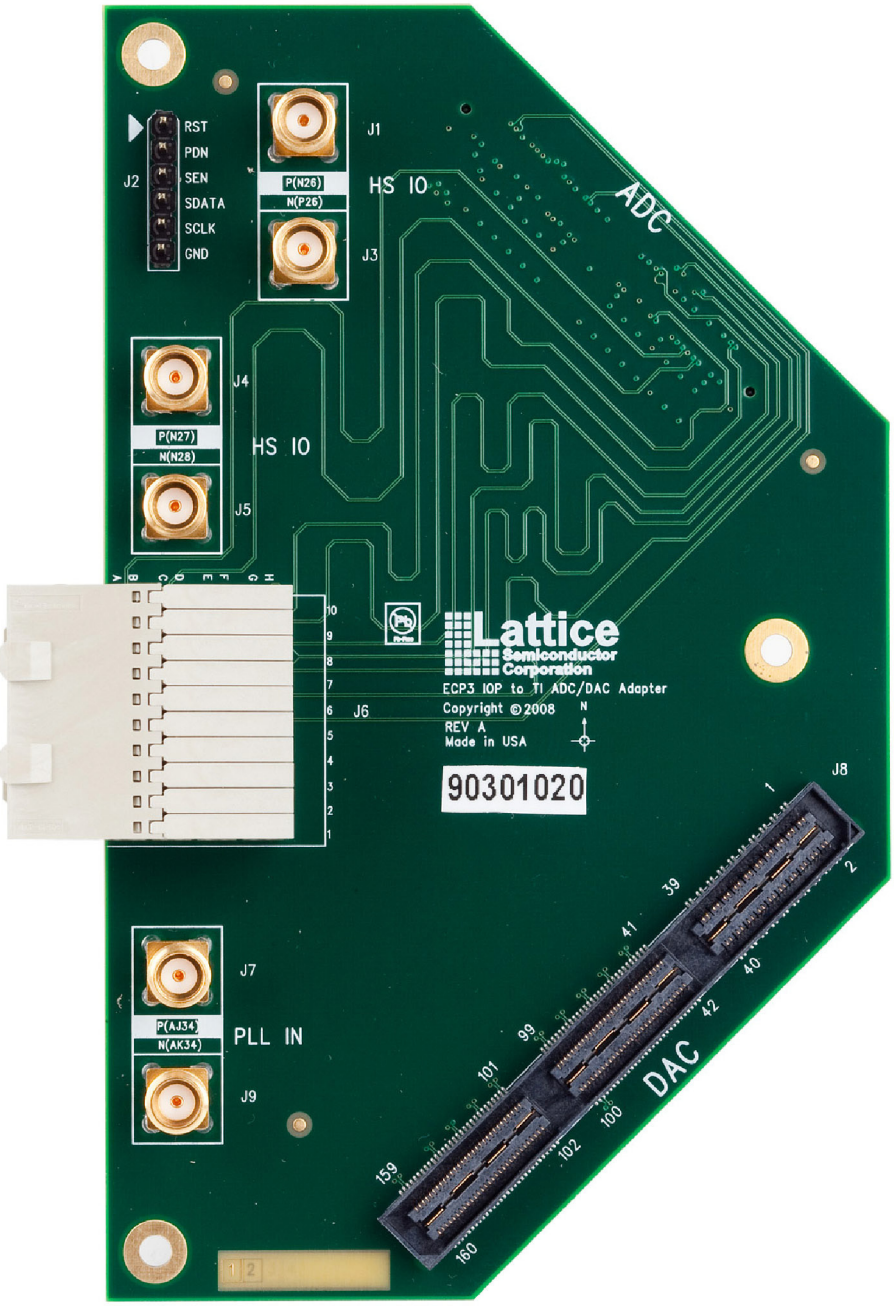
The ADS6425 ADC device from Texas Instruments is a high-speed, multi-channel, low power, 12- and 14-bit pin compatible Analog-to-Digital Converter (ADC) which can be evaluated using the TI ADS6425EVM board. The DAC5682Z DAC device from Texas Instruments is a 16-bit, 1.0 GSPS 2x-4x Interpolating Dual Channel Digital-to-Analog Converter (DAC) which can be evaluated using the TI DAC5682ZEVM board. Both the ADS6425EVM and DAC5682ZEVM evaluation boards can interface with the LatticeECP3 I/O Protocol Board simultaneously through the LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter as shown in Figure 1.

Figure 1. LatticeECP3 I/O Protocol Board Connected to TI ADC and DAC EVMs



General Description

Figure 2. LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter Board



The LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter Board easily connects the high-speed signals available at the LatticeECP3 I/O Protocol Board's HMZD connector at J6, to the high-speed connectors used by the TI ADS6425EVM at J10, and the DAC5682ZEVM at J8. The Adapter Board also provides several other remaining differential HMZD connected signals at SMA connectors J1, J3, J4, J5, J7 and J9. Other slow-speed signals used by the TI ADC at J10 are brought out to connector J2. The Adapter Board contains no active devices. Please observe proper ESD procedures when handling the boards connected to this Adapter Board.

Additional resources for the LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter board, such as updates to this document, sample programs and links to demos can be found on the Lattice web site.

Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 3.1 inches by 5.1 inches. Three 0.125” diameter plated through holes are provided to allow installation of plastic or metal spacers used to lift the board off the desktop to a uniform height. See the mechanical drawing in Appendix A for locations of the through holes. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: –40°C to 75°C
- Humidity: <95% without condensation

HMZD Connector

J6 is a high-speed HMZD header with 80 differential signal connections for interfacing the LatticeECP3 I/O Protocol Board to external application PCBs such as the TI ADC/DAC EVMs. The LatticeECP3 I/O Protocol Board has been verified to operate in a loop-through mode over the HMZD connector at up to 500 MT/s. The connections for J6 are listed in Table 1.

Table 1. J6 HMZD Connections

J58 Pin	LatticeECP3 I/O	Polarity	sysIO™ Bank	I/O Description[2]
A1	AA31	P	3	PR65A/PR83A[1]
B1	AA30	N	3	PR65A/PR83B[1]
A2	AD33	P	3	NC/PR97A[1]
B2	AD34	N	3	NC/PR97B[1]
A3	AE30	P	3	PR74A/PR101A[1]
B3	AE29	N	3	PR74B/PR101B[1]
A4	AD26	P	3	NC/PR106A[1]
B4	AD25	N	3	NC/PR106B[1]
A5	AP33	P	3	PR83A/PR110A[1]
B5	AP32	N	3	PR83B/PR110B[1]
A6	K31	P	2	NC/PR32A
B6	K32	N	2	NC/PR32B
A7	T32	P	2	PR35A/PR53A
B7	T31	N	2	PR35B/PR53B
A8	R28	P	2	PR28A[1]/PR46A[1]
B8	R27	N	2	PR28B[1]/PR46B[1]
A9	R31	P	2	PR29A/PR47A[1]
B9	R30	N	2	PR29B/PR47B[1]
A10	N32	P	2	PR20A/PR38A[1]
B10	N31	N	2	PR20B/PR38B[1]
C1	W27	P	3	PR55A[1]/PR73A[1]
D1	W26	N	3	PR55B[1]/PR73B[1]
C2	Y26	P	3	PR61A[1]/PR79A[1]
D2	Y25	N	3	PR61B[1]/PR79B[1]
C3	AE34	P	3	NC/PR92A[1]
D3	AE33	N	3	NC/PR92B[1]
C4	AL30	P	3	PR91A[1]/PR118A[1]

Table 1. J6 HMZD Connections (Continued)

J58 Pin	LatticeECP3 I/O	Polarity	sysIO™ Bank	I/O Description[2]
D4	AM30	N	3	PR91B[1]/PR118B[1]
C5	AJ31	P	3	PR88A[1]/PR115A[1]
D5	AK31	N	3	PR88B[1]/PR115B[1]
C6	V29	P	3	PR52A[1]/PR70A[1]/VREF1_3
D6	W28	N	3	PR52B[1]/PR70B[1]/VREF2_3
C7	U32	P	2	PR41A/PR59A
D7	U31	N	2	PR41B/PR59B
C8	W34	P	3	PR47A/PR65A[1]
D8	W33	N	3	PR47B/PR65B[1]
C9	L30	N	2	NC/PR34B[1]
D9	M29	P	2	NC/PR34A[1]
C10	N26	P	2	PR19A[1]/PR37A[1]
D10	P26	N	2	PR19B/PR37B[1]
E1	AA25	P	3	PR64A[1]/PR82A[1]
F1	AA26	N	3	PR64B[1]/PR82B[1]
E2	AA28	P	3	PR70A[1]/PR88A[1]
F2	AA27	N	3	PR70B[1]/PR88B[1]
E3	AD31	P	3	NC/PR91A[1]
F3	AD30	N	3	NC/PR91B[1]
E4	AC28	P	3	NC/PR100A[1]
F4	AB27	N	3	NC/PR100B[1]
E5	AM29	P	3	PR97A[1]/PR124A[1]
F5	AN29	N	3	PR97B[1]/PR124B[1]
E6	U28	P	3	PR46A[1]/PR64A[1]/PCLKT3_0
F6	V28	N	3	PR46B[1]/PR64B[1]/PCLKC3_0
E7	V31	P	3	PR44A/PR62A
F7	V30	N	3	PR44B/PR62B
E8	P28	P	2	PR25A[1]/PR43A[1]
F8	P27	N	2	PR25B[1]/PR43B[1]
E9	T29	P	2	PR34A[1]/PR52A[1]/VREF1_2
F9	T28	N	2	PR34B[1]/PR52B[1]/VREF1_2
E10	N34	P	2	PR23A/PR41A
F10	N33	N	2	PR23B/PR41B
G1	U33	N	3	PR43E_B/PR61E_B/RUM0_GPLLT_FB_B
H1	U34	P	3	PR43E_A/PR61E_A/RUM0/GPLLT_FB_A
G2	Y34	P	3	PR56A/PR74A[1]
H2	Y33	N	3	PR56B/PR74B[1]
G3	U26	P	2	PR43A[1]/PR61A[1]/PCLKT2_0
H3	U27	N	2	PR43A[1]/PR61B[1]/PCLKC2_0
G4	AH33	P	3	PR82A[1]/PR109A[1]
H4	AJ33	N	3	PR82B[1]/PR109B[1]
G5	AP31	P	3	PR92A/PR119A[1]
H5	AN31	N	3	PR92B/PR119B[1]
G6	W32	P	3	PR50A/PR68A

Table 1. J6 HMZD Connections (Continued)

J58 Pin	LatticeECP3 I/O	Polarity	sysIO™ Bank	I/O Description[2]
H6	W31	N	3	PR50B/PR68B
G7	R34	P	2	PR32A/PR50A
H7	R33	N	2	PR32B/PR50B
G8	T26	P	2	PR37A[1]/PR55A[1]/RUM0_GDLLT_IN_A
H8	T27	N	2	PR37B[1]/PR55B[1]/RUM0_GDLLT_IN_B
G9	N30	P	2	PR17A/PR35A
H9	N29	N	2	PR17B/PR35B
G10	P34	P	2	PR26A/PR44A
H10	P33	N	2	PR26B/PR44B

1. I/O with true LVDS output capability.
2. I/O description lists both LatticeECP3 –95/–150 density devices.

SMA Signal Connectors

There are three pairs of SMA connectors that provide general purpose high-speed differential signal paths to the LatticeECP3 through the HMZD connector J6. The SMA connectors are provided for general purpose user-definable signals. Table 2 details to which I/O pin each SMA connector is wired.

Table 2. SMA Connectors to the LatticeECP3-150 Device[1, 2]

Location	LatticeECP3 I/O	Polarity	sysIO Bank	I/O Description
J7	U33	N	2	PR43E_B/PR61E_B/RUM0_GPLLT_FB_B
J9	U34	P	2	PR43E_B/PR61E_B/RUM0_GPLLT_FB_A
J1	K31	P	2	NC/PR32A
J3	K32	N	2	NC/PR32B
J4	L30	N	2	NC/PR34B[3]
J5	M29	P	2	NC/PR34A[3]

1. The LatticeECP3 I/O pin numbers shown at the SMA connectors printed on the Adapater Board silk layer, are no longer valid.
2. J4, J5, J7 and J9 polarity indicators (P and N) printed on the Adapter Board silk layer, are swapped.
3. I/O with true LVDS output capability.

TI ADC EVM Connector J10

J10 is a high-speed header with 36 differential signal connections for interfacing the LatticeECP3 I/O Protocol Board to a TI ADS6425 EVM. Not all J10 pins are used by the TI ADS6425 EVM, but other boards may use those unused pins. The connections for J10 are listed in Table 3.

Table 3. TI ADC EVM Connections at J10

J10 Pin	ADS6425 Signal	LatticeECP3 Pin	Polarity	sysIO Bank	I/O Description[2]	J6 Pin
8		N29	N	2	PR17B/PR35B	H9
10		N30	P	2	PR17A/PR35B	G9
14		P26	N	2	PR19B[1]/PR37B[1]	D10
16		N26	P	2	PR19A[1]/PR37A[1]	C10
20		N31	N	2	PR20B/PR38B[1]	B10
22		N32	P	2	PR20A/PR38A[1]	A10
26		N33	N	2	PR23B/PR41B	F10
28		N34	P	2	PR23A/PR41A	E10
32	DA0_M	P27	N	2	PR25B[1]/PR43B[1]	F8
34	DA0_P	P28	P	2	PR25A[1]/PR43A[1]	E8

Table 3. TI ADC EVM Connections at J10 (Continued)

J10 Pin	ADS6425 Signal	LatticeECP3 Pin	Polarity	sysIO Bank	I/O Description[2]	J6 Pin
38	DA1_M	P33	N	2	PR26B/PR44B	H10
40	DA1_P	P34	P	2	PR26A/PR44A	G10
44	DB0_M	R27	N	2	PR28B[1]/PR46B[1]	B8
46	DB0_P	R28	P	2	PR28A[1]/PR46A[1]	A8
50	DB1_M	R30	N	2	PR29B/PR47B[1]	B9
52	DB1_P	R31	P	2	PR29A/PR47A[1]	A9
56	DCLK_M	U27	N	2	PR43B[1]/PR61B[1]/PCLKC2_0	H3
58	DCLK_P	U26	P	2	PR43A[1]/PR61B[1]/PCLKT2_0	G3
64	FCLK_M	T27	N	2	PR37B[1]/PR55B[1]/RUM0_GDLLT_IN_B	H8
66	FCLK_P	T26	P	2	PR37A[1]/PR55A[1]/RUM0_GDLLT_IN_A	G8
70	DC0_M	R33	N	2	PR32B/PR50B	H7
72	DC0_P	R34	P	2	PR32A/PR50A	G7
76	DC1_M	T28	N	2	PR34B[1]/PR52B[1]/VREF2_2	F9
78	DC1_P	T29	P	2	PR34A[1]/PR52A[1]/VREF2_2	E9
82	DD0_M	T31	N	2	PR35B/PR53B	B7
84	DD0_P	T32	P	2	PR35A/PR53A	A7
88	DD1_M	U31	N	2	PR41B/PR59B	D7
90	DD1_P	U32	P	2	PR41A/PR59A	C7
94		V30	N	3	PR44B/PR62B	F7
96		V31	P	3	PR44A/PR62A	E7
100		V28	N	3	PR46B[1]/PR64B[1]	F6
102		U28	P	3	PR46A[1]/PR64A[1]	E6
106		W33	N	3	PR47B/PR65B[1]	D8
108		W34	P	3	PR47A/PR65A[1]	C8
112		W31	N	3	PR50B/PR68B	H6
114		W32	P	3	PR50A/PR68A	G6

1. I/O with true LVDS output capability.
2. I/O description lists both LatticeECP3 –95/–150 density devices.

TI DAC EVM Connector J8

J8 is a high-speed header with 38 differential signal connections for interfacing the LatticeECP3 I/O Protocol Board to a TI DAC5682Z EVM. The connections for J8 are listed in Table 4.

Table 4. TI DAC EVM Connections at J8

J8 Pin	DAC5682Z Signal	LatticeECP3 Pin	Polarity	sysIO Bank	I/O Description[2]	J6 Pin
47	D15P	AP31	P	3	PR92A/PR119A[1]	G5
49	D15N	AN31	N	3	PR92B/PR119B[1]	H5
53	D14P	AL30	P	3	PR91A[1]/PR118A[1]	C4
55	D14N	AM30	N	3	PR91B[1]/PR118B[1]	D4
59	D13P	AJ31	P	3	PR88A[1]/PR115A[1]	C5
61	D13N	AK31	N	3	PR88B[1]/PR115B[1]	D5
65	D12P	AP33	P	3	PR83A/PR110A[1]	A5
67	D12N	AP32	N	3	PR83B/PR110B[1]	B5

Table 4. TI DAC EVM Connections at J8 (Continued)

J8 Pin	DAC5682Z Signal	LatticeECP3 Pin	Polarity	sysIO Bank	I/O Description[2]	J6 Pin
71	D11P	AH33	P	3	PR82A[1]/PR109A[1]	G4
73	D11N	AJ33	N	3	PR82B[1]/PR109B[1]	H4
77	D10P	AD26	P	3	NC/PR106A[1]	A4
79	D10N	AD25	N	3	NC/PR106B[1]	B4
83	D9P	AE30	P	3	PR74A/PR101A[1]	A3
85	D9N	AE29	N	3	PR74B/PR101B[1]	B3
89	D8P	AC28	P	3	NC/PR100A[1]	E4
91	D8N	AB27	N	3	NC/PR100B[1]	F4
95	DCLKP	AM29	P	3	PR97A[1]/PR124A[1]	E5
97	DCLKN	AN29	N	3	PR97B[1]/PR124B[1]	F5
96	CLKOUTP	V29	P	3	PR52A[1]/PR70A[1]/VREF1_3	C6
98	CLKOUTN	W28	N	3	PR52B[1]/PR70B[1]/VREF2_3	D6
101	D7P	AE34	P	3	NC/PR92A[1]	C3
103	D7N	AE33	N	3	NC/PR92B[1]	D3
107	D6P	AD31	P	3	NC/PR91A[1]	E3
109	D6N	AD30	N	3	NC/PR91B[1]	F3
113	D5P	AA28	P	3	PR70A[1]/PR88A[1]	E2
115	D5N	AA27	N	3	PR70B[1]/PR88B[1]	F2
119	D4P	AA31	P	3	PR65A/PR83A[1]	A1
121	D4N	AA30	N	3	PR65B/PR83B[1]	B1
125	D3P	AA25	P	3	PR64A[1]/PR82A[1]	E1
127	D3N	AA26	N	3	PR64B[1]/PR82B[1]	F1
131	D2P	Y26	P	3	PR61A[1]/PR79A[1]	C2
133	D2N	Y25	N	3	PR61B[1]/PR79B[1]	D2
137	D1P	Y34	P	3	PR56A/PR74A[1]	G2
139	D1N	Y33	N	3	PR56B/PR74B[1]	H2
143	D0P	W27	P	3	PR55A[1]/PR73A[1]	C1
145	D0N	W26	N	3	PR55B[1]/PR73B[1]	D1
155	SYNCP	AD33	P	3	NC/PR97A[1]	A2
157	SYNCN	AD34	N	3	NC/PR97B[1]	B2

1. I/O with true LVDS output capability.
2. I/O description lists both LatticeECP3 –95/–150 density devices.

ADC Control Signals Connector J2

There are five additional J10 signals with GND brought over to the ADC control signals header J2, as shown in Table 5.

Table 5. ADC Control Signals at J2

J2 Pin	Signal Name	J10 Pin[1]	Description
1	RST	111	ADC reset when low
2	PDN	113	ADC power down when high
3	SEN	115	ADC serial interface enable
4	SDATA	117	ADC serial interface data
5	SCLK	119	ADC serial interface clock
6	GND	GND	GND

1. Other TI ADC EVM boards may or may not use the same signal locations on J10.

Compatible TI ADC/DAC EVMs

Table 6 lists the TI EVM boards currently known to be compatible with the adapter board, likely to be compatible, and those that are not compatible due to data path connector mismatch or some other reason. The table is provided as supplemental information only and is at this time thought to be accurate. Please refer to the TI web site and TI EVM user's guides for the most accurate up to date information about any TI EVM you might be considering for use with this adapter.

Table 6. Compatible TI ADC/DAC EVMs

TI EVM	Type	Compatible
ADS64XX	ADC	Yes
ADS62XX	ADC	Yes
DAC5681/81z/82z	DAC	Yes
ADS62PXX	ADC	Likely
ADS61X9/55XX	ADC	Likely
ADS548X	ADC	Likely
ADS5440/44/63/74	ADC	Likely
DAC5686/88/89	DAC	No
DAC5687	DAC	No
THS56XX	DAC	No
DEM-DAC90x	DAC	No
DAC5674/75	DAC	No
DAC290x	DAC	No
DAC5672/62/52	DAC	No

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
November 2014	1.3	Corrected descriptions for J10 pin 94-114 in Table 3, TI ADC EVM Connections at J10.
		Corrected descriptions for J8 pins 53,55,77,79,143,145 in Table 4, TI DAC EVM Connections at J8.
		Updated corporate logo.
		Updated Technical Support Assistance section.
May 2010	01.2	Added new figure - LatticeECP3 I/O Protocol Board Connected to TI ADC DAC EVMs.
April 2010	01.1	Added Compatible TI ADC/DAC EVMs text section and table.
March 2010	01.0	Initial release.

Appendix A. Schematic

Figure 3. LatticeECP3 I/O Protocol Board to TI ADC/DAC Adapter Board

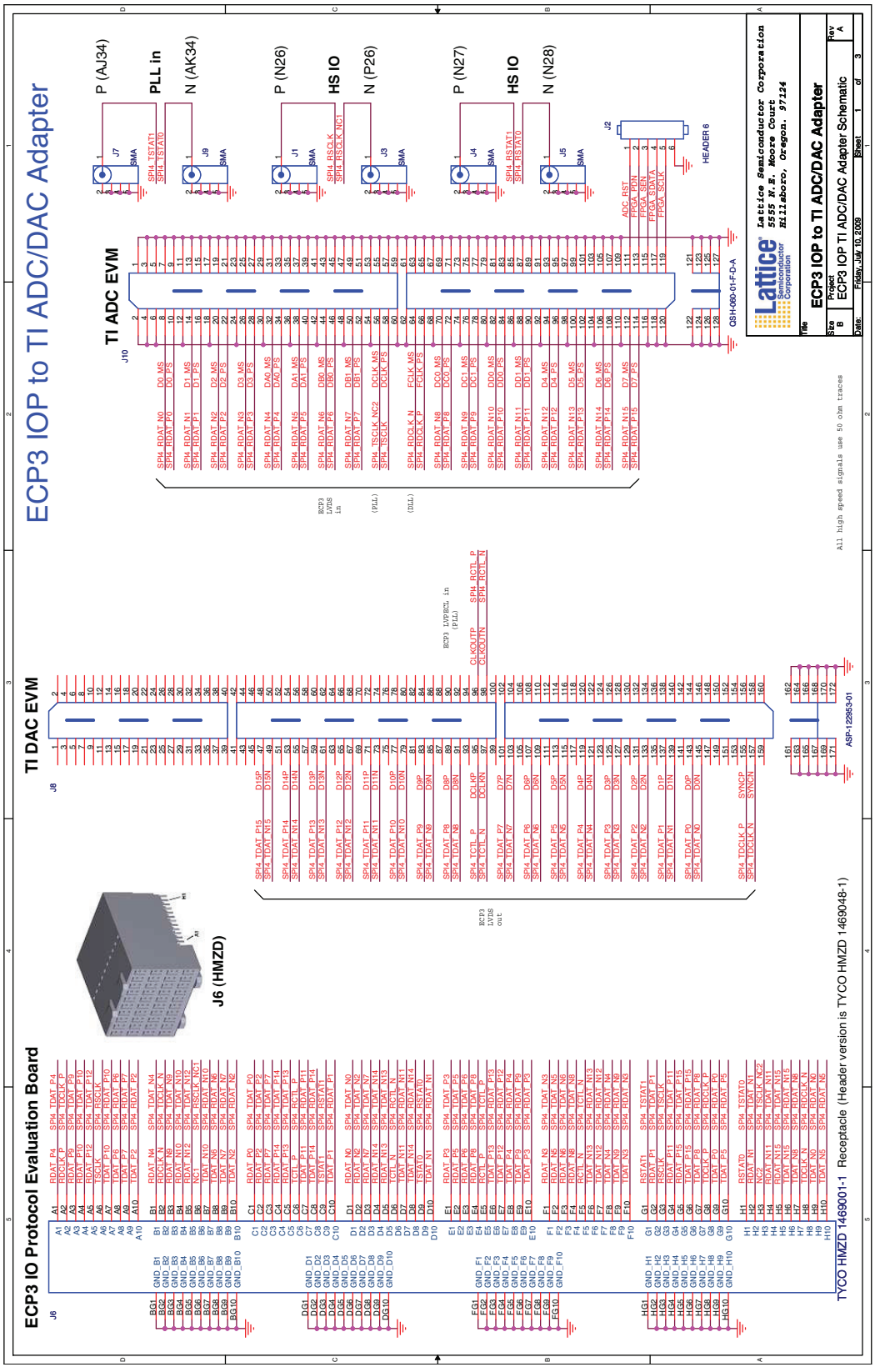


Figure 4. Mechanical Drawing

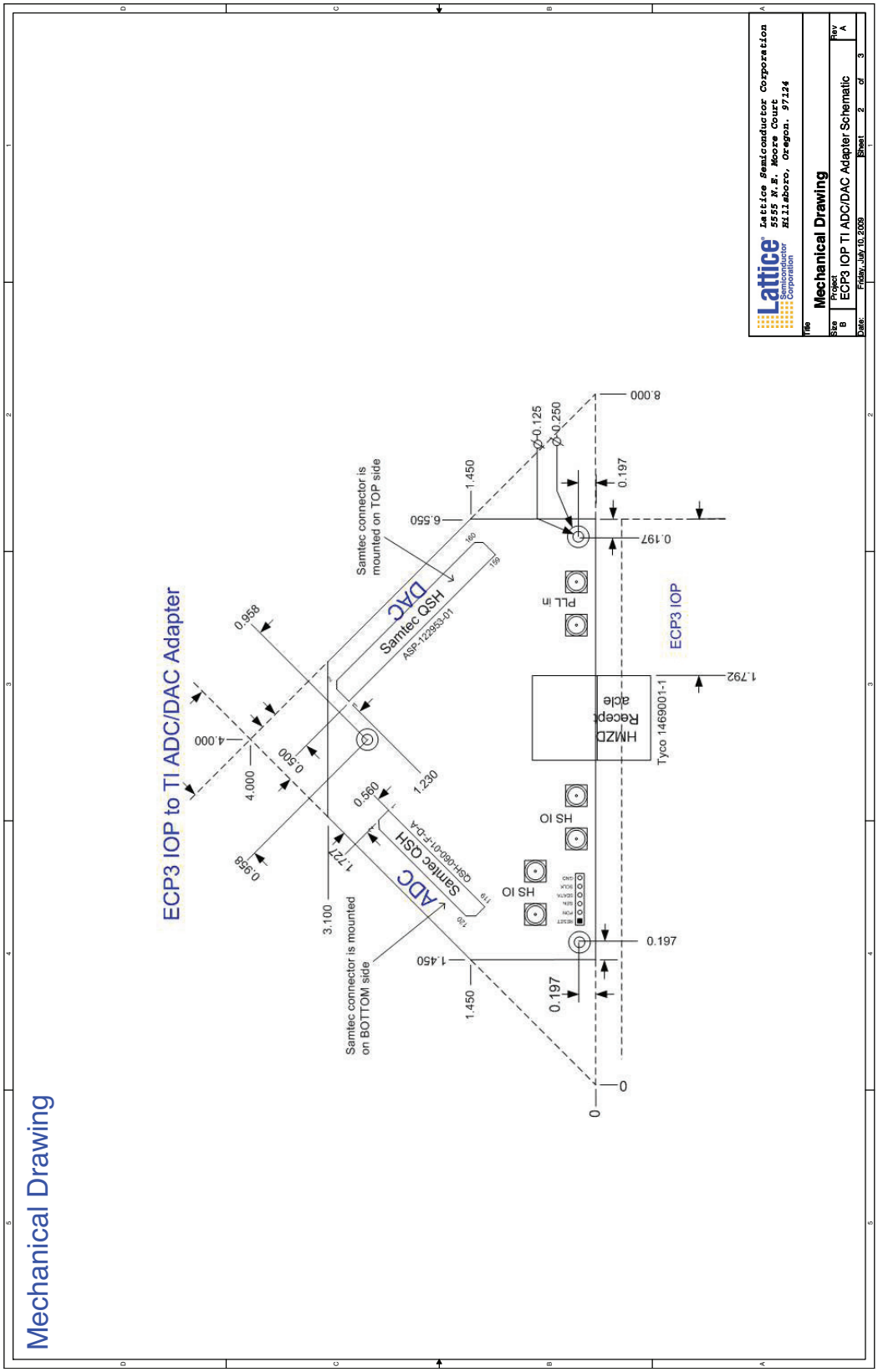


Figure 5. Mechanical Drawing