RELIABLE RESET GENERATION FOR

TI TMS320C6XXX ("DAVINCI") PROCESSORS

A Lattice Semiconductor White Paper

March 2010

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Introduction

Modern fabrication technologies facilitate the acceleration of processor throughput by enabling the integration of board-level functions, such as SERDES interface, memory interface and multiple types of processors, on a single chip. One of the direct results of fine transistor geometries is lower core power supply voltages, such as 1.2V. However, peripherals require their own power supply levels, depending on the communication interface type. As a result, multiple supply voltages are required to power these devices. Texas Instruments' fixed and floating point DSPs, like the TMS320C6x family, also require multiple supply voltages.

Every microprocessor or DSP requires a reset generator circuit or IC to perform two functions: (1) start up from a fixed condition after the supplies are turned on, and (2) prevent the processor from executing instructions incorrectly and causing flash memory corruption when their power supplies are lower than the specified operating level. Traditional, simple, single-supply reset generators were adequate for single supply processors, but no longer are sufficient to guarantee reliable operation of multiple supply processors like the TMS320C6x. This white paper examines some of the challenges associated with resetting modern day processors.

TMS320C6XXX Processor Power Requirements

Increasingly, newer members of the TMS320 DSP family integrate multiple peripherals within the processor chip. Because of these peripherals, these processors have additional power supply requirements. For example, the integrated DDR memory interface requires a 1.8V supply and a 0.9V reference voltage for a SSTL18 interface. In addition, all processors require a standard 3.3V I/O interface supply and core power supply.

The TI Design Guide for the TMS320 DSP specifies that the core power supply be capable of sourcing 1.0V, 1.05V, 1.1V, 1.14V, 1.2V or 1.26V to be compatible with

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future releases of the devices. The voltage rating of these supplies should be 3%. In addition the reset generator is required to wait for the clock to be stable before releasing the reset.

Most TMS320 processors also provide emulation support. As a result, two types of reset signals must be provided: Power on reset (POR pin) and Warm reset (RESET pin). The Power on reset signal is activated when both the processor and the emulation sections are to be reset. The Warm reset, however, resets only the processor and not the emulation section. The reset generator should support both reset signals. The datasheet also specifies that the Warm reset (RESET pin) should be activated when an external watchdog timer expires.

Traditional Reset Generation Circuit Drawbacks

A traditional reset generator IC has one analog voltage monitoring input and a digital output that resets the microprocessor. The threshold is set 5% or 10% below the nominal voltage level. For example, the threshold voltage of a reset generator monitoring a 3.3V supply is 3.3 – 10% = 3V. This device holds the processor in reset condition until the supply voltage is above 3V. During operation, the reset generator reactivates the reset signal of the processor when the supply voltage drops below 3V. This is fine for a processor that requires only a 3.3V supply.

Figure 1 shows a TMS320 processor connected to a DDRII memory interface. As a result, there are four supply voltages in this system: 3.3V, 1.8V, 1.2V and 0.9V.
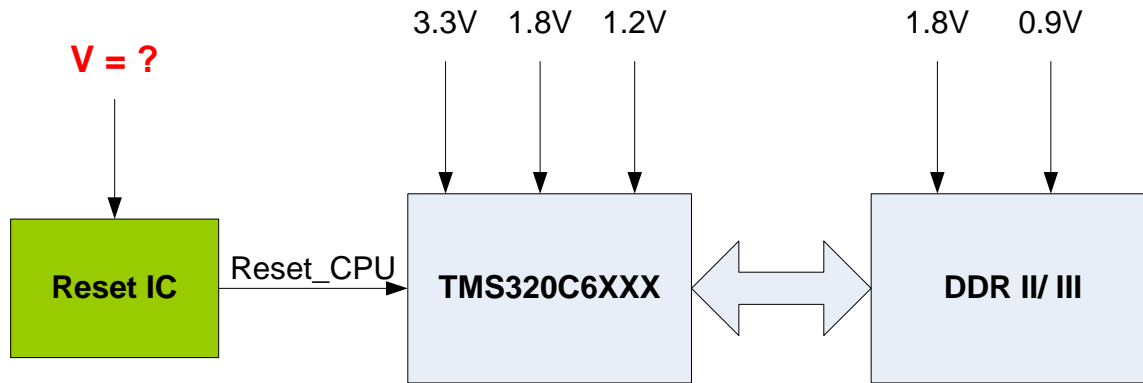
Figure 1 - A reset generator should monitor all the supplies connected to the processor and memory

A single supply reset IC clearly cannot deterministically reset the processor. This system requires at least 3 supply monitoring reset ICs. The most reliable system will require monitoring of even the 0.9V supply.

Need for Higher Monitoring Accuracy

Typical range for the core supply voltage for a processor (e.g., 1.2V) is +/- 5%. The reset generator should monitor for a voltage of 1.14V. So, a reset generator with 0% error will be able to monitor a voltage of exactly -5%. But if the error of the reset generator is 1%, it will activate the reset to CPU from 1.2V-4% to 1.2V-6%. Usually this is acceptable. But if the reset generator has an error of 3%, then it will flag errors from 1.2V-2% to 1.2V-8%. So, it will flag error prematurely and, with potential danger, allow the processor to operate when its supply is faulty.

In order to reliably reset the processor, the reset generator should monitor all supplies with an accuracy of 1% or better to meet the specifications of the processor.

Internal or External Watchdog Timer?

The TMS320 processor provides a 64-bit watchdog timer to support a wide range of watchdog timer delays. This watchdog timer value is set by software to a required value during the initialization phase. However, many designers feel that an external, slower

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hardware watchdog timer, which cannot be changed by the processor; is necessary as a backup The backup watchdog timer reactivates the processor in case the on-processor watchdog timer setting is corrupted due to software error .

An ideal companion device for modern processors and DSPs is one that integrates multiple supply monitoring and reset generation and provides reprogrammable logic and timers. This is because such a device increases reliability by providing expanded supply monitoring, external watchdog timer circuits and improved accuracy.

Proposed Reset Generation Circuit

Here is a summary of the requirements for a reliable reset generator for a TMS320C6XXX ("DaVinci") processor:

- Wait for all four supplies and clock present signals before releasing the power on reset (POR pin)
- Activate Power-on reset if any of the supplies are below their respective thresholds, or if the clock is removed
- After power on, if manual reset input is activated, activate only the warm reset (RESET pin)
- If the watchdog timer expires, activate warm reset (RESET pin)

All these features are supported by Lattice Semiconductor's ProcessorPM POWR605 device. Figure 2 shows the reset generation for a TMS320C6XXX ("DaVinci") processor.
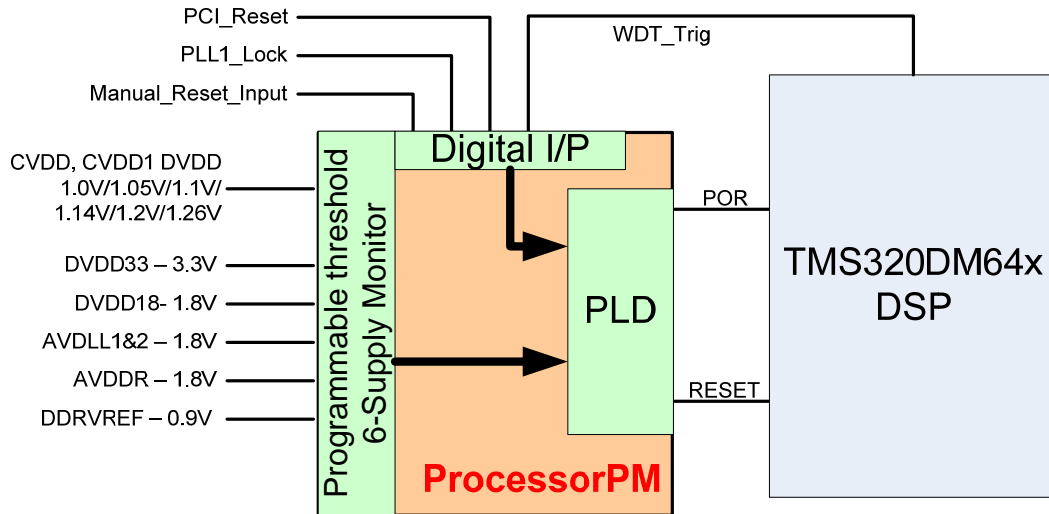
Figure 2 - Reset generation for a TMS320 processor using ProcessorPM

The ProcessorPM device is a low-cost, 6-supply voltage monitoring device with two digital inputs and five digital I/O pins. The logic to control the output pins is implemented in the on-chip 16-macrocell PLD. The ProcessorPM device can be used as a standard reset generator and watchdog timer IC across a wide range of processors and DSPs. The ProcessorPM device also integrates multiple timers, which can be used to implement watchdog timer delays of milliseconds to minutes. Board-specific design can be programmed into the device using the JTAG interface.

The voltage monitoring thresholds can be programmed into the 6-supply monitor block. The exact value of the monitoring threshold can be selected using 192 steps. The accuracy of the voltage monitoring thresholds is 0.7%. In this example, the thresholds are set to 0.9V-5%, 1.8V-5% (3 separate supplies), 3.3V-5% and 1V-5%. The core voltage threshold can be changed to meet the actual core voltage value, depending on the version and speed of the processor.

The digital inputs of the ProcessorPM device are connected to manual reset input, PLL_Lock signal (input clock frequency is correct), PCI_reset and watchdog timer trigger. The ProcessorPM device generates the POR signal as well as the RESET

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signal. The PCI_Reset and the Manual Reset input signals activate the RESET signal.
The RESET signal is also activated when the watchdog timer expires. The POR signal
is activated during power-up and power fault conditions.

Software-Based Design and Evaluation Hardware

Reprogrammable devices like the ProcessorPM are designed via software tools rather
than static external circuits like pin straps. Software interfaces provide a means to vary
threshold voltages, watchdog timer period and output logic. This ensures the device
can be adapted to various TMS320 models. This versatility is attractive both to
designers and procurement managers who are seeking ways to reduce the variety of
power management devices to be stocked and qualified. The ProcessorPM provides a
JTAG programming interface, making in-system changes easy.

ProcessorPM designs can be implemented with Lattice's user friendly, intuitive PAC-
Designer software. This software also supports simulation capabilities that let the
designer verify the design before programming the device. The PAC-Designer software
can be downloaded for free from the Lattice semiconductor website
www.latticesemi.com.

The ProcessorPM Development Kit can be used to verify the design in hardware before
implementation in the actual circuit board. The development kit also is available from
the Lattice on-line store.

Advantages of the Proposed Reset Generation Solution

Multiple single voltage reset generator ICs are required to provide a reliable reset
solution for the TMS320C6XXX ("DaVinci") processors. The drawback of most low-cost
off the shelf single supply ICs is unacceptably high voltage monitoring error. Accurate
voltage supervisor ICs are expensive. Designers have to use a different reset generator
IC to monitor different core voltages, depending on the version and speed of operation
of the TMS320C6XXX (DaVinci) processors.

The ProcessorPM devices provide the most reliable, low-cost, single chip solution as they cover all the supply rails for accurate fault monitoring and offer multiple outputs to support Power-on-reset and Warm reset functions. In addition, the same device can be used to monitor a different core voltage when a different TMS320C6XXX processor is used.

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