Generic Macro Library Reference Manual

March 2018

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Type Conventions Used in This Document

Convention	Meaning or Use
Bold	Items in the user interface that you select or click. Text that you type into the user interface.
<*Italic*>	Variables in commands, code syntax, and path names.
Ctrl+L	Press the two keys at the same time.
`Courier`	Code examples. Messages, reports, and prompts from the software.
`...`	Omitted material in a line of code.
`.` `.` `.`	Omitted lines in code and report examples.
`[ ]`	Optional items in syntax descriptions. In bus specifications, the brackets are required.
`( )`	Grouped items in syntax descriptions.
`{ }`	Repeatable items in syntax descriptions.
`|`	A choice between items in syntax descriptions.

Contents

Arithmetic Functions

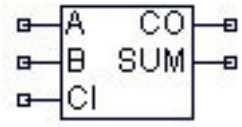
This chapter contains information on the following macros:

- Adders

Adders

G_FADD

G_FADD



Function

G_FADD: 1-bit full adder.

Type

Soft

Logic Resources

Table 1:

Macro	PT	Macrocell	Output	Level
G_FADD	*	2	2	1

* Z0: 3 PTC0: 3PT

Truth Table

Table 2:

Input			Output	
A	B	CI	CO	SUM
data	data	0	*	A+B
data	data	1	**	A+B+1

* If $A + B < 2^n$, CO=0. If $A + B \geq 2^n$, CO=1.

** If $A + B + 1 < 2^n$, CO=0. If $A + B + 1 \geq 2^n$, CO=1.

G_HADD

G_HADD

Function

G_HADD: 1-bit half adder.

Type

Soft

Logic Resources

Table 3:

Macro	PT	Macrocell	Output	Level
G_FADD	*	2	2	1

* Z0: 2 PTC0: 1PT

Truth Table

Table 4:

Input			Output	
A	B	CI	CO	SUM
data	data	1	*	A+B

* If $A + B < 2^n$, CO=0. If $A + B \geq 2^n$, CO=1.

I/O Pins

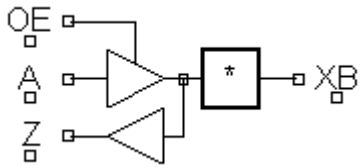
This chapter contains information on the following macros:

- Bidirectional Pin
- Input Pin
- Output Pins

Bidirectional Pin

G_BIDIR

G_BIDIR



Function

G_BIDIR: 1-bit bidirectional pin.

Type

Hard

Truth Table

Do not drive XB when OE=1.

Table 5:

Input			Output	
OE	A	B	XB	Z
0	x	d	-	d
0	x	Z	-	X
1	d	Z	d	d

D = any pattern of 1s and 0s on an input or set of inputs, x = don’t care,

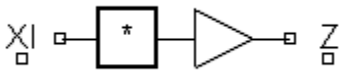
X = X (unknown) state, Z = high impedance state,

- = appears in output column if a dibirectional pin acts as an input pin.

Input Pin

G_INPUT

G_INPUT



Function

G_INPUT: 1-bit input pin.

Type

Hard

Truth Table

Table 6:

Input	Output
XI	Z
d	d

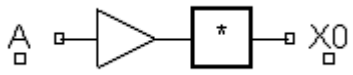
d = any pattern of 1s and 0s on an input or set of inputs,

XI = external input pin, Z = output.

Output Pin

G_OUTPUT

G_OUTPUT



Function

G_OUTPUT: 1-bit output pin.

Type

Hard

Truth Table

Table 7:

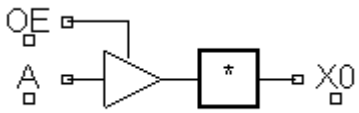
Input	Output
A	X0
d	d

d = any pattern of 1s and 0s on an input or set of inputs.

Tri-state Output Pin

G_TRI

G_TRI



Function

G_TRI: 1-bit tri-state output pin.

Type

Hard

Truth Table

Table 8:

Input		Output
OE	A	X0
0	x	Z
1	D	d

d = any pattern of 1s and 0s on an input or set of inputs,

x = don’t care, Z = high impedance state.

Logic Gates

This chapter contains information on logic gate macros.

AND Gates

2AND, 2AND1, 2AND2

G_2ANDG_2AND1G_2AND2

Function

G_2AND, G_2AND1, G_2AND2: 2 input AND gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic primitive.

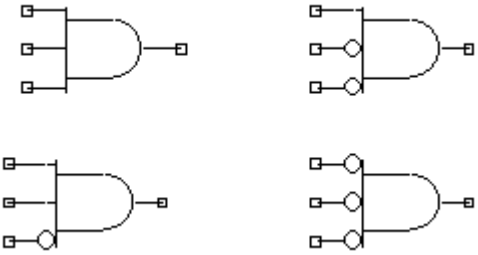
Truth Table

Table 9:

Inputs		2AND	2AND1	2AND2
0	0	0	0	1
0	1	0	0	0
1	0	0	1	0
1	1	1	0	0

3AND, 3AND1, 3AND2, 3AND3

G_3ANDG_3AND2



G_3AND1G_3AND3

Function

G_3AND, G_3AND1, G_3AND2: 3 input AND gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic primitive.

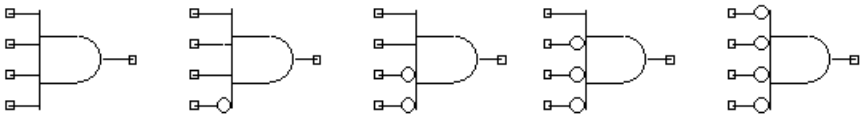
Truth Table

Table 10:

Inputs			3AND	3AND1	3AND2	3AND3
0	0	0	0	0	0	1
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	1	0
1	0	1	0	0	0	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

4AND, 4AND1, 4AND2, 4AND3, 4AND4

G_4ANDG_4AND1G_4AND2G_4AND3G_4AND4



Function

G_4AND, G_4AND1, G_4AND2, G_4AND3, G_4AND4: 4 input AND gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic primitive.

Truth Table

Table 11:

Inputs				4AND	4AND1	4AND2	4AND3	4AND4
0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0
1	1	1	1	1	0	0	0	0

OR Gates

2OR, 2OR1, 2OR2

G_2ORG_2OR1G_2OR2

Function

G_2OR, G_2OR1, G_2OR2: 2 input OR gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic primitive.

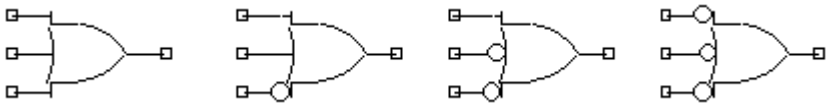
Truth Table

Table 12:

Inputs		2OR	2OR1	2OR2
0	0	0	0	1
0	1	1	0	1
1	0	1	1	1
1	1	1	1	0

3OR, 3OR1, 3OR2, 3OR3

G_3ORG_3OR1G_3OR2G_3OR3



Function

G_3OR, G_3OR1, G_3OR2, G_3OR3: 3 input OR gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic primitive.

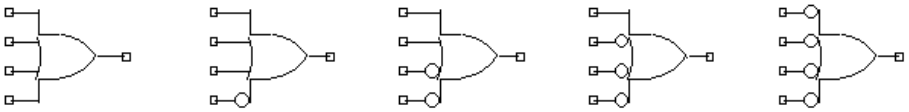
Truth Table

Table 13:

Inputs			3OR	3OR1	3OR2	3OR3
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	1	1
0	1	1	1	1	0	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	0

4OR, 4OR1, 4OR2, 4OR3, 4OR4

G_4ORG_4OR1G_4OR2G_4OR3G_4OR4



Function

G_4OR, G_4OR1, G_4OR2, G_4OR4: 4 input OR gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic primitive.

Truth Table

Table 14:

Inputs				4OR	4OR1	4OR2	4OR3	4OR4
0	0	0	0	0	1	1	1	1
0	0	0	1	1	0	1	1	1
0	0	1	0	1	1	1	1	1
0	0	1	1	1	1	0	1	1
0	1	0	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	1
1	0	0	0	1	1	1	1	1
1	0	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	1	0

NAND Gates

2NAND, 2NAND1, 2NAND2

G_2NANDG_2NAND1G_2NAND2

Function

G_2NAND, G_2NAND1, G_2NAND2: 2 input NAND gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic Primitive.

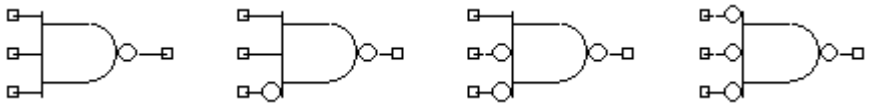
Truth Table

Table 15:

Inputs		2NAND	2NAND1	2NAND2
0	0	1	1	0
0	1	1	1	1
1	0	1	0	1
1	1	0	1	1

3NAND, 3NAND1, 3NAND2, 3NAND3

G_3NANDG_3NAND1G_3NAND2G_3NAND3



Function

G_3NAND, G_3NAND1, G_3NAND2, G_3AND3: 3 input NAND gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

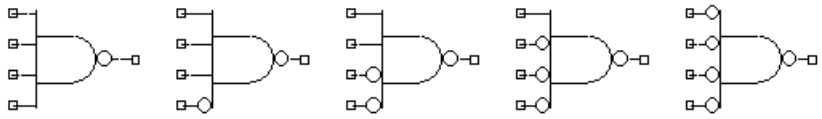
Logic Primitive.

Truth Table

Inputs			3NAND	3NAND1	3NAND2	3NAND3
0	0	0	1	1	1	0
0	0	1	1	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	1	0	1
1	0	1	1	1	1	1
1	1	0	1	0	1	1
1	1	1	0	1	1	1

4NAND, 4NAND1, 4NAND2, 4NAND3, 4NAND4

G_4NANDG_4NAND1G_4NAND2G_4NAND3G_4NAND4



Function

G_4NAND, G_4NAND1, G_4NAND2, G_4NAND3, G_4NAND4: 4 input NAND gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic Primitive.

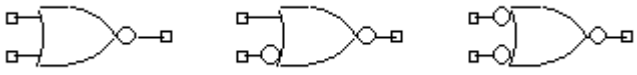
Truth Table

Inputs				4NAND	4NAND1	4NAND2	4NAND3	4NAND4
0	0	0	0	1	1	1	1	0
0	0	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	0	1
1	0	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	0	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	1	0	1	1	1
1	1	1	1	0	1	1	1	1

NOR Gates

2NOR, 2NOR1, 2NOR2

G_2NORG_2NOR1G_2NOR2



Function

G_2NOR, G_2NOR1, G_2NOR2: 2 input NOR gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

Logic Primitive.

Truth Table

Inputs		2NOR	2NOR1	2NOR2
0	0	1	0	0
0	1	0	1	0
1	0	0	0	0
1	1	0	0	1

3NOR, 3NOR1, 3NOR2, 3NOR3

G_3NORG_3NOR1G_3NOR2G_3NOR3

Function

G_3NOR, G_3NOR1, G_3NOR2, G_3NOR3: 3 input NOR gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

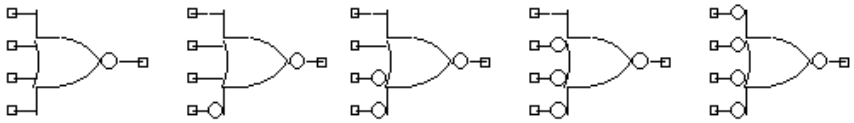
Logic Primitive.

Truth Table

Inputs			3NOR	3NOR1	3NOR2	3NOR3
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

4NOR, 4NOR1, 4NOR2, 4NOR3, 4NOR4

G_4NORG_4NOR1G_4NOR2G_4NOR3G_4NOR4



Function

G_4NOR, G_4NOR1, G_4NOR2, G_4NOR3, G_4NOR4: 4 input NOR gates.

Note: Bubble(s) on the input(s) mean inverted input(s).

Type

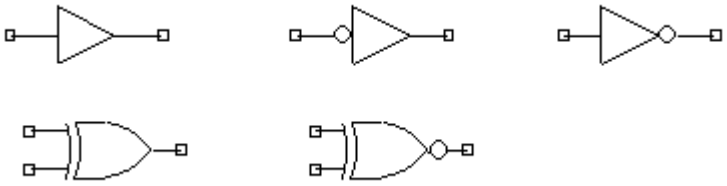
Logic Primitive.

Truth Table

Inputs				4NOR	4NOR1	4NOR2	4NOR3	4NOR4
0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	0	1	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	1	0
1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	1

BUF, INV, XOR, XNOR

G_BUFG_BUFBG_INV



G_XORG_XNOR

Function

G_BUF: single input buffer.

G_BUFB: single inverted input buffer.

G_INV: single input inverter.

G_XOR: 2 input exclusive OR gate.

G_XNOR: 2 input exclusive NOR gate.

Type

Logic Primitive.

Truth Table

Input	G_BUF	G_BUFB	G_INV
0	0	1	1
1	1	0	0

Inputs		XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

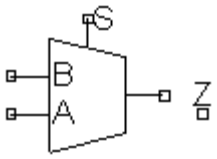
Multiplexers

This chapter contains information on the following macros:

- 2-to-1 multiplexer
- 4-to-1 multiplexer
- 8-to-1 multiplexer

MUX21

G_MUX21



Function

G_MUX21: 2 input multiplexer with 1 select line.

Type

Soft

Logic Resources

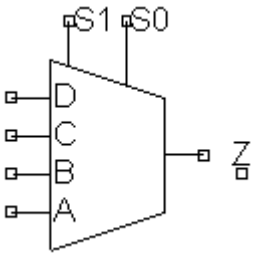
Macro	PT	Macrocell	Output	Level
G_MUX21	2	1	1	1

Truth Table

Input	Output
S	Z
0	A
1	B

MUX41

G_MUX41



Function

G_MUX41: 4 input multiplexer with 2 select line.

Type

Soft

Logic Resources

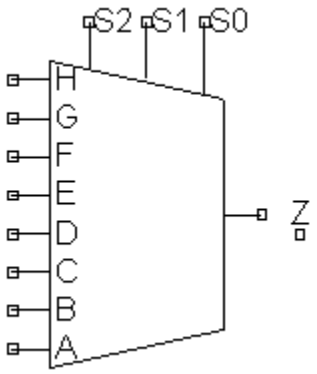
Macro	PT	Macrocell	Output	Level
G_MUX41	4	1	1	1

Truth Table

Input		Output
S1	S0	Z
0	0	A
0	1	B
1	0	C
1	1	D

MUX81

G_MUX81



Function

G_MUX81: 8 input multiplexer with 3 select line.

Type

Soft

Logic Resources

Macro	PT	Macrocell	Output	Level
G_MUX81	8	2	1	1

Truth Table

Input			Output
S2	S1	S0	Z
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

Registers

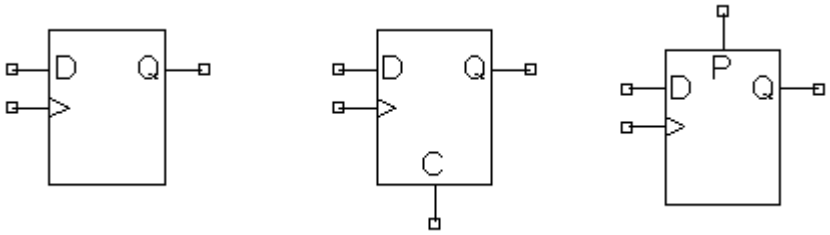
This chapter contains information on the following macros:

- D Flip-Flops
- JK Flip-Flops
- Toggle Flip-Flops
- D Latches
- SR Latches

D Flip-Flops

G_D, G_DC, G_DP

G_DG_DCG_DP



Function

G_D: 1-bit D flip-flop.

G_DC: 1-bit D flip-flop with synchronous clear.

G_DP: 1-bit D flip-flop with synchronous preset.

Type

Logic Primitive.

Logic Resources

Macro	PT	Macrocell	Output	Level
G_D	1*	1	1	1
G_DC	1*	1	1	1
G_DP	2*	1	1	1

* Add 1 PT per GLB if Product Term Clock is used.

Truth Table

Input				**Output (Q0~Q $_{n-1}$)**		
D0~D $_{n-1}$	CLK	C	P	G_D	G_DC	G_DP
x	¦	1	1	-	0	1
d	¦	0	0	d	d	d
x	0	0	x	Q0’~Qn’	Q0’~Qn’	Q0’~Qn’
x	1	0	x	Q0’~Qn’	Q0’~Qn’	Q0’~Qn’

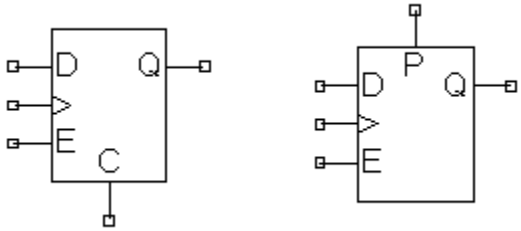
d = any pattern of 1s and 0s in an input or set of inputs,

Q0’~Qn’ = previous output of flip-flop or latch, - = not apply,

x = don’t care, ↑ = rising clock edge.

G_DEC, G_DEP

G_DECG_DEP



Function

G_DEC: 1-bit D flip-flop with synchronous clear and enable.

G_DEP: 1-bit D flip-flop with synchronous preset and enable.

Type

Soft

Logic Resources

Macro	PT	Macrocell	Output	Level
G_DEC	1*	1	1	1
G_DEP	2*	1	1	1

* Add 1 PT per GLB if Product Term Clock is used.

Truth Table

Input				Output (Q0~Q_{n-1})	
D0~D_{n-1}	CLK	C	P	G_DEC	G_DEP
x	↑	1	1	0	1
d	↑	0	0	d	d
x	0	0	x	Q0'~Qn'	Q0'~Qn'
x	1	0	x	Q0'~Qn'	Q0'~Qn'

d = any pattern of 1s and 0s in an input or set of inputs,

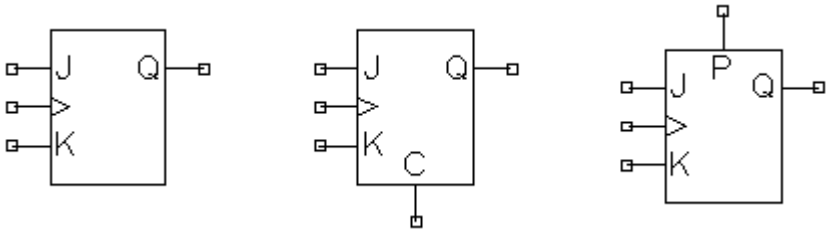
Q0'~Qn' = previous output of flip-flop or latch,

x = don't care, ↑ = rising clock edge.

JK Flip-Flops

G_JK, G_JKC, G_JKP

G_JKG_JKCG_JKP



Function

G_JK: JK flip-flop.

G_JKC: JK flip-flop with synchronous clear.

G_JKP: JK flip-flop with synchronous preset.

Type

Soft

Logic Resources

Macro	PT	Macrocell	Output	Level
G_JK	2*	1	1	1
G_JKC	2*	1	1	1
G_JKP	2*	1	1	1

* Add 1 PT per GLB if Product Term Clock is used.

Truth Table

Input					Output
P	C	J	K	CLK	Q
x	1	x	x	x	0
0	0	0	0	↑	Q0’
0	0	0	1	↑	0
0	0	1	0	↑	1
0	0	1	1	↑	$\bar{Q}$0’
x	0	x	x	0	Q0’
x	0	x	x	1	Q0’
1	0	x	x	↑	1

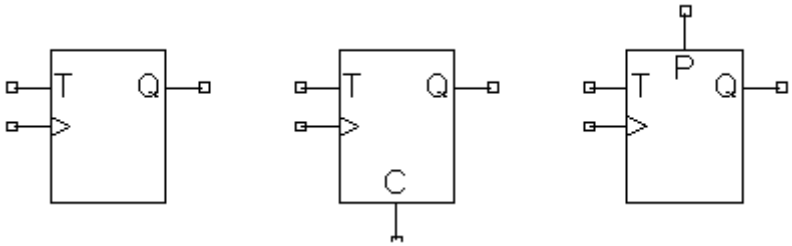
Q0’ = previous output of flip flop, $\bar{Q}$0’ = inverse of Q0’,

X=don’t care, ↑ = rising clock edge

Toggle Flip-flop

G_T, G_TC, G_TP

G_TG_TCG_TP



Function

G_T: Toggle flip-flop.

G_TC: Toggle flip-flop with synchronous clear.

G_TP: Toggle flip-flop with synchronous preset.

Type

Soft

Logic Resources

Macro	PT	Macrocell	Output	Level
G_T	3*	1	1	1
G_TC	3*	1	1	1
G_TP	3*	1	1	1

* Add 1 PT per GLB if Product Term Clock is used.

Truth Table

Input				Output
P	C	T	CLK	Q
1	x	x	¦	1
0	1	x	¦	0
0	0	0	¦	Q0’
0	0	1	¦	$\bar{Q}$0’
x	x	x	0	Q0’
x	x	x	1	Q0’

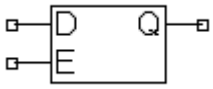
Q0’ = previous output of flip flop, $\bar{Q}$0’=inverse of Q0’,

X=don’t care, ↑ = rising clock edge

D Latches

G_LATCH

G_LATCH



Function

G_LATCH: 1-bit D latch with enable.

Type

Hard

Logic Resources

Macro	PT	Macrocell	Output	Level
G_LATCH	3	1	1	1

Truth Table

Input		Output
D0~D $_{n-1}$	E	Q0~Q $_{n-1}$
d	1	d
x	0	Q0'~Qn'

d = any pattern of 1s and 0s in an input or set of inputs,

Q0'~Qn' = previous output of flip-flop or latch,

x = don't care.

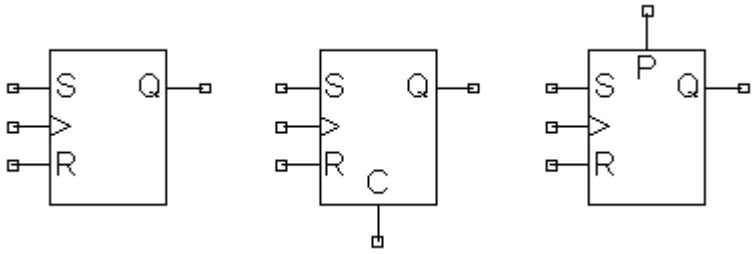
NOTE:

The Truth Table was changed in March, 2018. It previously had 1 in the x row. The 1 has been changed to 0.

SR Latches

G_RS, G_RSC, G_RSP

G_RSG_RSCG_RSP



Function

G_RS: simple SR latch.

G_RSC: simple SR latch with synchronous clear.

G_RSP: simple SR latch with synchronous preset.

Type

Soft

Logic Resources

Macro	PT	Macrocell	Output	Level
G_RS	2	1	1	1
G_RSC	2	1	1	1
G_RSP	2	1	1	1

Truth Table

Input				Output
P	C	S	R	Q
0	0	0	0	Q
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1*
1	0	x	x	1
0	1	x	x	0

* These outputs are not entirely stable. They may not remain when both S and R return to 1.