Generating a Single-Ended Clock Source from ispClock5400D Differential Clock Buffers

January 2010 **Reference Design RD1069**

Introduction

The Lattice ispClock™ product line features three clock families, ispClock5300S, ispClock5400D, and ispClock5600A, that provide a wide range of solutions for clocking applications. The clock solution includes but is not limited to frequency generation, zero delay buffer, and programmable I/O interfaces. Among the three clock families, the ispClock5400D is unique in terms of its CleanClock™ PLL and FlexiClock™ output block. The CleanClock PLL supports the ultra-low jitter performance required by high-speed communication applications. The FlexiClock output block supports six differential I/O interfaces and flexible phase and time delay adjustments for each output. The ispClock5400D is a low-cost integrated clock solution for high-performance applications that uses low-cost CMOS oscillators as clock input.

In applications where single-ended LVTTL/LVCMOS clock source and ultra-low jitter is required, the ispClock5400D family can be used to take advantage of the CleanClock PLL. This document discusses the steps necessary to generate a single-ended clock source from an ispClock5400D device.

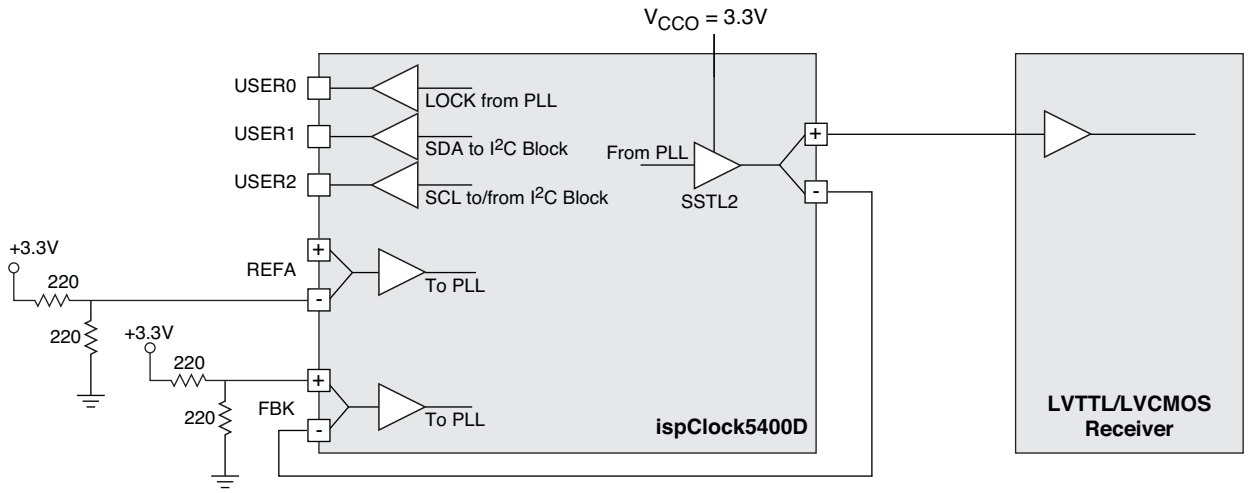
Features

- Low-jitter LVTTL/LVCMOS single-ended clock source
- Zero-delay clock buffer
- Programmable time and phase skew
- Dynamic device control through I^2C

Functional Description

The SSTL2 I/O logic standard of the ispClock5400D is used to generate the single-ended clock source. Figure 1 is the suggested hardware connection of the design. The figure shows the I/O buffer configurations and connections only.

Figure 1. Hardware Connection



Conceptually, the SSTL and LVCMOS drivers are equivalent since both consist of a pull-up PMOS and pull-down NMOS. The difference in the driver behavior is determined by the off-chip termination circuitry. The LVTTL/LVCMOS input and output specifications are defined in JESD8C, the JEDEC standard for Nominal 3.0V/3.3V Supply

Digital Integrated Circuits. Tables 1 and 2 are the LVTTL and LVCMOS V_{OH} and V_{OL} specifications, extracted from JESD8C.

Table 1. LVTTL Output Specifications (Table 3 of JESD8C.01)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH}	Output High Voltage	V_{DD} = Min., I_{OH} = -2 mA	2.4		V
V_{OL}	Output Low Voltage	V_{DD} = Min., I_{OL} = 2 mA		0.4	V

3.3V nominal supply: $V_{DD(min)}$ = 3.0V and $V_{DD(max)}$ = 3.6V
3.3V nominal supply: $V_{DD(min)}$ = 3.15V and $V_{DD(max)}$ = 3.45V

Table 2. 3.3V LVCMOS Output Specifications (Table 4 of JESD8C.01)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH}	Output High Voltage	V_{DD} = Min., I_{OH} = -100 µA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = Min., I_{OL} = -100 µA		0.2	V

3.0V nominal supply: $V_{DD(min)}$ = 2.7V and $V_{DD(max)}$ = 3.6V
3.3V nominal supply: $V_{DD(min)}$ = 3.0V and $V_{DD(max)}$ = 3.6V
3.3V nominal supply: $V_{DD(min)}$ = 3.15V and $V_{DD(max)}$ = 3.45V

Based on the characterization data of the SSTL2 I/O logic at V_{CCO} values of 2.3V, 2.5V, and 2.7V, the V_{OH} and V_{OL} at V_{CCO} values of 3.0V can be calculated through linear extrapolation of the data.

Table 3. Expected V_{OH} and V_{OL} Behavior of SSTL2 at V_{CC} = 3.0V

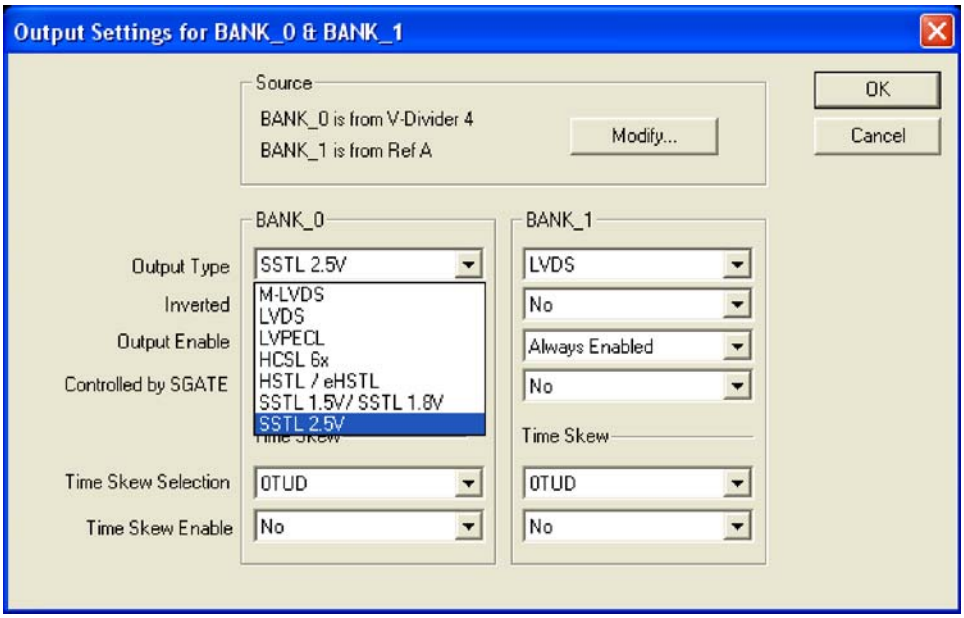
	V_{OH} Min. (V)			V_{OL} Max. (V)		
V_{CCO} (V)	I_{OH} = 8 mA	I_{OH} = 2 mA	I_{OH} = 100 µA	I_{OL} = 8 mA	I_{OL} = 2 mA	I_{OL}= 100 µA
2.3	2.10	2.25	2.298	0.18	0.04	0.002
3.0	2.84	2.96	2.998	0.16	0.04	0.002

Table 3 shows the V_{OH} and V_{OL} values under different load conditions. The 100 µA and 2 mA are based on the test conditions specified in JESD8C for 3.3V LVCMOS and LVTTL respectively, and in the JESD8-5A for 2.5V LVCMOS. The 8 mA condition is based on the existing SSTL2 characterization data. It shows that at a load of 8 mA the V_{OL} can still meet the 0.2V requirement of the LVCMOS specification. As most of the FPGA/CPLD LVTTL/LVCMOS I/Os have more relaxed V_{IH} min. and V_{IL} max. requirements, the result in Table 3 provides a sufficient margin for interfacing to LVTTL, LVCMOS 3.3 or LVCMOS2.5 receivers.

Design Description

This design is implemented using Lattice PAC-Designer® software. Bank 0 is configured to be SSTL2 I/O logic. Figure 2 shows the selection of the output type in an I/O bank in PAC-Designer. Banks that are not being used for single-ended applications can be configured as differential outputs to drive high-speed clock signals.

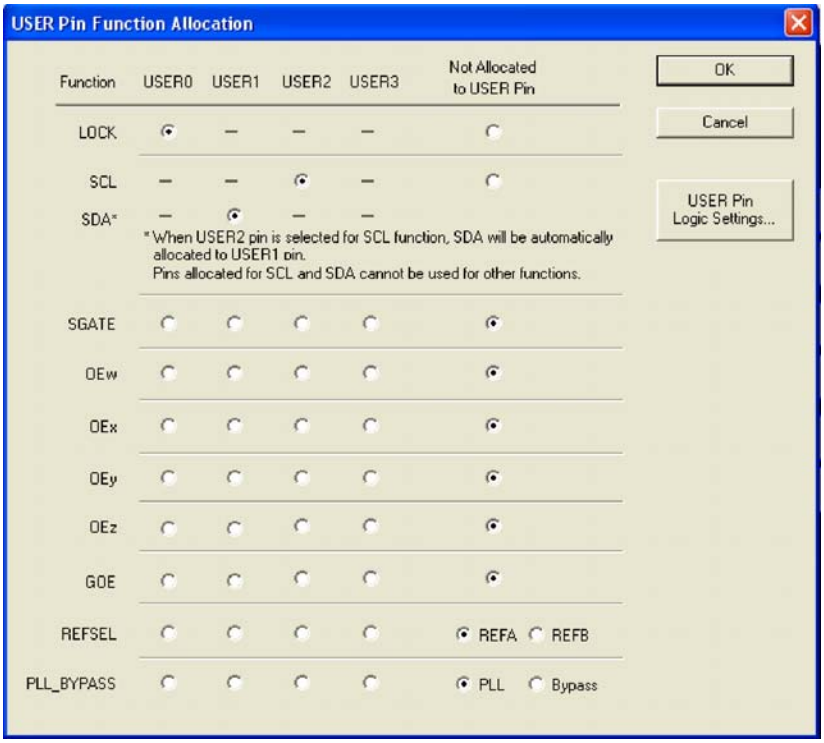
Figure 2. Selecting SSTL 2.5V for Bank 0



The external PLL feedback is used here to generate zero-delay clock output. Users can make use of the phase and time delay adjustment in the device to further compensate for the board routing delay. The phase skew adjustment can be modified in the Phase Skew Manager block in PAC-Designer. The time skew can be modified in the output block as shown in Figure 2.

Pin USER0 is used as a LOCK output of the PLL. Pins USER1 and USER2 are used as an I^2C SDA pin and SCL pin respectively. The I^2C interface can be used to dynamically control the output clock frequency, phase and time skew adjustment, and more. Figure 3 shows the User Signal Routing block of the design.

Figure 3. User Signal Routing Block Function



As shown in Figure 1, the negative pin of the SSTL2 output is connected to the feedback negative pin of the PLL while the feedback positive pin is biased to $V_{CCO}/2$. The same biasing circuitry is applied to the reference clock negative pin since this design uses a single-ended oscillator to drive the input reference clock. The reference clock pins and feedback pins of the ispClock5400D device can accommodate any single-ended logic type. AN6080, Using a Low-Cost CMOS Oscillator as a Reference Clock for SERDES Applications provides a more detailed description of how to use a low-cost oscillator to drive the clock pins of the ispClock5400D. Suggestions for handling any unused pins can be found in the ispClock5400D Family Data Sheet.

Implementation

Table 4. Performance and Resource Utilization1

Device Family	I/Os	I^2C Blocks	PLLs
ispClock5400D[1]	9	1	1

1. Resource characteristics are generated using an ispClock5406D or ispClock5410D device with Lattice PAC-Designer 5.2 software. When using this design in a different device, utilization characteristics may vary.

References

- ispClock5400D Family Data Sheet
- AN6080 - Using a Low-Cost CMOS Oscillator as a Reference Clock for SERDES Applications
- JEDEC Standard JESD8C.01
- JEDEC Standard JESD8-5A.01

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
January 2010	01.0	Initial release.