

Introduction

This application note discusses the states of the ProcessorPM™ ispPAC®-POWR605 device's open drain logic outputs (IN_OUT1 to IN_OUT5) during power-up, reset, and JTAG programming, as well as the states of these pins on a device that has not yet been programmed by the user. Suggested methods for interfacing to the enable pin of DC/DC converters and for performing in-system programming are also covered in this application note.

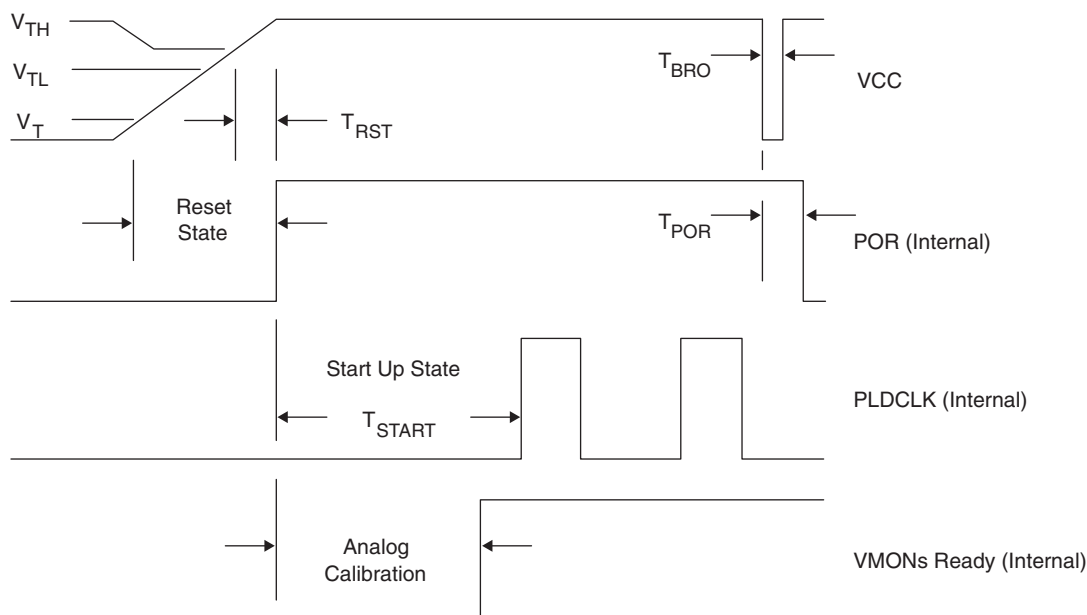
Power-on Reset State

The ProcessorPM contains on-chip power-on reset circuitry to ensure that all parts of the device start up reliably, regardless of VCC ramp rate. As shown in Figure 1, the device enters the power-on reset state when VCC is typically at 0.8V. When VCC is greater than 2.5V, the device will exit the power-on reset state after T_{RST} delay. During power-on reset state, the output pins will go to the states shown in Table 1. After the device exits the power-on reset state, any brownouts that cause the VCC supply to dip below V_{TL} for T_{BRO} will cause the device to re-enter the power-on reset state. An internally generated power-on-reset (POR) signal becomes active during the power-on reset state. The POR signal is used to asynchronously reset or preset the macrocells within the PLD. The designer can specify whether an output is reset or preset by using the PINS window of LogiBuilder in PAC-Designer. By default all the state machine macrocells are reset so the device will start-up in Step 0.

Table 1. Output States During Power-On Reset

Output Type	Power-on Reset State
IN_OUT1 to IN_OUT5	High Impedance

Figure 1. Internal Power-On Reset

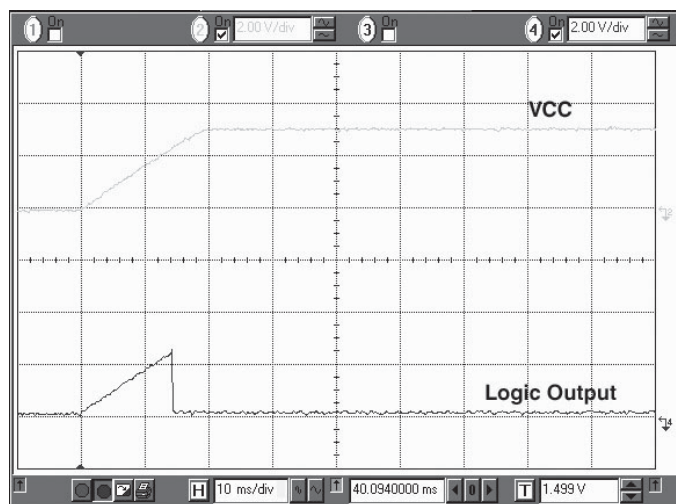


Start-up State

The ProcessorPM exits the power-on reset state and enters the start-up state as the internal POR signal becomes active. The start-up state initializes and enables additional circuits before releasing the PLD-clock. During the start-up state the VMON comparator outputs are Low, the PLD-clock is inactive, and the analog circuits are calibrated. The end of the start-up state is signified with the first rising edge of the PLD-Clock, which is applied to all the programmable registers within the device. The analog circuit calibration is typically completed 4 μ s before the end of the start-up state.

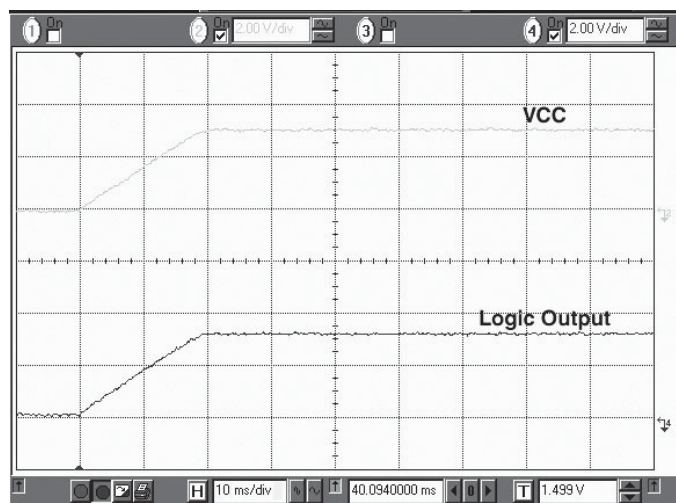
Figures 2-5 illustrate the power-on reset behavior associated with logic outputs IN_OUT1 to IN_OUT5 pins that have been programmed to operate as open drain logic outputs. 2k Ohm pullup resistors to the VCCD pin were used on the logic output pins in all of the plots.

Figure 2. Startup with Slow Supply; Output Resets Low



10 ms/div

Figure 3. Startup with Slow Supply; Output Resets High

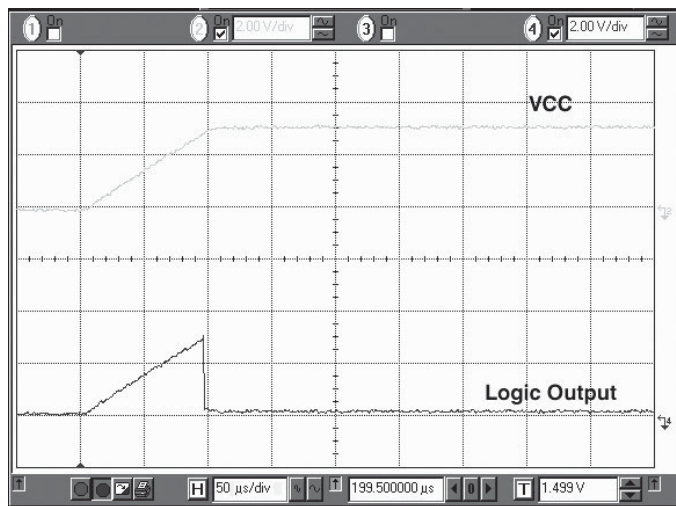


10 ms/div

Figures 2 and 3 show an open drain logic output pin that has been programmed to behave as a registered output. The difference between these two plots is that in Figure 2, the output has been programmed to reset to a low level, whereas in Figure 3, it has been programmed to reset high. The power supply goes from zero to 3.3V in 20 milliseconds. The waveforms in Figures 2 and 3 are typical of VCC supplies that take more than a millisecond to reach 3.3V.

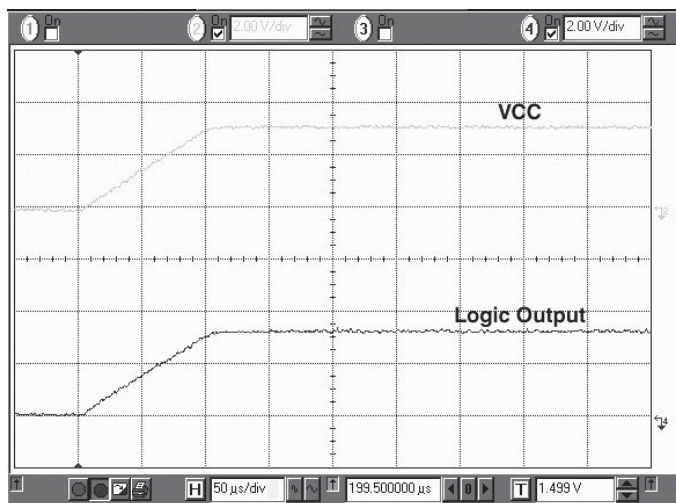
The behavior in both cases is identical until the time that VCC reaches 2.5V. The open drain logic output retains its high impedance state until VCC reaches 2.5V; the voltage observed at the open drain logic output thus follows VCC to 2.5V. When VCC reaches 2.5V, power-on reset ends. From that point on, the logic outputs assume their programmed macrocell reset levels.

Figure 4. Startup with Fast Supply; Output Resets Low



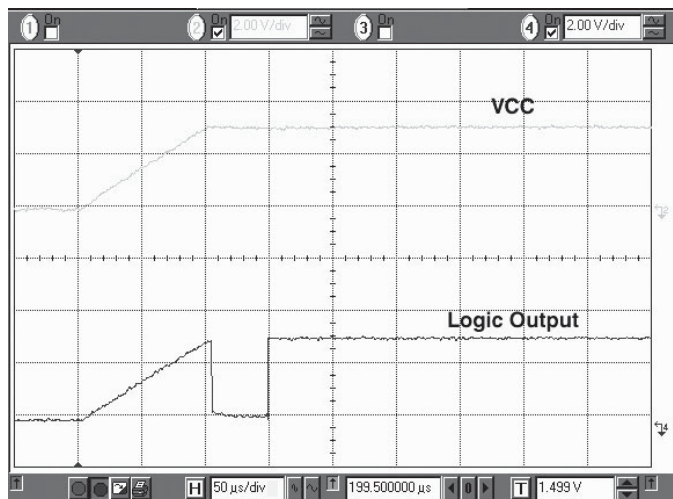
50 μs/div

Figure 5. Startup with Fast Supply; Output Resets High



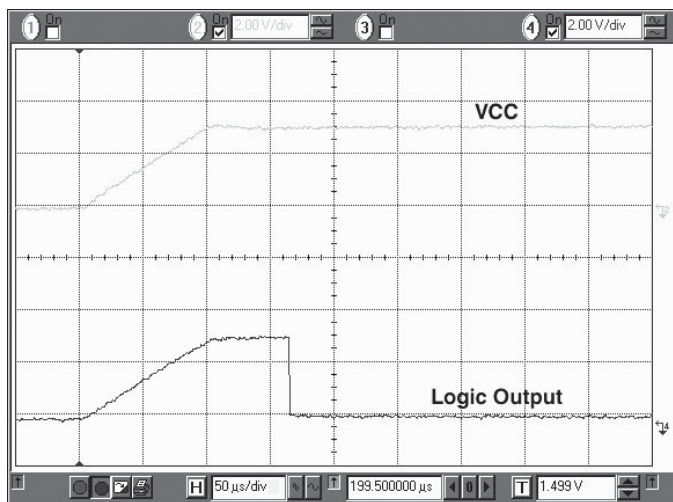
50 μs/div

Figures 4 and 5 show the waveforms observed when the same device and setup that were examined in Figures 2 and 3 are powered from a supply that goes from 0 to 3.3V in 100 microseconds. At this faster power-up rate we begin to see the internal logic delays in the scope plots. The internal reset appears to take effect when VCC reaches 3.3V instead of 2.5V as in the previous plots. This is due to the reset delay that is specified in the data sheet as T_{RST} .

Figure 6. Combinatorial Output that Follows VMON

50 μs/div

VMON comparator outputs will be low, regardless of the voltage at the VMON input pin, while the internal POR is active. Any supervisory logic equations in which a low VMON comparator output indicates a failure condition will have an invalid region in the waveform at startup, as shown in Figure 6. This situation can be avoided by either using registered logic that is reset HIGH or by including a logic OR of an output that is reset HIGH but, set LOW early in the sequence.

Figure 7. Registered Output's Reset High; Set Low in Step 0

50 μs/div

Figure 7 shows the behavior of a registered output during the reset and start-up states. The register is reset HIGH and then set LOW in the very first step of the sequencer. The delay between the end of the VCC ramp and the LOW going transition on the Logic Output results from the T_{START} delay that is specified in the data sheet.

A waveform similar to what is shown in Figure 6 would result from a register that is reset LOW and then set HIGH in the very first step of the sequencer.

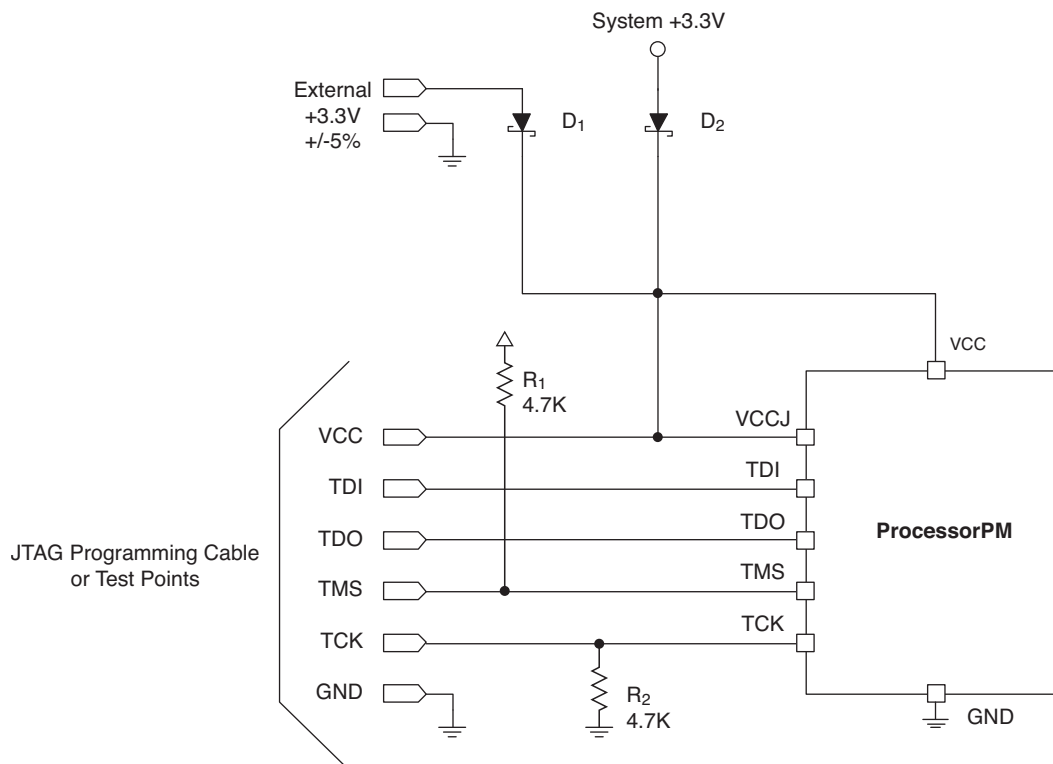
Behavior During JTAG Programming

During JTAG programming, the output pins go to the states defined in Table 2.

Table 2. Output States During JTAG Programming

Output Type	State During JTAG Programming
IN_OUT1 to IN_OUT5	High Impedance

Figure 8. Diode Circuit Provides Power for Programming or Normal Operation



The circuit in Figure 8 (or an equivalent) is recommended to support programming the ProcessorPM without having to power-up the entire system or board. This is because all the outputs are high impedance during programming and are not under control of the sequencer. When 3.3V power is applied to the external connector then only the JTAG programming cable and the ProcessorPM are powered. They receive power from D_1 while D_2 blocks power from the rest of the circuitry during erasure and programming. The 3.3V supply should be $\pm 5\%$, rather than the $\pm 10\%$ specified for JTAG, because of the voltage drop across the Schottky diode. After programming the power is removed from the external connector and then the board or system can be powered up so the ProcessorPM will receive power from D_2 . R_1 and R_2 are recommended to prevent spurious activity of the JTAG interface when a cable is not installed.

Shipped State of New Parts

ProcessorPM devices are programmed at the factory with a sequence known as the “as-shipped” state. The output pins of devices in the as-shipped state will assume the states defined in Table 3 once power-on reset is completed. For additional information about the factory configuration, see RD1056, [Supervisor, WDT and Reset Generation with ProcessorPM](#) reference design.

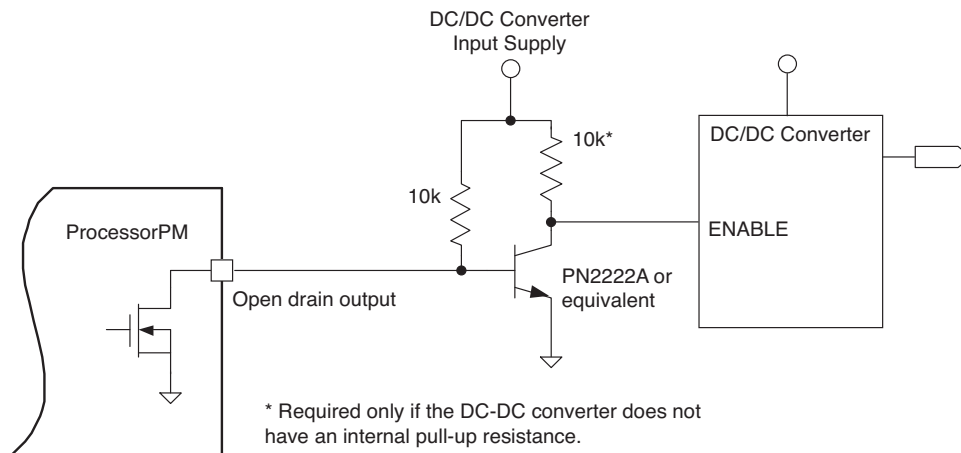
Table 3. Output Functions of a Device As Shipped from Lattice Semiconductor

Output Pin	As-Shipped State
IN_OUT1	Output: Reset Low
IN_OUT2	Output: Reset High
IN_OUT3 to IN_OUT5	Input: High Impedance

Ensuring Reliable Operation at Power-up

Power supply systems using the ProcessorPM should be designed such that a high impedance state on a given logic output disables the supply controlled by that pin. Supplies with negative enable logic – the ones in which pulling the enable pin to ground turns the supply on – can be connected directly to the open drain output pins without any additional components. For supplies with positive enable logic, the circuit in Figure 9 should be used. In both cases, the DC/DC converter data sheet should be checked to see whether its enable input has a built-in pullup resistor or whether an external resistor must be used. Tables 4 and 5 list the values that should be used in the LogiBuilder OUTPUT instructions and the reset levels that should be selected in the “PINS” window for supplies with positive and negative enable logic, respectively. Clicking on the “PINS” tool shown in Figure 10 will open the “PINS” window. Double-clicking on any output will bring up the “Pin Definition” dialog box (also shown in Figure 10) that is used to set the reset levels.

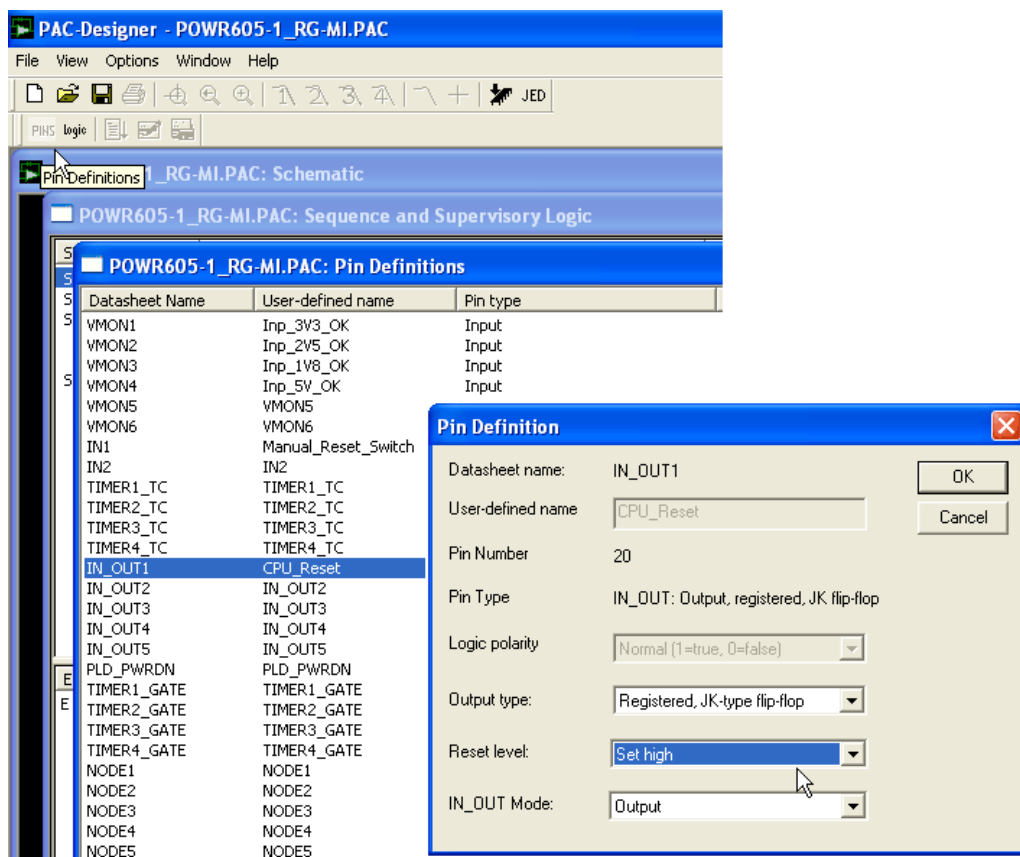
The added benefit of using a bipolar transistor (such as the 2222) is that regardless of the DC-to-DC Input Supply Voltage (12V or more), the ProcessorPM open-drain output will only see 0.7V maximum because, the Emitter-Base junction will bias to that voltage. And when the open-drain output is low, the voltage on the pin is near ground.

Figure 9. Interfacing to Supplies with Positive Enable Logic**Table 4. Controlling Positive Logic Supplies**

Interface Method	POR Level	“PINS” Window Reset Level	LogiBuilder OUTPUT Value to Turn Supply ON	LogiBuilder OUTPUT Value to Turn Supply OFF
Use Inverter Circuit (Figure 9)	HIGH	HIGH	0 (Deassert)	1 (Assert)

Table 5. Controlling Negative Logic Supplies

Interface Method	POR Level	“PINS” Window Reset Level	LogiBuilder OUTPUT Value to Turn Supply ON	LogiBuilder OUTPUT Value to Turn Supply OFF
Connect Directly to Open-Drain Output	HIGH	HIGH	0 (Deassert)	1 (Assert)

Figure 10. Setting Reset Level in the PINS Window

Coming Out of Power-Down Mode

The ProcessorPM is capable of being powered down to conserve battery power in portable applications. The power-down mode is enabled and configured from PAC-Designer and can be activated either with internal logic or by the status of the pin IN1_PWRDN. To power-up the device, the pin IN1_PWRDN has to have a logic HIGH applied to it. In power-down mode, all the outputs are High impedance, to avoid any leakage to ground, and the device itself draws less than 10 μ A when the VCCJ pin is left floating. Figure 11 shows the timing relationship from the IN1_PWRDN pin going High to an output going Low as the ProcessorPM comes out of the power-down mode. The output in this example is reset High and then set Low in the very first step of the sequencer. The delay from the rising edge of IN1_PWRDN to the falling edge of the output is the T_{START} delay shown in Figure 1.

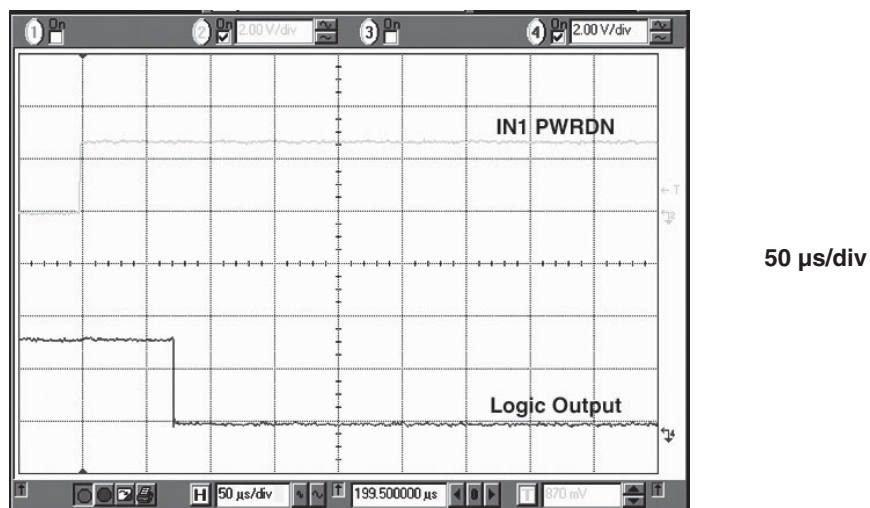
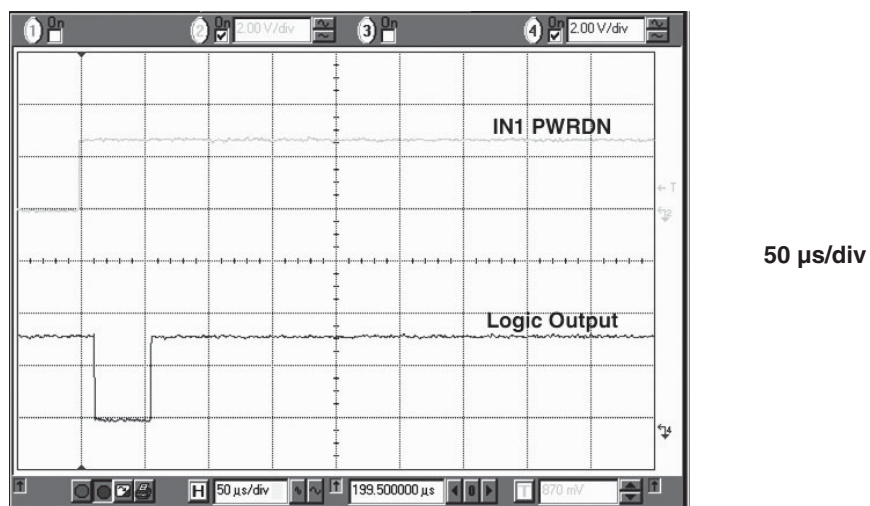
Figure 11. Coming Out of Power-Down Mode; Reset High; Set Low in Step 0

Figure 12 shows the behavior of an output configured to combinatorially (un-registered) follow a VMON comparator output. In this example, the input pin has a bias on it and the output should be true. Figure 12 shows T_{RST} delay from the rising edge of IN1_PWRDN to the falling edge of the output while the analog circuits are starting up.

Figure 12. Coming out of Power-Down Mode; Output Follows VMON

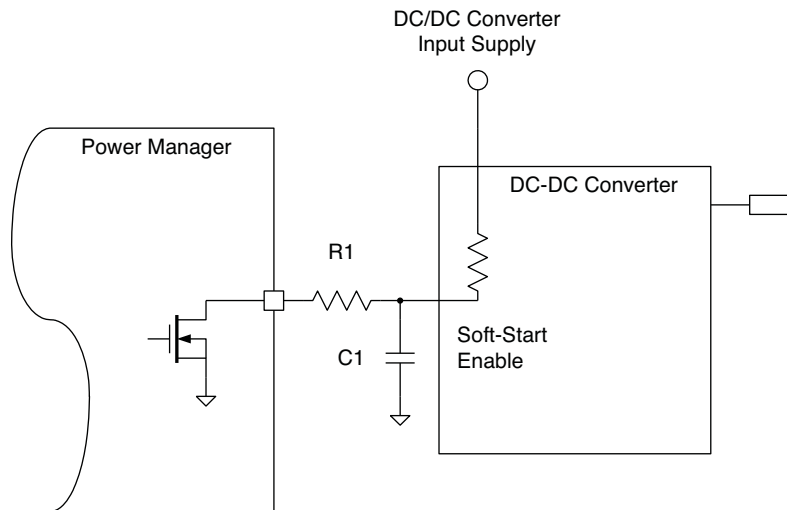
Capacitive Loading on Outputs

In certain applications, the outputs of the Power Manager device are used to enable the soft-start feature of a DC-DC converter. This presents a capacitive load to the outputs of the Power Manager. During the power-up cycle of the Power Manager, the open-drain outputs will transition from active low to high-z. Likewise, the HVOUT pins will transition from active low to discharge (or high-z depending on the configuration) during the power-up cycle. If the soft-start capacitors have any charge stored during this time, excessive currents will flow through the open-drain outputs to ground. These currents can result in an unreliable start-up of the Power Manager. Furthermore, during normal operation setting an output low can also result in a discharge current that exceeds the maximum current limits in the data sheet.

To ensure reliable Power Manager start-up and to limit the current surge it is required to add a series resistor when a capacitive load is connected to an output as shown in Figure 13. The value of R1 should be such that when C1 is discharged by the open-drain output the current is less than the $I_{SINKMAXTOTAL}$ limit in the data sheet. The $I_{SINKMAXTO-}$

I_{SINK_TAL} is for any single output and is found in the Absolute Maximum Ratings Table of the data sheet. If multiple outputs have capacitive loads the I_{SINK_TOTAL} Max should also be considered in setting a value for the series resistors. The I_{SINK_TOTAL} number is found in the Digital Specifications table of the data sheet and applies to all outputs combined.

Figure 13. Limiting Capacitive Load Currents to Less than $I_{SINK_MAX_TOTAL}$



Summary

The startup characteristics of the open drain logic outputs (IN_OUT1 to IN_OUT5) pins as a function of the power-on reset condition have been described. The behavior of these outputs has also been defined during JTAG programming. The programmed state in which new devices are shipped from the factory (the “as-shipped” state) has been described.

To ensure reliable startup of power supplies, the ProcessorPM’s logic outputs should be set up so that a logic low activates the supplies. Supplies that use positive enable logic require a simple one-transistor inverter to interface to the ProcessorPM’s open drain logic outputs.

The ProcessorPM has similar behavior in both a cold reset (powering up from a cold supply) or a warm reset (powering up from the power-down mode). In either case, there is a short delay (T_{RST}) before the internal POR is released and a slightly longer delay (T_{START}) before the first internal PLD-Clock edge is available for either the sequencer or any registered outputs.

The strategy to perform in-system programming by applying power only to the ProcessorPM is recommended.

When outputs are driving a capacitive load a series resistor is required to insure the discharge current is below the current limits in the data sheet.

Related Literature

- [ProcessorPM-POWR605 Data Sheet](#)
- RD1056, [Supervisor, WDT and Reset Generation with ProcessorPM](#)

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: isppacs@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
December 2009	01.0	Initial release.
April 2011	01.1	Updated to address capacitive loading on the outputs.