LatticeECP2M Broadcom XAUI 10 Gbps Physical Layer Interoperability Over CX-4

November 2009 Technical Note TN1188

Introduction

This technical note describes a physical layer 10 Gigabit Ethernet XAUI (10 Gbps) interoperability test between a LatticeECP2M™ device and the Broadcom® BCM56800 network switch. The test was limited to the physical layer (up to XGMII) of the 10 Gigabit Ethernet protocol stack.

Specifically, the document discusses the following topics:

- Overview of LatticeECP2M devices and Broadcom BCM56800 network switch
- Physical layer interoperability setup and results

Two significant aspects of the interoperability test need to be highlighted:

- The BCM56800 uses a CX-4 port, whereas the LatticeECP2M SERDES Evaluation Board provides an SMA connector. So a CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards. The SMA side of the CX-4 to SMA conversion board has four differential Tx/Rx channels (10 Gbps bandwidth total). All four SMA channels (Quad 360) were connected to the LatticeECP2M side.
- The physical layer interoperability ran at a 10 Gbps data rate (12.5 Gbps aggregated rate).

XAUI Interoperability

XAUI is a high-speed interconnect that offers reduced pin count and the ability to drive up to 20” of PCB trace on standard FR-4 material. In order to connect a 10-Gigabit Ethernet MAC to an off-chip PHY device, an XGMII interface is used. The XGMII is a low-speed parallel interface for short range (approximately 2”) interconnects.

XAUI interoperability is based on the 10-Gigabit Ethernet standard (IEEE Standard 802.3ae-2002). Two XAUI link partners can be directly plugged into a XAUI backplane. Both boards are capable of generating and checking packets.

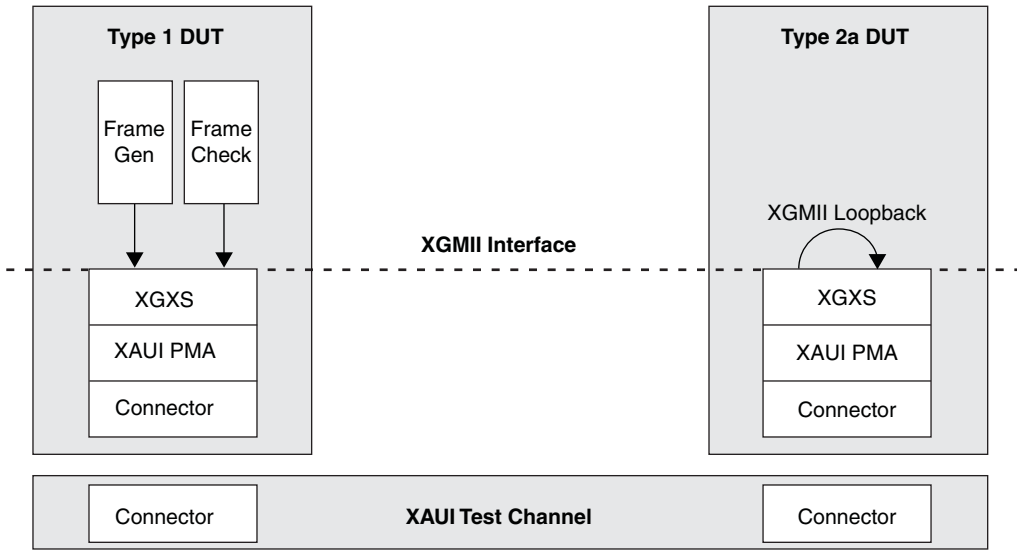
The board that sources packets is capable of keeping a detailed count of the number of packets transmitted while the sink board is capable of keeping detailed statistics on the number of packets received and errors associated with the packets. The XAUI backplane is also called the XAUI test channel. A typical test setup is shown in Figure 1.

Each reference station must be a line card that is directly plugged into the XAUI test channel. Both DUTs are required to have their own clock domain. Synchronous clocking (distributing a single clock to the two DUTs) is not allowed. Local management indicators on the DUT (reference stations) that provide information on link level errors such as CRC errors are also needed. A DUT is called a Type #1 device if it is capable of transmitting and checking packets.

A DUT is called a Type #2a device if it receives packets and does a Rx to Tx loopback through XGMII and sends the packets back to the transmitting station, which is a Type #1 device. The Type #1 device then checks the received packets for errors. Figure 1 shows a setup where one DUT is of Type #1 and the other is of Type #2a.

The LatticeECP2M and BCM56800 interoperability exercises the whole physical layer, including XGMII.

Figure 1. Typical XAUI Interoperability Test Setup



LatticeECP2M Overview

LatticeECP2M Features

The LatticeECP2M family is the industry's only true low-cost FPGA family with built-in SERDES. This family of devices includes features to meet the needs of today's communication network systems.

The LatticeECP2M family also feature up to 16 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The PCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

LatticeECP2M in XAUI Mode

The LatticeECP2M XAUI IP was used for the interoperability exercise described in this document. The LatticeECP2M SERDES/PCS in XAUI mode, along with the Lattice XAUI IP, provide full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard.

Transmit Path Functionality (From LatticeECP2M Device to Line)

- Transmit State Machine which performs translation of XGMII idles to proper ||A||, ||K||, ||R|| characters according to the IEEE 802.3ae-2002 specification
- 8b10b encoding

Receive Path Functionality (From Line to LatticeECP2M Device)

- Word alignment based on IEEE 802.3-2002 defined alignment characters
- 8b10b decoding
- Link State Machine functions incorporating operations defined in PCS Synchronization State Diagram of the IEEE 802.3ae-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine compliant to the IEEE 802ae.3-2002 specification

Broadcom BCM56800 Overview

BCM56800 Features

The BCM56800 network switch is a high-density, 10 GbE switching chip solution with 20 ports. Each of these flexible ports supports 10 GbE or 1 GbE. Additionally, the BCM56800 integrates all the SERDES required to interface to applicable copper and fiber physical interfaces. The integrated SERDES functionality includes 10-Gbps XAUI interfaces and 1-Gbps SGMII PHY interfaces. The integrated SERDES complies with the CX-4 standard and PICMG3.1 standard, which ensures interoperability with Ethernet line cards in an Advanced TCA chassis.

BCM56800 10 GbE Ports

The BCM56800 has 20 10-GbE/1-GbE ports. The BCM56800 is based on the StrataXGS® field-proven, robust architecture. It has integrated high-performance SERDES: integrated XAUI SERDES for all 20 10-GbE ports, and it uses a single SERDES lane per port at GbE speeds. The device supports 200-Gbps switching capacity at line rate.

Test Equipment

Listed below is the equipment used in the interoperability tests.

Broadcom BCM56800 Network Switch

Figure 2 shows the BCM56800 network switch.

Figure 2. Broadcom BCM56800 Network Switch

One can configure the Broadcom ports by connecting its serial port to a PC and starting a HyperTerminal session. Figure 2 shows a serial cable connected to the serial port at the back of the BCM56800.

Figure 2 also shows a CX-4 connector inserted into one 10 GbE port available on the front right side of the BCM56800.

This port, referred to as xe0/hg0, was selected for the interoperation with the LatticeECP2M device. It was configured in XAUI mode.

Agilent Technologies 81130A Pulse/Data Generator

The Agilent Technologies 81130A pulse/data generator was used to supply an external 156.25 MHz reference clock source to the LatticeECP2M SERDES/PCS.

For more information this module, please refer to the Agilent Technologies website at www.agilent.com.

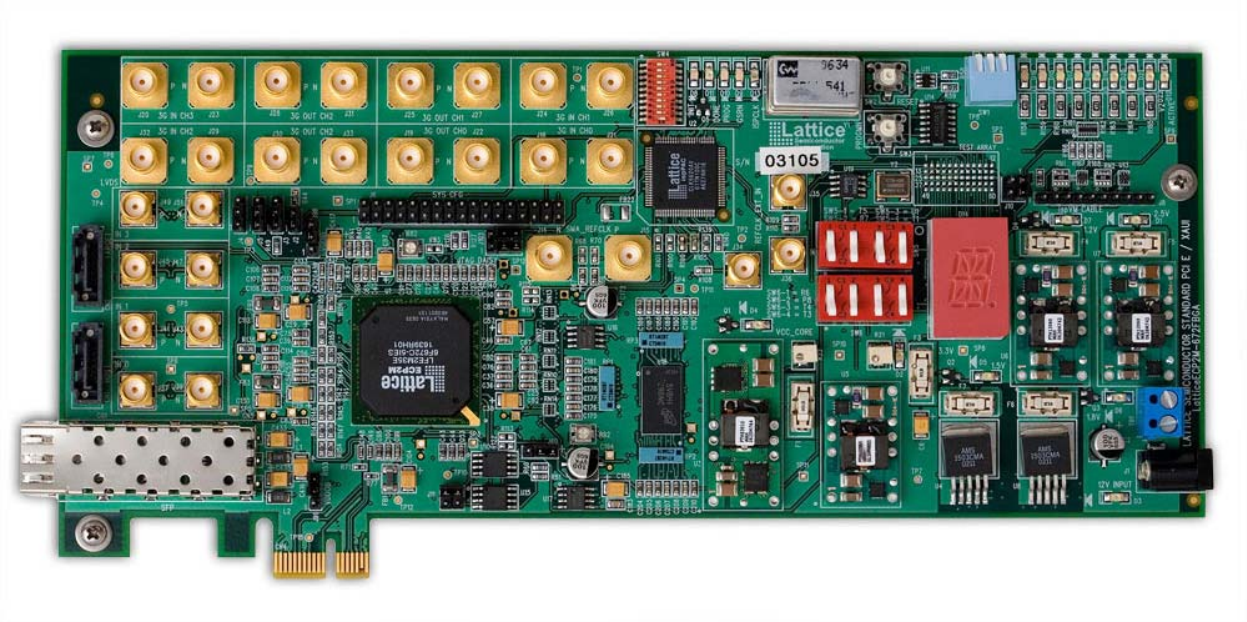
LatticeECP2M SERDES Evaluation Board

The LatticeECP2M SERDES Evaluation Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeECP2M SERDES and FPGA, or aid in the development of custom designs. The LatticeECP2M SERDES Evaluation Board features:

- LFE2M50E-6F672C FPGA
- SMA connectors for SERDES I/O, LVDS evaluation, and external clock I/O
- x1 PCI Express edge connector *(Note: Only available with LatticeECP2M-50 or larger FPGA installed)*
- On-board DDR2 memory
- SFP transceiver cage and associated interface *(Note: Only available with LatticeECP2M-50 or larger FPGA installed)*
- SATA-like connections to SERDES channels *(Note: Only available with LatticeECP2M-50 or larger FPGA installed)*
- On-board Flash configuration memory
- Various LEDs, switches, connectors, I/O headers, high-speed layout structures, and on-board power control

Figure 3 shows the LatticeECP2M SERDES Evaluation Board.

Figure 3. LatticeECP2M SERDES Evaluation Board



ispVM™ System Software

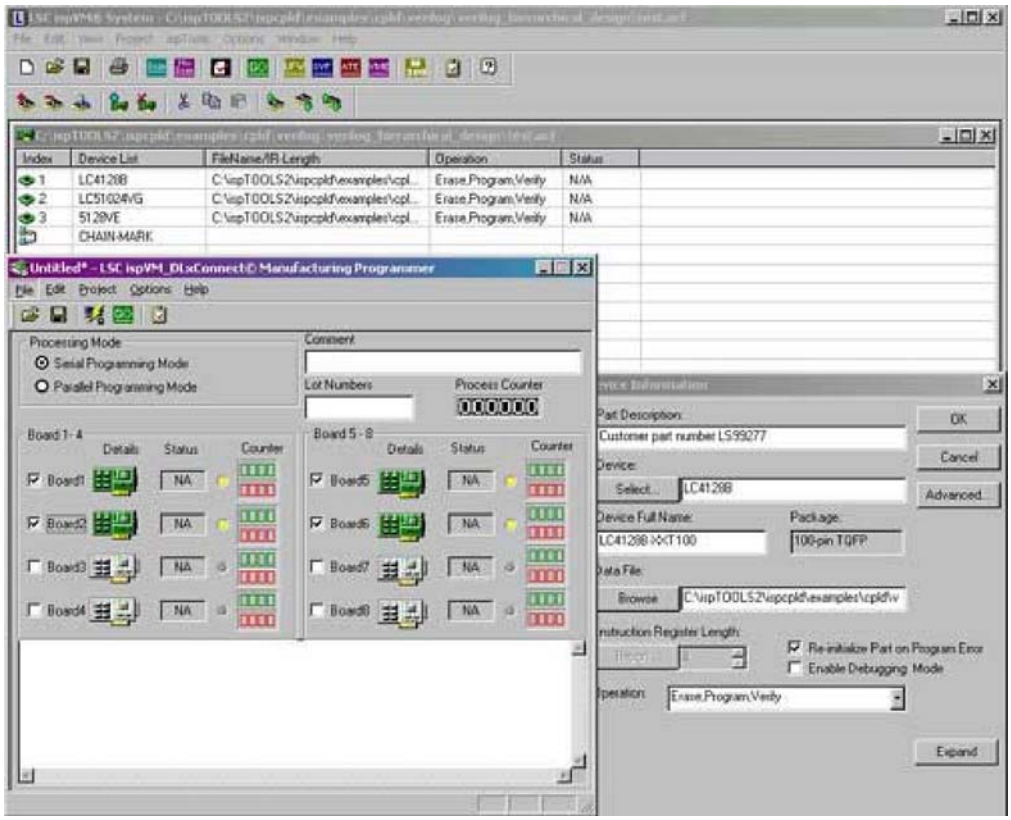
The ispVM System is included with Lattice's ispLEVER® software, and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP devices using JEDEC and bitstream files generated by Lattice, and other, design tools. This complete device programming tool allows the user to quickly and easily download designs through an

ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

ispVM System software is used in this interoperability test to download the LatticeECP2M bitstream, which configures the device in 10 Gigabit Ethernet mode (XAUI).

Figure 4 is a screen shot of the ispVM System software.

Figure 4. ispVM System Software GUI



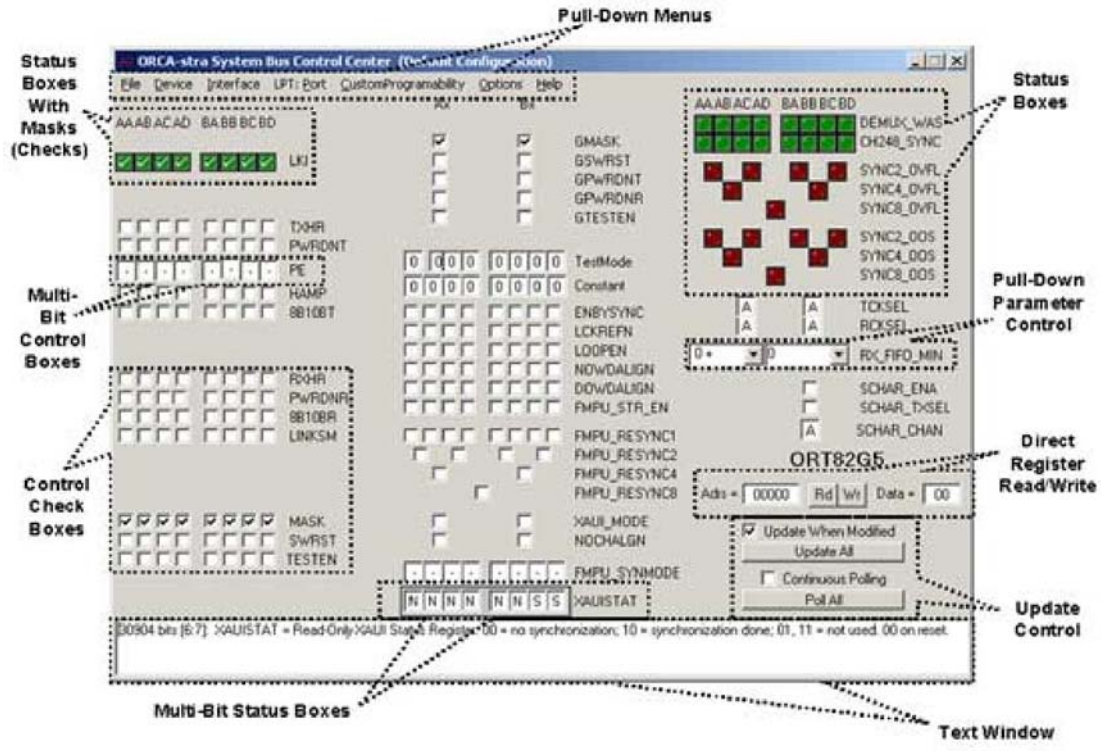
ORCAstra Software

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to their board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the LatticeECP2M.

Figure 5 is a screen shot of the ORCAstra software.

Figure 5. ORCAstra Software GUI



Interoperability Testing

This section provides details on the 10 GbE (10 Gbps) XAUI Physical Layer interoperability between a LatticeECP2M device and the Broadcom BCM56800 network switch. This interoperability tests the correct processing of XAUI (10 Gbps) data from the BCM56800 network switch to the LatticeECP2M and then back in the other direction. Particularly, the test verifies the ability to transfer packets across the system in an asynchronous way.

Test Setup

Figure 6 shows the LatticeECP2M and Broadcom board connections. Figure 7 is a block diagram of the test setup.

The set-up includes:

- The Broadcom BCM56800 network switch
- The LatticeECP2M SERDES Evaluation Board. In 10 GbE, the Agilent Technologies 811130A Data/Pulse Generator provides an external 156.25 MHz reference clock to the LatticeECP2M SERDES/PCS. The clock is multiplied internally by 20 to achieve a 12.5 Gbps aggregated rate (10 Gbps data rate). Note that an on-board 156.25 MHz differential oscillator can also be used to provide a reference clock to the LatticeECP2M SERDES/PCS.
- A PC for software control/monitoring
- A CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards (see Figure 6). The SMA side of the CX-4 to SMA conversion board has four differential Tx/Rx channels, or 16 SMA connectors for a total bandwidth of 10 Gbps (12.5 Gbps aggregated rate). All four differential Tx/Rx channels were connected to the LatticeECP2M side (as shown in Figure 6).
- Cables
  - 16 SMA for LatticeECP2M SERDES channels 0 through 4
  - 2 SMA for Agilent Technologies clock generator
  - CX-4 for BCM56800 port xe0

– ispVM JTAG cable for downloading LatticeECP2M bitstream and ORCAstra GUI access
– Serial cable for BCM56800 HyperTerminal access

Figure 6. Board Connections

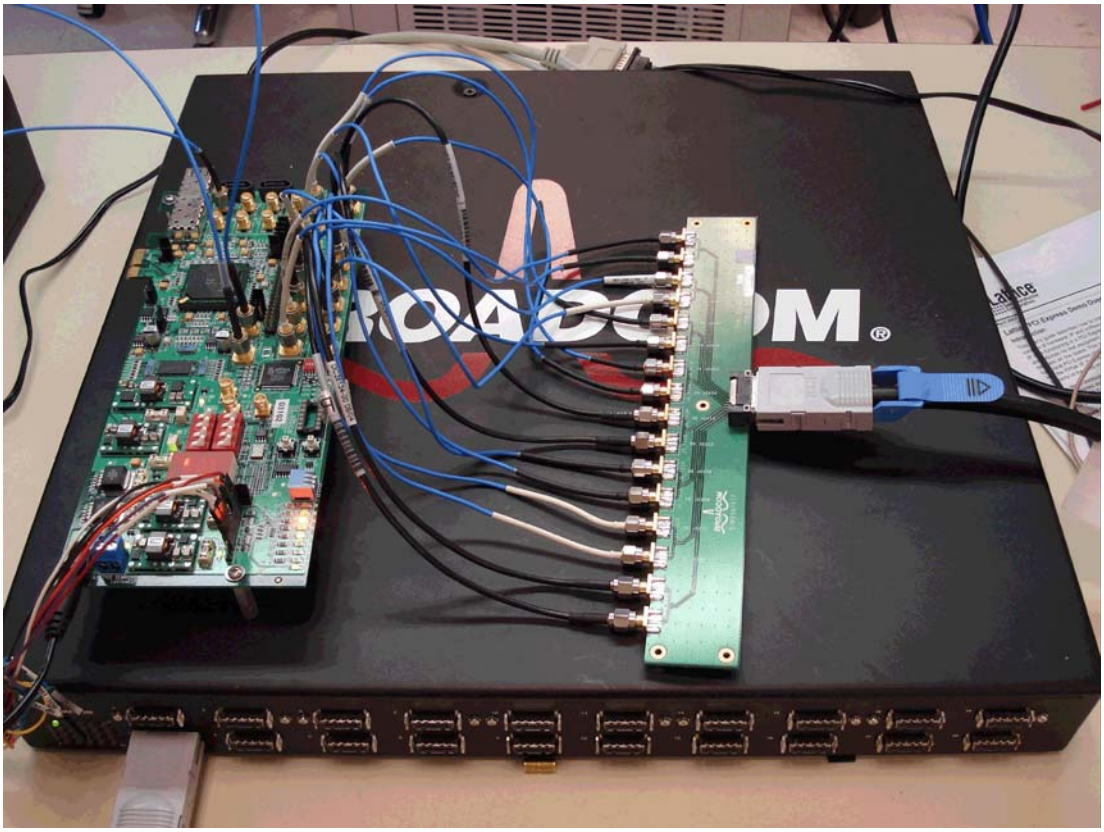
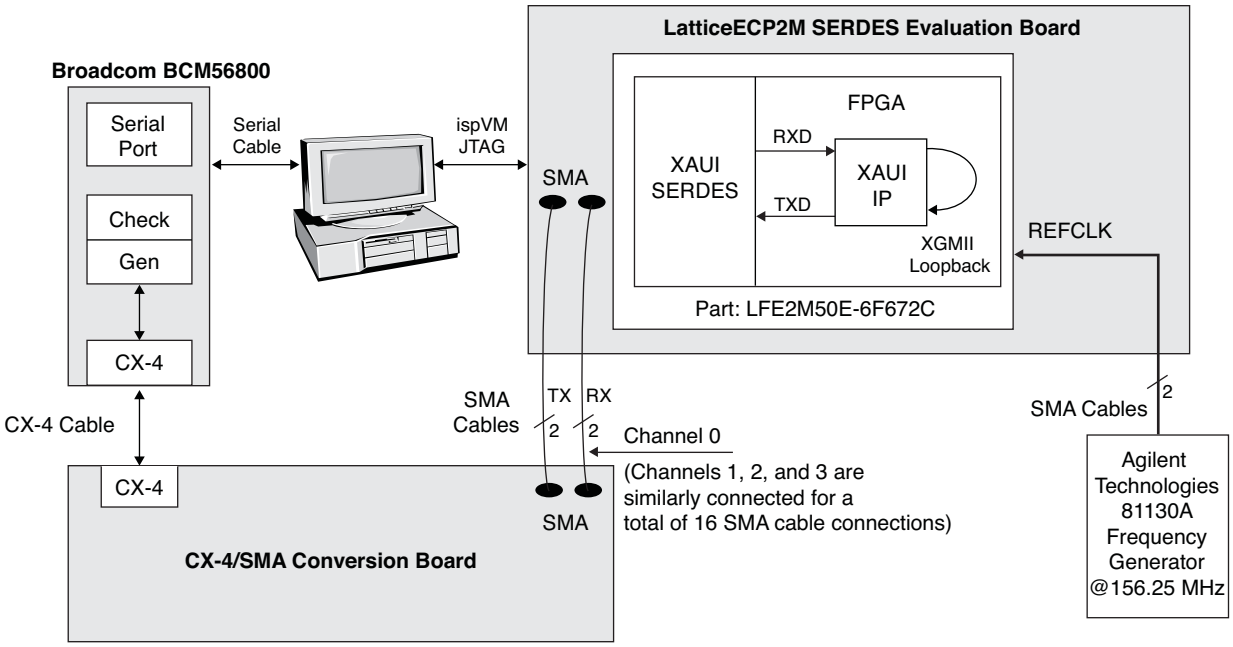


Figure 7. Test Setup Block Diagram



Test Description

This section describes how each interoperability partner is set up for 10 GbE physical layer interoperability.

BCM56800

The BCM56800 switch generates and checks full protocol compliant 10 GbE packets. The BCM56800 is configured in either XAUI mode.

Figure 8 illustrates the sequence of events performed in a HyperTerminal from startup to configure Port 0 (xe0) of BCM56800 in XAUI mode.

Figure 8. Configuring BCM56800 Port 0 in XAUI

```
BCM.0> rc
rc: unit 0 device BCM56800_A0
BCM.0> port xe0 speed=10000 AN=OFF
BCM.0> sleep 10
Sleeping for 10 seconds
BCM.0> ps
       ena/  speed/  link   auto   STP                          lrn     inter     max    loop
port  link  duplex   scan  neg?   state      pause    discrd  ops    face     frame  back
 xe0  up    10G FD  SW    No     Forward             None     FA   XGMII 16360
 xe1  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe2  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe3  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe4  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe5  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe6  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe7  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe8  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
 xe9  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe10  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe11  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe12  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe13  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe14  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe15  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe16  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe17  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe18  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
xe19  down  -       SW    Yes    Forward  TX RX      None     FA   XGMII 16360
BCM.0> clear counters
BCM.0> show counters
BCM.0> time
2771.638545 sec
BCM.0> tx 10000000 pbm=xe0 file=bc_DA_1022
BCM.0> time
4822.619023 sec
BCM.0> sleep 1
Sleeping for 1 second
BCM.0> show counters
RUC.xe0        :          10,000,000        +10,000,000
RDBGC0.xe0     :           9,999,771         +9,999,771
ITPKT.xe0      :          10,000,000        +10,000,000
IT1518.xe0     :          10,000,000        +10,000,000
ITBYT.xe0      :      10,440,000,000    +10,440,000,000
IR1518.xe0     :          10,000,000        +10,000,000
IRPKT.xe0      :          10,000,000        +10,000,000
IRBYT.xe0      :      10,440,000,000    +10,440,000,000
IRJUNK.xe0     :                   1               +1
BCM.0>
```

LatticeECP2M SERDES Evaluation Board

The Agilent Technologies 811130A sources the LatticeECP2M PCS reference clock for XAUI. The reference clock is multiplied internally by 20 to achieve a 10 Gbps data rate (12.5 Gbps aggregated rate).

In the Rx direction, the LatticeECP2M SERDES recovers the packets from the BCM56800 device and the XAUI IP converts them into XGMII format.

The XGMII loopback logic in the FPGA portion loops the XGMII data back into the Tx direction. The LatticeECP2M device then transmits the packets back to the BCM56800 device.

XAUI Results

As shown in Figure 8, port 0 (xe0) of BCM56800 was configured for XAUI.

The HyperTerminal “tx” command generated 10,000,000 packets from the BCM56800 to the LatticeECP2M SERDES Evaluation Board.

The “show counter” command was then used to monitor the status of the BCM56800 Tx and Rx packet (GTPKT.xe0 & GRPKT.xe0) and byte (GTBYT.xe0 & GRBYT.xe0) counters. Figure 8 does not show any error counters. This is an indication that the error counters have remained at a zero value during the test. Additionally, the Lattice ORCAstra software GUI (shown in Figure 5) was monitored for proper 10 GbE link state machine synchronization.

The results show that all the Ethernet packets were successfully transmitted to the LatticeECP2M and recovered at the BCM56800 error-free.

Summary

In conclusion, the LatticeECP2M FPGA family offers users XAUI physical layer support and is fully interoperable with the Broadcom BCM56800 network switch in XAUI (10 Gbps) mode.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2009	01.0	Initial release.