



LatticeECP3 CPRI Demo Design

User's Guide

Introduction

This document provides technical information and instructions for using the LatticeECP3™ CPRI Demo Design. The demo has been designed to demonstrate the performance of the LatticeECP3 PCS with the CPRI IP core at 1.228/2.457/3.072 Gbps. Note that the IP core itself does support all four rates (614 Mbps, 1.228/2.457/3.072 Gbps). The document provides a circuit description as well as instructions for running the demo on the LatticeECP3 Serial Protocol Board.

In addition to this user's guide the CPRI Demo comes with the following:

- Verilog source code for the FPGA design.
- ispLEVER® Project Navigator implementation project file and Aldec® Active-HDL® simulation scripts
- Bitstream (in *.bit format)
- ORCAstra plug-in GUI

Hardware requirements for the CPRI demo design:

- LatticeECP3 Serial Protocol Board (revision C or later) with LatticeECP3-95, 1156-pin device
- 12V DC power supply
- PC with ORCAstra (PC not provided)
- SMA cables for loopback

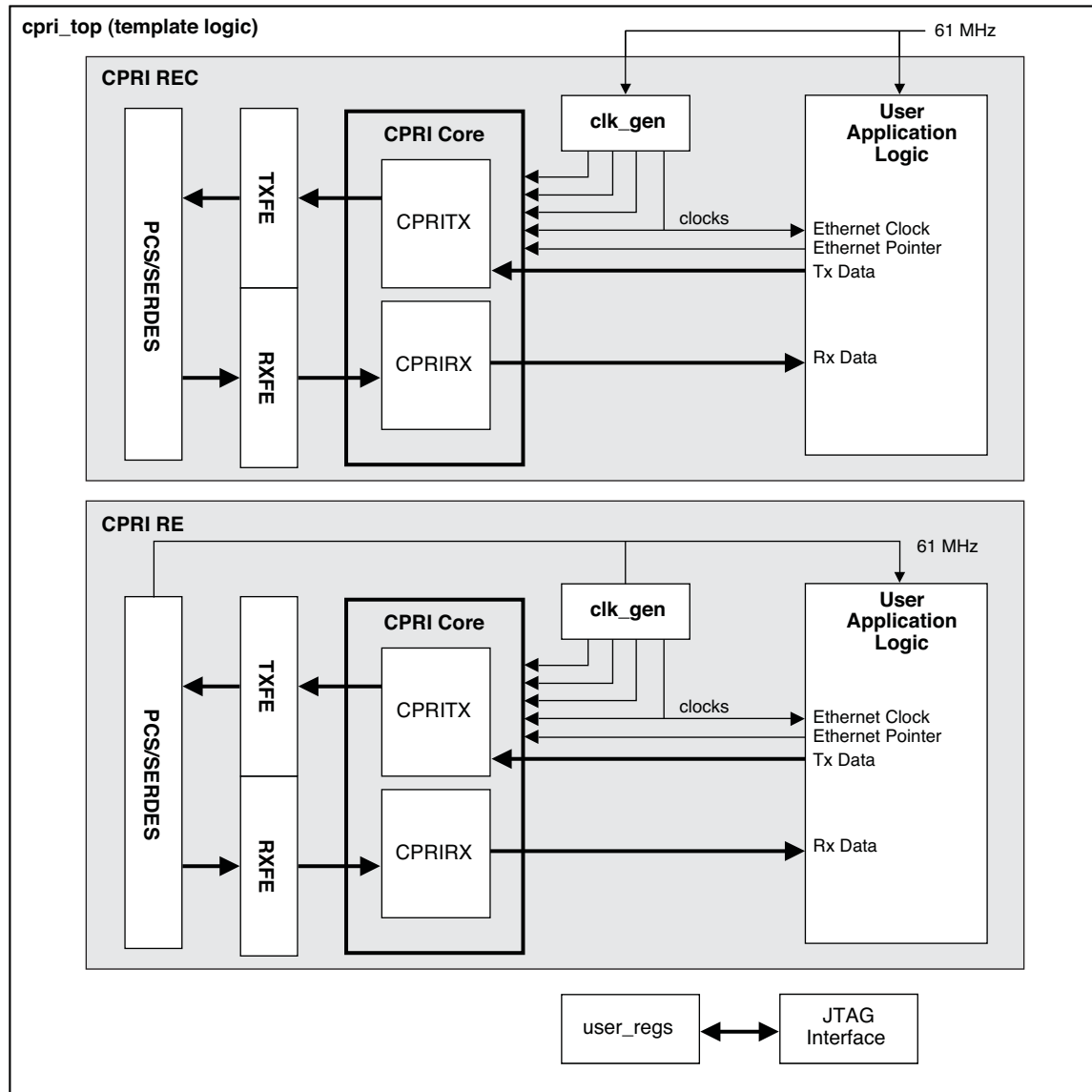
Software application and driver requirements:

- ispVM™ System software (version 17.4 or later) for FPGA bitstream download
- ispVM JTAG to USB download cable
- ispLEVER 7.2 SP2 or later
- ORCAstra software for user control interface (included with ispLEVER 7.2 SP2 or later)

CPRI Demo Design Overview

A block diagram of the CPRI core in the FPGA I/O demo design is provided in Figure 1.

Figure 1. CPRI Demo Design

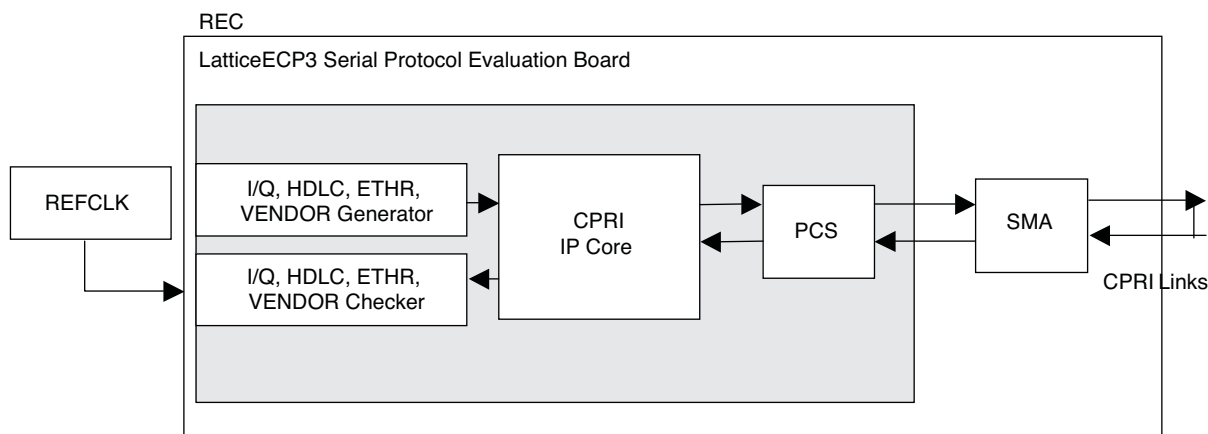


For this demo design, the PCS Quad B location on the chip is used. It has been generated in CPRI mode and supports rates of 1.228/2.457/3.072 Gbps.

The CPRI Demo Design is a single-channel CPRI core with data generator/checker. The PCS serializes the data in the transmit direction, and de-serializes it in the receive direction. For the Radio Equipment Control (REC) standalone loopback demo, the encoded serial data stream is looped back externally via I/O buffer serial loopback or via cables using the on-board SMA connectors. In the CPRI REC standalone loopback demo, only one evaluation board is needed to run the loopback test.

The CPRI Demo design requires a reference clock. In the REC demo, the default reference clock is the on-board 122.88 MHz oscillator.

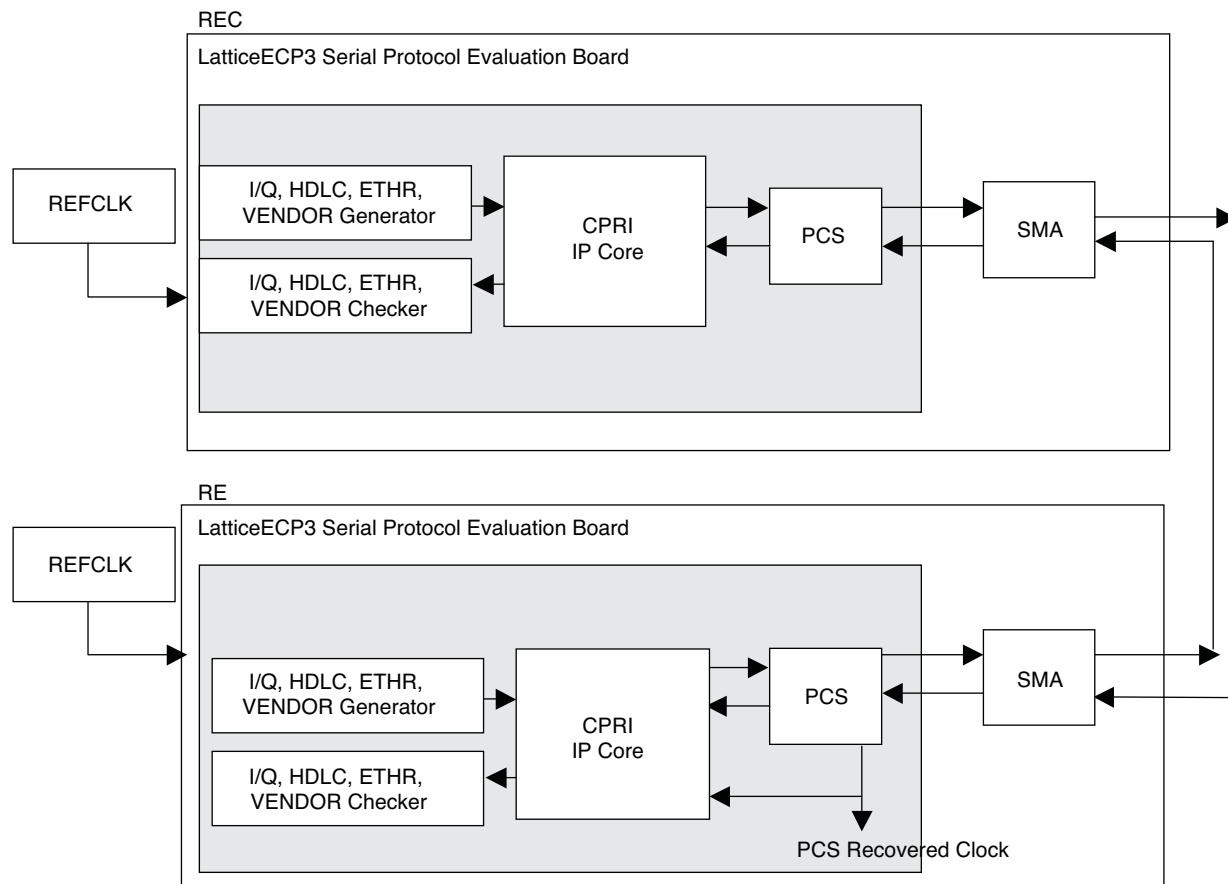
Figure 2. CPRI REC Standalone Loopback Demo (One Evaluation Board)



For the REC-RE demo, two LatticeECP3 Serial Protocol Boards are required. On the REC side, the tx side serial data stream is generated in the FPGA and run from the local system clock. The tx data is connected through SMA cables to the Radio Equipment (RE) Rx side on the second LatticeECP3 Serial Protocol Board. The RE receives the data from the REC and the recovered clock is then used to drive the RE Tx data traffic generation circuit completing the “loop timing”.

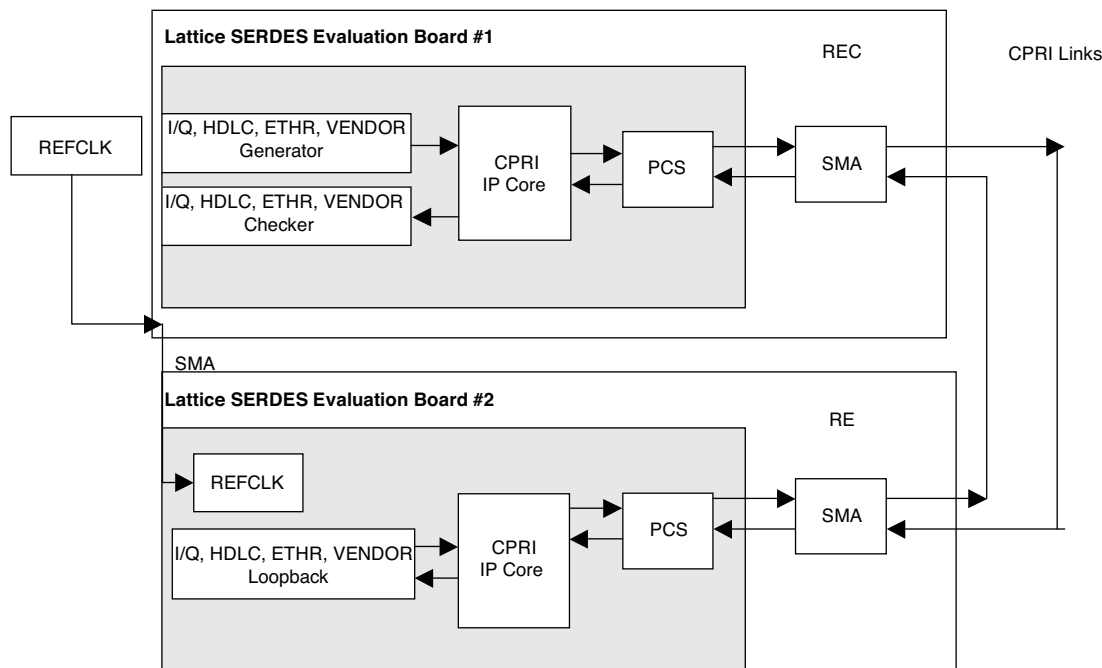
The CPRI demo design requires a reference clock. In the REC and the RE demos, the default reference clock is the on-board 122.88 MHz oscillator. Users can regenerate new bitstreams if they want to use an external reference clock through the SMA ports.

Figure 3. CPRI REC-RE Demo (Two Evaluation Boards, Loop Timing, Clock Only)



The second part of the REC-RE demo includes the data loopback in synchronous mode. On the REC side, the TX SERDES output port sends out the CPRI serial datastream generated in the FPGA and is run based on the local system clock. The REC device on evaluation board #1 uses the 122.88 MHz oscillator on board as the default system reference clock. The RE device on evaluation board #2 uses the 122.88 MHz clock as system reference clock from evaluation board #1 through external SMA ports. The TX data port is connected to the RE SERDES RX side on the second Serial Protocol Board through SMA cables. The RE receives the data from the REC and loops back the data inside of the FPGA and then to the SERDES TX port output of the RE device. Note that the RE FPGA circuit does not generate test traffic in this mode. Thus, the error insertion or test pattern controls are valid only on the REC side.

Figure 4. CPRI REC-RE Demo (Two Evaluation Boards, Synchronous, Data Loopback)



LatticeECP3 CPRI PCS

PCS Quad B is clocked by its designated FPGA TX/RX reference clock source. The reference clock's frequency is 122.88 MHz and is provided by the on-board Y5 differential oscillator (current default "AB28" location for sysclk_p in LPF file) or SMA differential inputs J38 (P) and J39 (N) (by changing the LOCATE preference on sysclk_p to "U28" in the LPF file). Internal to the PCS, the reference clock is multiplied by a factor to generate the 1.228/2.457/3.072 Gbps per channel data rate.

CPRI IP

The major functional blocks in the example are the CPRI core, the PCS/SERDES block, and the user application logic. The CPRI IP core consists of two major functional blocks, the transmitter (CPRITX) and the receiver (CPRIRX). One side of each of these blocks interfaces to the PCS/SERDES module. The other side interfaces to the user logic that implements the data link and higher layers of the CPRI protocol.

The CPRI core configuration implements all of the capabilities required to support the physical layer of the CPRI specification, except specific requirements related to link delay accuracy. The "low latency" core configuration includes a modified SERDES/PCS interface that supports the ability to manage the variability in the absolute latency for data transmission through the core to meet the stringent CPRI link delay accuracy requirements. The CPRI IP supports four different bit rates: 614.4/1228/2457/3072 Mbps. The current demo design supports the popular 1228/2457/3072 Mbps in order to simplify the clocking structure and timing requirements of the FPGA circuit.

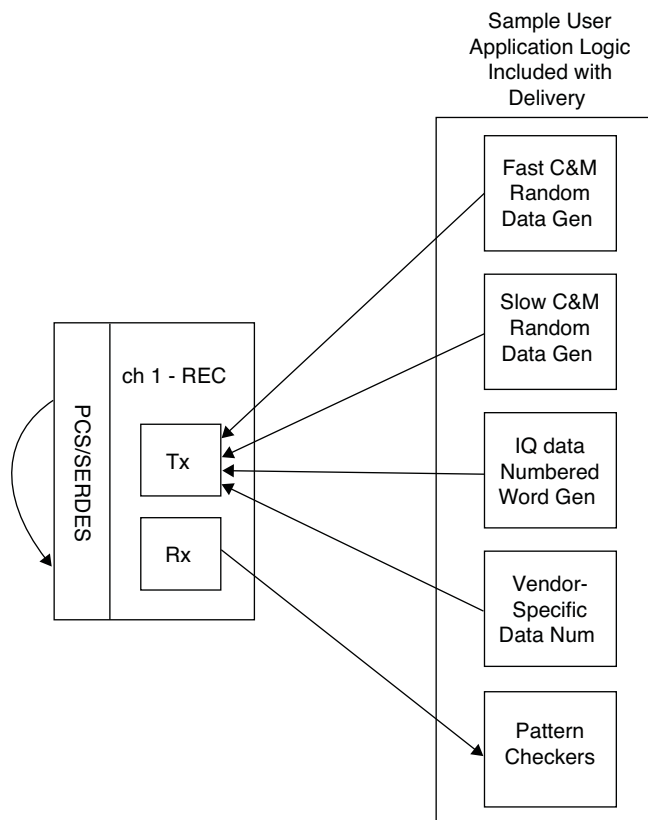
The CPRI IP core interleaves user IQ (in-phase and quadrature) data with control and management (C&M) data into the frame and hyperframe formats specified by the CPRI specification.

For more information on the CPRI PCS IP, please refer to IPUG56, [CPRI IP Core User's Guide](#).

User's Test Bench Logic

The demo design includes a user's testbench that connects the top-level template logic as a REC or RE interface. Test data is sent from the transmitter to the receiver. This circuitry, implemented in the FPGA fabric, consists of the clocking structure, pseudo-random number generators for the fast and slow C&M channels, as well as circuits which insert numbered words into the user IQ data and the vendor-specific channels.

Figure 5. CPRI Demo Testbench Logic



Testbench Data Generator/Checker

The CPRI demo testbench includes the Generator/Checker block in the demo design:

- Fast C&M data generator and checker
- Slow C&M data generator and checker
- IQ C&M data generator and checker
- Vendor-specific data generator and checker
- Each data generator and checker can be set as constant data
- Control/status interface to user registers
- Error counter connected to user registers for monitoring

The ORCAstra block controls all user registers as well as the LatticeECP3 PCS Quad via the SCI interface. ORCAstra is in turn controlled via the JTAG interface.

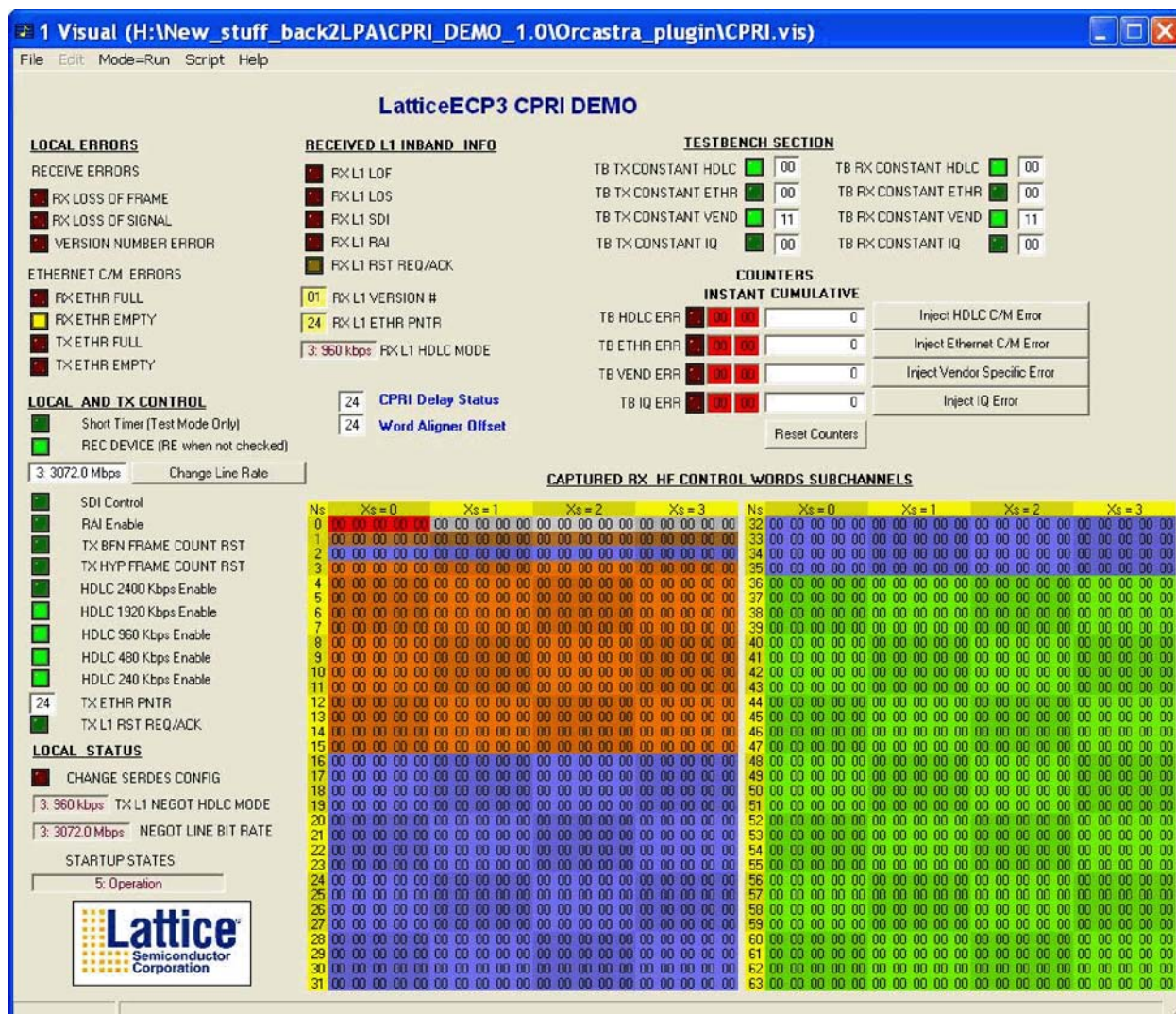
CPRI Demo ORCAstra GUI

Overview of the CPRI Demo ORCAstra Visual Window

This demo utilizes a visual window as a plug-in to the base ORCAstra installation. The visual window is associated with logical LatticeECP3 PCS Quad 1. To open the visual windows, complete the following steps.

1. Open ORCAstra and select **Custom Programmability > Visual Window**. An empty Custom Visual Interface window will appear.
2. In the Custom Visual Interface window, select **File > Open**. Browse to the directory where you have installed the CPRI Demo directory, then to **ORCAstra Plug-ins**. Select **CPRI.vis** and click **Open**. This will open the visual window plug-in for the CPRI Demo.

Figure 6. CPRI Demo ORCAstra Plug-in Visual Window



The following is a description of the control and status elements for the visual window.

Note the following:

- Red and yellow LEDs are read only
- Green LEDs are control boxes. When checked, the LED turns bright green and the corresponding register bits are set
- White text boxes contain data to be written to the register bits
- All other text boxes (yellow, red, grey, and transparent with red font) represent values that are read from the register bits

The Demo GUI is divided into sub-sections:

- Local Errors
- Received L1 Inband Info
- Local and Tx Control
- Local Status
- Testbench Section
- Captured Rx Hyperframe Control Words Subchannels – This section is a reproduction of the frame consisting of 1024 bytes of subchannels as defined in the CPRI Specification. Note that ORCAstra will capture a new frame one after another continuously when it is in continuous polling mode.

The subchannel color structure will also dynamically update based on the Ethernet Pointer value. Note that for any Ns/Xs combination, the figure frame shows a corresponding Control Word of up to 4 bytes in length. However, only the relevant bytes of control words will be displayed based on the negotiated line bit rate. For example, if the negotiated line bit rate = 1228.8 Mbps, only the first two bytes of all Control Words will be displayed. If the negotiated line bit rate = 2457.6 Mbps, all four bytes of all Control Words will be displayed. When the user points to a byte location in the captured frame, the GUI should display the information (variable/value) based on the definitions supplied in the CPRI Specification.

Key Control Buttons in the Visual Window

Under the Testbench section, the default of all the green control buttons are off. When the control buttons are turned on by clicking the green control button, it will start using constant data instead of PRBS data.

Under the Counters Instant Cumulative sub-section, four error counters continuously monitor the incoming receive data stream. Any error will be accumulated until reset to clear. Click on **Reset Counters** to clear the error counters.

Error injection: One click on the control button such as **Inject HDLC C/M Error** will inject an error in the respective Tx C&M channel data stream.

Notes:

1. To configure the proper register settings, three macros are provided. It is not recommended to manually change configuration settings such as the line rate because multiple registers are required to be set proper line rate.
2. In the visual window, to “mouse over” place the moving mouse cursor on top of the respective control or status register. A small “pop up” will indicate the address of the register. All the status and control registers are described in the Registers section of IPUG74, [CPRI IP Core Low Latency Variation Design Considerations](#).

Low Latency Status Registers in the Visual Window

Two registers related to the low latency core configuration are described in IPUG74, [CPRI IP Core Low Latency Variation Design Considerations](#).

- **CPRI Delay Status** – Read-only register at address 0x81F. Its value represents the path delay. The actual time delay is the total number of this clock count multiplied by the clock period. This clock counter value is reset when TX_sync starts. This counter value is stopped and captured when the first RX_Sync is detected. Note that during the latency demo mode, while the value of this register should be stable (constant) after every SERDES reset, its value can have a +/-1 variation after each SERDES reset due to the sampling clock frequency and data/clock boundary relationship.
- **Word Aligner Offset** – Read-only register at address 0x80B. The valid counter is 0-9, which represents the 10 phases of the SERDES bit clock. The counter value may change after each SERDES reset. In this demo, the phase variation is compensated (the phase variation compensation circuit is part of the demo reference design but not part of the CPRI IP core). After multiple SERDES resets, regardless of how the value changes in the Word Aligner Offset register 0x80B, the value in CPRI Delay Status register 0x81F should remain constant (+/-1) indicating that the phase variation compensation circuit is working successfully.

CPRI Demo Design Register Map

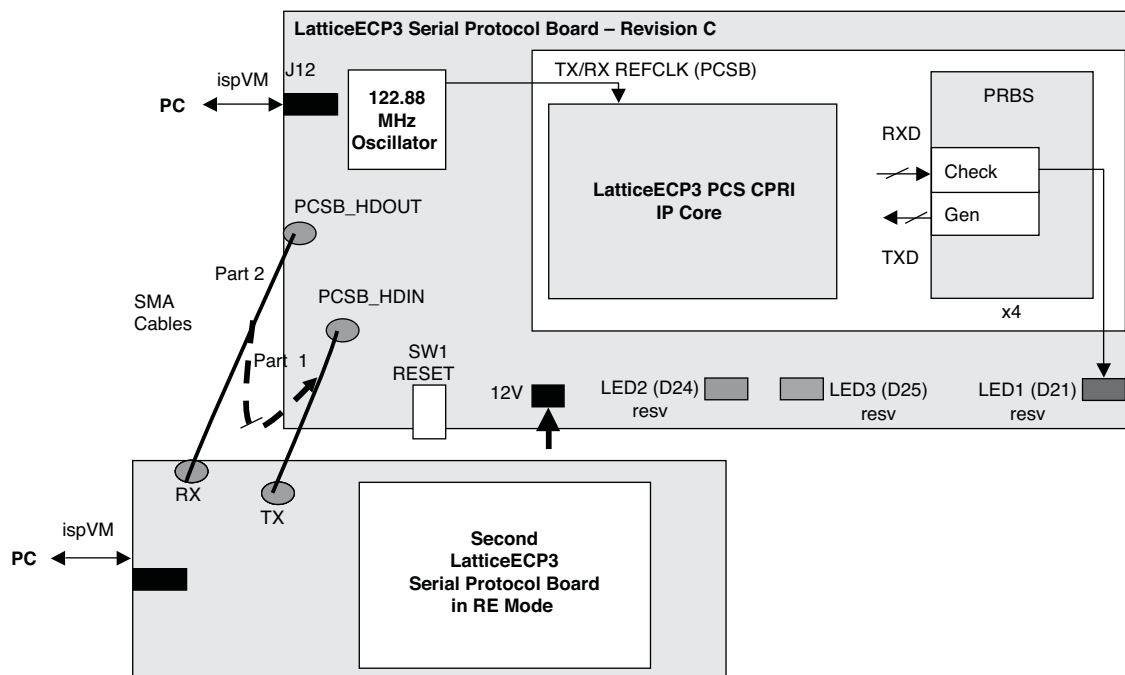
There are no user-accessible registers within the core. All control and status registers appear as internal I/O at the core boundary. User registers are provided in the testbench to drive and monitor all the control and status registers that interface with the core. These registers are shown in IPUG56, [CPRI IP Core User's Guide](#). Additional registers supporting the low latency core configuration are described in IPUG74, [CPRI IP Core Low Latency Variation Design Considerations](#).

LatticeECP3 Serial Protocol Board (Version C or Later) Setup

The CPRI Demo design transmits CPRI data in the Tx direction, loops the serial high-speed data back to the LatticeECP3 and checks the data. The setup assumes the following:

1. ispVM is installed on a PC.
2. ORCAstra is installed on a PC.
3. An ispVM download cable is connected to the USB port of the PC and to the ispVM JTAG connector on the board.
4. Two LatticeECP3 Serial Protocol Boards are set up in parallel. SERDES channels PCSB (HDOUT0 HDIN0) are connected between the two boards.
5. Power is applied to the board via the provided power supply.

Figure 7. LatticeECP3 Serial Protocol Board Setup



CPRI Demo Design Signal Descriptions

Table 1 lists all of the CPRI Demo Design signals that are connected on the LatticeECP3 Serial Protocol Board.

Table 1. Signal Descriptions

Signal Name	Type	LatticeECP3 Serial Protocol Board Connection	Description
General Signals			
reset_n	I	SW1 Push-button	FPGA global active low reset
Reference Design Signals			
Reserve	O	D24 yellow LED	N/A
JTAG Signals			
Tck	I	To J12 JTAG header	JTAG pins
Tdi	I		
Tdo	O		
Tms	I		
PCS Quad			
FPGA_SMA_P/N	I	Sourced from J38 (P) and J39 (N)	Optional SMA differential input reference clock (need to modify “sysclk_p” location to “U28” in LPF file and re-run place and route)
hdinp_0/ hdinn_0	I	SMA J13 and J14	Channel 0 differential high-speed SERDES inputs
hdoutp_0/ hdoutn_0	O	SMA J17 and J18	Channel 0 differential high-speed SERDES outputs

Loading the LatticeECP3 CPRI Demo Bitstream with ispVM

The demo package provides several bitstreams. Note that the LatticeECP3 Serial Protocol Board supports both the LatticeECP3-95 and LatticeECP3-150 packages. The demo provides bitstreams for both the -95 or -150 1156-ball fpBGA package. Select the appropriate bitstream for the device populated on the selected LatticeECP3 Serial Protocol Board.

- **REC Bitstream:** \CPRI_DEMO_x.x\Bitstream_REC_122mhz_clk\rec_***....bit
This bitstream configures the CPRI core in REC mode (hard coded) and uses the FPGA testbench generator/checkers for each of the IQ/HDLC/VENDOR and Ethernet interfaces. These testbench functions can be controlled from ORCAstra via the CPRI ORCASTRa visual GUI. This bitstream can be used to perform a single board standalone SFP loopback CPRI demo, or can be used in conjunction with another LatticeECP3.
- **RE Bitstream (Part 1: Loop time):** \CPRI_DEMO_x.x\Bitstream_RE_122mhz_clk\re_***....bit. For example, the re_95_rclkclean_spi.bit can be used for the LatticeECP3-95 1156-ball fpBGA device that has a 122.88 MHz on-board oscillator. The re_150_rclkclean_spi.bit is used for the -150 device. These bitstream use the on-board Texas Instruments (TI) clock cleaner to recondition the recover clock. When using these TI clock cleaner enabled bitstreams, users should make sure DIP switch SW14 position 8 is in the up position. This DIP switch reset (down position) the SPI control interface and load the proper configuration register to the TI CTC clock cleaner device. After both the RE and REC boards are set up and the ORCAstra macro scripts are loaded, the RE device will detect incoming data from the SERDES and detect the CPRI link. Three LED lights D13/D14/D15 on the LatticeECP3 Serial Protocol Board will turn orange to indicate the TI clock cleaning was successful. This bitstream configures the CPRI core in RE mode (hard coded) and uses FPGA testbench generator/checkers (see Figure 1) for each of the IQ/HDLC/VENDOR and Ethernet interfaces. The testbench generators and checkers are designed to generate and check the same patterns as those used in the REC design. These testbench functions can be controlled from ORCAstra via the CPRI ORCAstra visual GUI. This bitstream is used in conjunction with another LatticeECP3 or third-party REC board.
- **RE Bitstream (Part 2: Data loopback in synchronous mode):**
\CPRI_DEMO_x.x\Bitstream_RE_122mhz_clk\ne_re_95_data_loopback.bit
This bitstream configures the CPRI core in RE mode (hard coded) and loops received data back to the TX side. The testbench generators are not used. This bitstream is used in conjunction with another LatticeECP3 or third-party REC board. When running this ne_re_data_loopback demo, connect SMAs J38/J39 between the REC and RE boards. The REC board provides the RE board with a reference clock as they are running in synchronous mode and share the same reference clock source.

Follow the instructions below to load the CPRI bitstream for the REC LatticeECP3 Serial Protocol Board.

If ORCAstra is already loaded, make sure Interface is set to **None**.

1. Start ispVM v.17.4 or higher.
2. Click on the green **Scan** icon.
3. Make sure devices 2 and 3 are in bypass.
4. Make sure device 1 selects LFE3-95_ES or equivalent -95 device on the board. If using a LatticeECP3 Serial Protocol Board that includes the LatticeECP3-150 device, make sure to use the "EA" device instead of the "E" version.
5. Make sure the device 1 bitstream file name points to a bitstream that matches the proper device on your evaluation board: <your_project_path>\CPRI_DEMO_x.x\Bitstream_REC_122mhz_clk\rec_***....bit and that **Operation** is set to **Fast Program**.
6. Click **Go**.
7. The bitstream should program successfully.

To perform an REC-RE demo, after setting up the REC board and REC bitstream download, follow the instructions below to load the CPRI bitstream for the RE LatticeECP3 Serial Protocol Board.

1. Repeat the same steps as for the REC evaluation board except make sure the device 1 bitstream file name points to the proper RE bitstream for the matching device on the LatticeECP3 Serial Protocol Board:
<your_project_path>\CPRI_DEMO_x.x\Bitstream_RE_122mhz_clk\re_***....bit

Figure 8. ispVM Setup

New Scan Configuration Setup*					
Index	Device List	FileName/IR-Length	Operation	Status	
1	LFE3-95E-ES	H:\New_stuff_back2LPA\CPRI_DEMO_1.0\Bitstream_REC_122mhz_clk\rec_cpri_demo_reference_eval.bit	Fast Program	N/A	
2	LCM60D1200C		FLASH Bypass	N/A	
3	ispPAC-POWER1220AT8		Bypass	N/A	

Running a Demo with the ORCAstra PCS View

This section describes the use of the ORCAstra GUI to interactively change/monitor LatticeECP3 PCS and user registers.

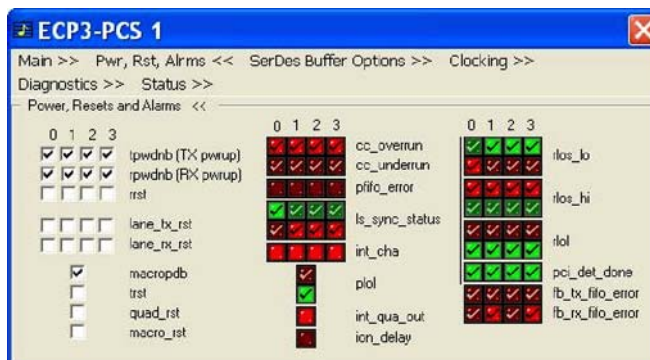
Starting ORCAstra

ORCAstra Setup for REC

Ensure the LatticeECP3 CPRI Demo bitstream has been loaded on the REC evaluation board, then:

1. Start ORCAstra version 2.3.14 or later
2. Select **Interface > 3. ispVM JTAG HUB USB Interface**. If the **Select Target JTAG Device** window comes up, select **ECP3 device** and click **OK**.
3. Select **Device > LatticeECP3**.
4. Issue board hardware reset (SW1 switch on the board).
5. Load macro from <your_project_path>\CPRI_DEMO_x.x\Orcastra_plugin\Orcastra_macro*.fpm to set the desired line rate.
6. In the ORCAstra control window write **0x11** to address **00211** to set the SERDES in serial loopback.
7. Click on **ECP3 PCS1** option. This will launch the ECP3-PCS1 Visual Window. Close the **Main** tab, and open the **Pwr**, **Rst**, **Alrms**, and **SerDes Buffer Options** tabs. The PCS GUI is useful for checking for the status of the PCS registers. Note that:
 - a. The PCBB (PCS1) channel 0 for **Is_sync_status** should be green.
 - b. The **Plol** LED should be green.
 - c. This means that the PCS is locking to the clock and the receive section of the channel has properly synchronized to the incoming data. If **Plol** or **Is_sync_status** are red, check the SERDES reference clock source, or rerun the macro again, or check and then uncheck the PCS GUI macro_rst.

Figure 9. LatticeECP3 PCS 1 ORCAstra View



8. From the main ORCAstra Control Center, select **Custom Programmability > Visual Window**.
9. In the new window, select **File > Open > <your_project_path>\CPRI_DEMO_x.x\Orcastra_plugin\cpri.vis**.
10. You will see the LatticeECP3 CPRI Demo window.
11. Make sure **Continuous Polling** is checked in the main ORCAstra window.

ORCAstra Setup for RE Loop Time Mode

Ensure the LatticeECP3 CPRI Demo bitstream has been loaded on the RE evaluation board, then:

1. Load the same macro for the RE board as in the previous step for the REC.
2. Run the ORCAstra setup for the REC procedure, but do not repeat step 6 since in RE mode there is no need to set SERDES serial loopback.
3. Repeat the same steps as for the REC evaluation board.

Note: Using the TI clock cleaner enabled RE bitstreams, users must make sure DIP switch SW14 position 8 is in the up position. Toggle this DIP switch to reset the SPI control interface and load the proper configuration register to the TI CTC clock cleaner device. After both the RE and REC boards are set up and the ORCAstra macro scripts are loaded, the RE device will detect incoming data from the SERDES and detect the CPRI link. Three LED lights D13/D14/D15 on the LatticeECP3 Serial Protocol Board will turn orange to indicate the TI clock cleaning has been successful. The demo package provides three ORCAstra macros under \..\Orcastra_plugin\Orcastra_macro

- *PCS_1228Mbps_config_ECP3.fpm*
- *PCS_2458Mbps_config_ECP3.fpm*
- *PCS_3072Mbps_config_ECP3.fpm*

These can be used to configure the different line rates of 1.228/2.458/3.072 Gbps.

ORCAstra Setup for NE_RE Data Loopback Mode

Load the NE_RE data loopback bistream on the RE demo board. Set the proper data rate by loading the ORCAstra macro.

Disable self-data-loopback on the REC device by setting 0x211 to 0x01.

In this mode, only REC ORCAstra GUI hyperframe capture and monitor is used for error injection and monitoring. Run the demo similar to the REC-standalone data loopback demo procedure.

Configuring PCS 1 Options in ORCAstra

The default Pwr, Resets and Alarms section contains the following important information:

- Green/red LEDs (one per channel) to indicate that the receive link state machines are synchronized (ls_sync_status). Green indicates successful synchronization.
- Green/red LEDs (one for whole quad) to indicate that the SERDES transmit PLL (plol) is locking. Green indicates successful lock.
- Green/red LEDs (one per channel) to indicate Receive CDR lock (rlol). Green indicates successful lock.

In this view, users can identify which channels (or the entire quad) are powered down or reset. Users can also reset PCS digital logic (lane_tx_rst and lane_rx_rst), as well as SERDES logic (macro_rst) and the whole quad (quad_rst).

Typical CPRI Demo Applications

REC Loopback Demo

The following section describes the REC loopback demo. In this setup:

- Only one LatticeECP3 Serial Protocol Board is used. Test data traffic is generated in the FPGA test bench (FPGA test bench is used as a general term here, referring to the FPGA CPRI data generators and checkers), and is transmitted through the CPRI core, PCS, SERDES out of the device and then looped back through either SERDES serial loopback or SMA cables. The device is configured in CPRI REC mode.
- As described in the ispVM Download and ORCAstra Macro Setup section, at this point,
 - LatticeECP3 CPRI Demo GUI status:
 - The Startup state should reach state 5
 - None of the red LEDs should be blinking
 - The negotiated rate should be at 1228, 2457 or 3072 Mbps depending on which macro file was chosen.
 - The Rx L1 HDLC Mode rate should match the highest common REC/RE HDLC rate. HDLC rate can be changed by clicking any of the HDLC-enabled green LEDs in the Local and Tx Control section.
 - The Rx L1 ETHR PNTR status should match the Tx ETHR pointer value.
 - Clear the error counter by clicking the counter reset in the visual window. In the testbench section of the REC device CPRI Demo GUI, the instant data (IQ, HDLC, Ethernet, Vendor) error counters should be 0 and the cumulative data error counters should not increment.
 - To change the Tx Ethernet pointer value (REC only), uncheck **Continuous Polling** in the main ORCAstra window, then go back to the LatticeECP3 CPRI GUI window, type the desired HEX value, and press **M** on the keyboard. This saves the new value. Return to the main ORCAstra window and check **Continuous Polling** again. The new value will remain. Note that the Tx and Rx Ethernet pointer values are in HEX.
 - In the Testbench section, to change the values in the Constant Data Boxes, uncheck **Continuous Polling** in the main ORCAstra window. Then go back to the LatticeECP3 CPRI GUI window, type the desired HEX value and press **M** on the keyboard. This saves the new value. Return to the main ORCAstra window and check **Continuous Polling** again. The new value will remain. All values are in HEX. Note the following:
 - It is not enough to set the constant values in the data boxes. It is also necessary to check the green LED for Tx and Rx for constant data to be transmitted and checked. If the green LEDs are not checked, then the default random or numbered DATA is sent (REC) and checked (REC and RE).
 - The Ethernet interface does not support constant data (testbench limitation). The HDLC interface only supports 0x00 constant data for constant.
 - Continuous capturing of the HyperFrame. In the HyperFrame section, the bytes that are relevant to the negotiated bit rate will appear in bold font:
 - For 1228Mbps, only two bytes are bold for every control word.
 - For 2457Mbps, all 4 bytes are bold for every control word.
 - For 3072Mbps, all 5 bytes are bold for every control word.
 - The Ethernet C/M section of the HyperFrame (green section) will change based on the value of RX L1 ETHR PNTR polled at the time of the HyperFrame capture.
 - To change the line rate, load the appropriate macro. It is not enough to push the Change Line Rate push-button in the CPRI Demo GUI, because this button does not change to the PCS configuration to match the new

line rate. Only the macro files change the PCS configuration to match the corresponding line bite rate.

Low Latency

- When the REC loopback is running smoothly in loopback mode (internal loopback, register 211 setting is 11, the CPRI Delay Status register value shall remain as a constant (+/-1).
- Reset the REC SERDES or re-download the macro. The Word Aligner Offset register may have a new value. The CPRI Delay Status register value shall remain as the same constant as the previous value (+/-1).
- Reset the RE SERDES or re-download the macro. The Word Aligner Offset register may have a new value. The CPRI Delay Status register value will change but then it shall remain as a constant when ORCAstra in continuous polling mode.

REC-RE Loopback Demo (Recover Clock Loop Time)

In the REC-RE part 1 demo setup, an RE device is used to demonstrate the loop timing mode and a recover clock is used as reference clock for the transmit data.

- Two LatticeECP3 Serial Protocol Boards are used. In the RE device, test data traffic is coming from REC through the SMA port. Make sure REC HDOUT* are connected to RE HDIN* SMA.
- Once REC is up and loopback mode is running, download the RE bitstream and load the respective ORCAstra macros to the RE device.
- The RE bitstream does not use the Tx testbench options of the LatticeECP3 CPRI Demo GUI. Only the RX testbench options are useful.
- Similar to the REC receive side, from the RE device, perform the tasks to monitor the error status, error counter and hyperframe capture.
- If hyperframe capture continues while all error counters remain at zero, the CPRI checker is receiving error-free packets.
- If any of the error counters increment, then the CPRI checker is receiving packets with errors.
 - Verify that the Power, Reset and Alarm section of PCS 1 CPRI View does not show any PLL loss of lock (plol), CDR loss of lock (rlol), or internal link state machines loss of sync (ls_sync_status).
 - A red plol indicates that the reference clock source to the Tx PLL is not stable.
 - A red rlol indicates incorrect activity on the HDIN* inputs. The input signals may be too attenuated by the medium. Also, if the data was transmitted from a different device, the reference clock transmitting the HDIN* input data may not be within the required +/-100 ppm of the local reference clock. The latter issue, though rarely the case, needs to be addressed.
 - Reset, or reload the bitstream and reload macro.

Note: In the current REC-RE loopback demo, the recovered clock in the RE device is used to clock all the Tx circuits and testbench data generation. The TI clock cleaner is used in this version of the demo design. Therefore this recovered clock has been jitter-cleaned.

Debugging tip: During re-configuration, keep the CPRI visual window closed. If the control PC loses its connection with ORCAstra, it can cause ORCAstra and the circuit to lock up or lose PLL lock or link status. If this happens, close ORCAstra, power down the board, re-download the bitstream and repeat the ORCAstra connection procedure.

Low Latency

- When the REC loopback is running smoothly on the first evaluation board, and the second RE evaluation board is receiving data without error from the REC device, the CPRI Delay Status register value shall remain as a constant (+/-1).
- Reset the REC SERDES or re-download the macro. The Word Aligner Offset register may have a new value. The CPRI Delay Status register value shall remain as the same constant as the previous value (+/-1).

- Reset the RE SERDES or re-download the macro. The Word Aligner Offset register may have a new value. The CPRI Delay Status register value will change but then it shall remain as a constant when ORCAstra in continuous polling mode.

REC-RE Loopback Demo (Data Loopback)

In this part of the REC-RE demo setup, data is looped back into the RE device. To simplify the design while supporting all three data rates, both REC and RE are running in synchronous mode and using the same system reference clock.

- Two LatticeECP3 Serial Protocol Boards are used. In the RE device, test data traffic is coming from REC through the SMA port. Make sure the REC HDOUT* are connected to the RE HDIN* SMA.
- Using a second pair of matched SMA cables, connect the J38 and J39 SMA ports between the REC and RE boards.
- Once REC is up and SERDES buffer loopback mode (setting register 0x211 to "11") is running without error, download the RE bitstream and load the respective ORCAstra macros to the RE device.
- The RE bitstream does not use the Tx testbench options of the LatticeECP3 CPRI Demo GUI. Only the RX testbench options are used.
- Similar to the REC receive side, from the RE device, hyperframe capture is valid and can be used to monitor incoming data. But in this operation, REC hyperframe capture is the primary data monitoring stage to check whether the complete data path is looping data through properly.
- Once both REC and RE are set up for matching data rates, and REC self loopback is running properly, turn off the REC self loopback by setting register 0x211 to "01".
- Clear the ORCAstra CPRI RX testbench error counters. If hyperframe capture continues to receive valid data while all error counters remain at zero, the CPRI checker is receiving error-free packets.
- Disconnect the cable between the RE HDOUT port and the REC HDIN port. Verify that errors can be detected only in the RE visual window. Reconnect the cable.
- Disconnect the cable between the REC HDOUT port and the RE HDIN port. Verify that errors can be detected in both the REC and RE visual windows.
- If any of the error counters increment, then the CPRI checker is receiving packets with errors.
 - Verify that the Power, Reset and Alarm section of PCS 1 CPRI View does not show any PLL loss of lock (plol), CDR loss of lock (rlol), or internal link state machines loss of sync (ls_sync_status).
 - A red plol indicates that the reference clock source to the Tx PLL is not stable.
 - A red rlol indicates incorrect activity on the HDIN* inputs. If the data was transmitted from a different device, the reference clock transmitting the HDIN* input data may not be within the required +/-100 ppm of the local reference clock.
 - Reset, reload the bitstream and reload the macro.

Implementing and Simulating the Reference Design

The steps below explain how to run the CPRI reference design source code through ispLEVER Project Navigator map, place and route, bitstream generation, and simulation.

Both implementation and simulation start with the same steps:

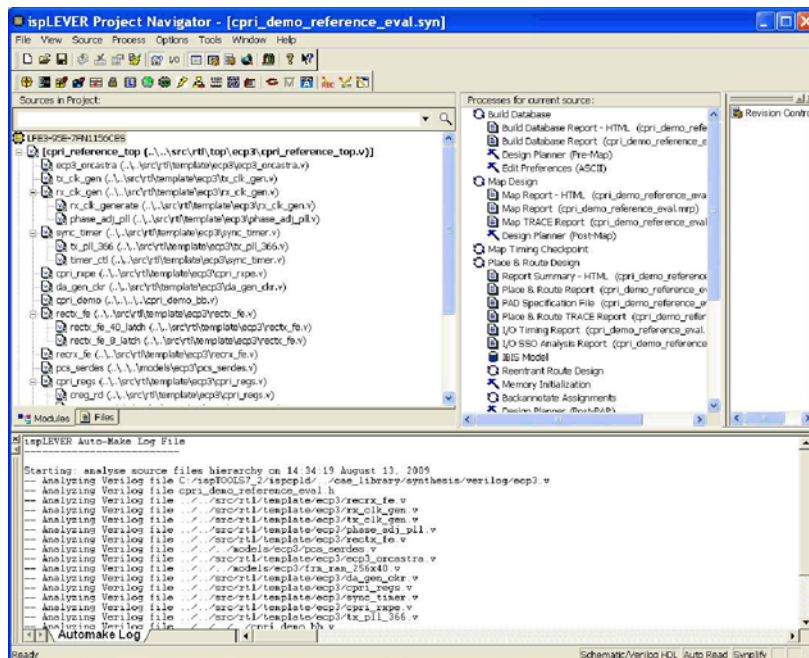
1. Start ispLEVER Project Navigator
2. Open **<your_project_path>CPRI\Target\CPRI_Demo_reference_eval.syn**. This will load the Verilog-based project as shown in Figure 10.

Two *.syn project files are provided in the demo package under the directories:

- \your_project_dir\CPRI_DEMO_x.x\REC_RE_target\cpri_lowlatency_eval\cpri_demo\impl\REC_reference
- \your_project_dir\CPRI_DEMO_x.x\REC_RE_target\cpri_lowlatency_eval\cpri_demo\impl\RE_reference

One project contains the project for REC implementation and the other for RE implementation.

Figure 10. Project Navigator

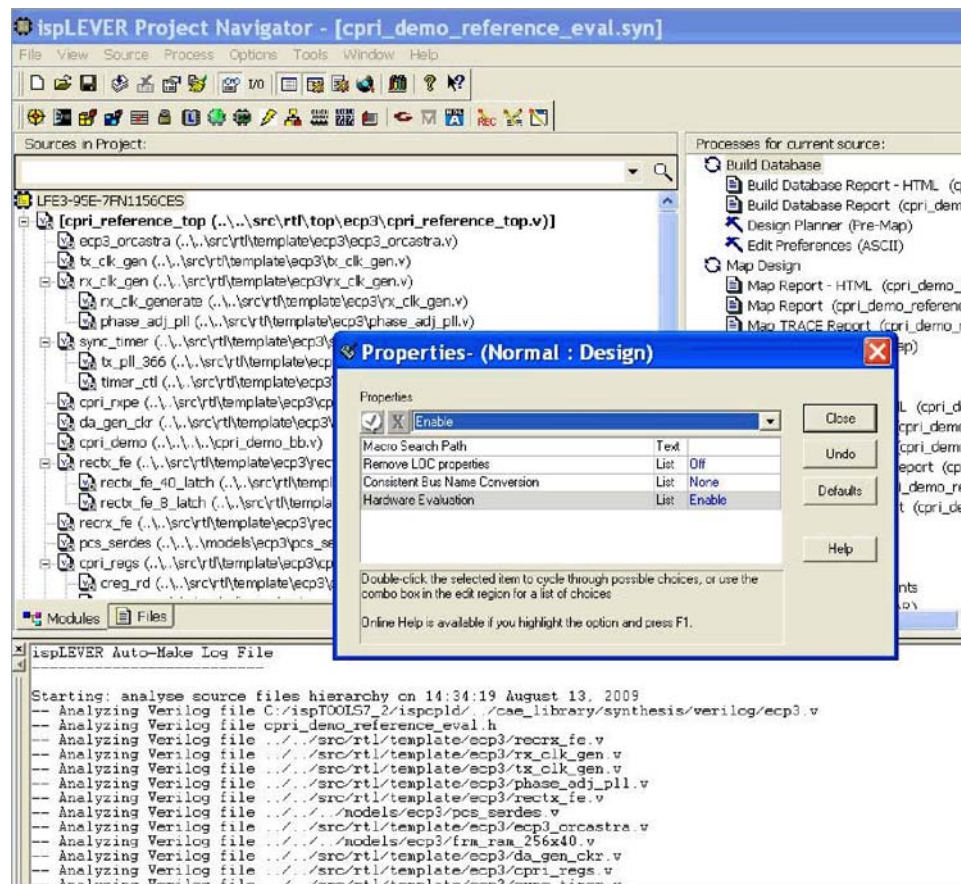


Implementation

Follow the steps below as illustrated in Figure 11.

1. Select **Build Database** in the **Processes** window, then right-click and select **Properties**.
2. In the **Properties** windows, set the **Hardware Evaluation** value to **Enable**. Lattice's IP hardware evaluation capability makes it possible to create versions of IP cores that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. The hardware evaluation capability is turned on by enabling the **Hardware Evaluation** option in the properties of the **Build Database** process in ispLEVER. When the Hardware Evaluation option is enabled it is possible to generate a programming file that may be downloaded into the device. After initialization, the IP core will be operational for approximately four hours. After four hours, the IP core will stop working and it will be necessary to reprogram the device to re-enable operation. This hardware evaluation capability is only enabled if the core has not been licensed. If a license is detected, core generation is completed with no restrictions.
3. Click **Close**.

Figure 11. Build Database Properties



To implement the design and generate a bitstream, double-click the **Generate Bitstream Data** target in the **Processes** window. This will run through the full synthesis, place and route flow and generate a new bit file. Re-download the new bitstream file and run the demo procedure as described before.

Simulation

Simulation Script

The simulation process uses the Aldec Active-HDL simulation script located under the simulation directory `your_project_dir_name\CPRI_DEMO_x.x\REC_RE_target\cpri_lowlatency_eval\cpri_demo\sim\aldec\rtl\`:

- verilog_cpri_demo_1230_reference_eval_oem.do
- verilog_cpri_demo_2460_reference_eval_oem.do
- verilog_cpri_demo_3072_reference_eval_oem.do

These scripts are for REC simulation at the different line rates of 1230/2460/3072 Mbps.

Use a text editor to modify the script so that the path name is pointing to the proper location. The name of your project directory might differ from the default path.

For example: the current default path is:

H:/New_stuff_back2LPA/CPRI_DEMO_x.x/temp_ip-exp/cpri_lowlatency_eval/cpri_demo/sim/aldec/rtl

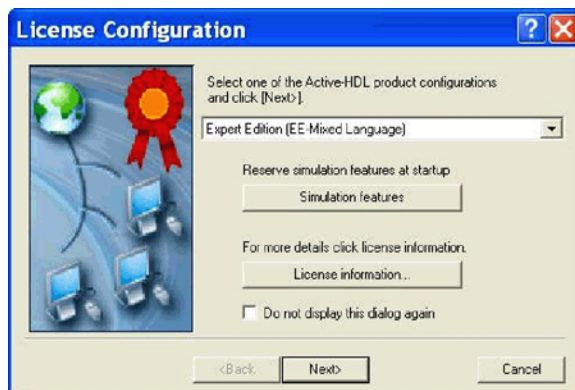
which might need to be changed to:

H:/New_stuff_back2LPA/CPRI_DEMO_x.x/REC_RE_target/cpri_lowlatency_eval/cpri_demo/sim/aldec/rtl

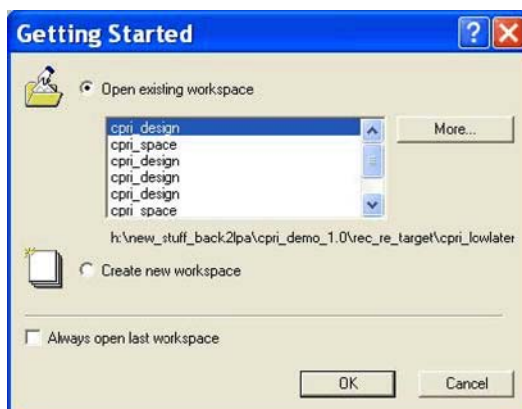
Simulation Procedure

Follow the steps below.

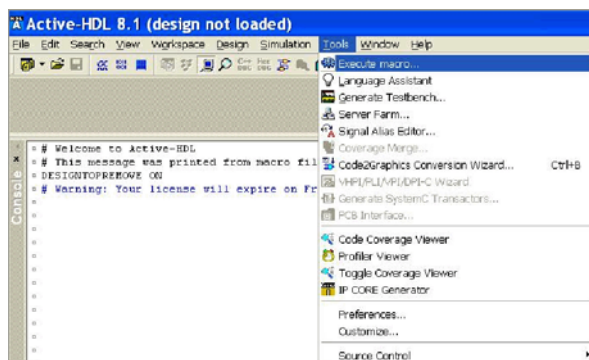
1. Invoke the Active-HDL tool.



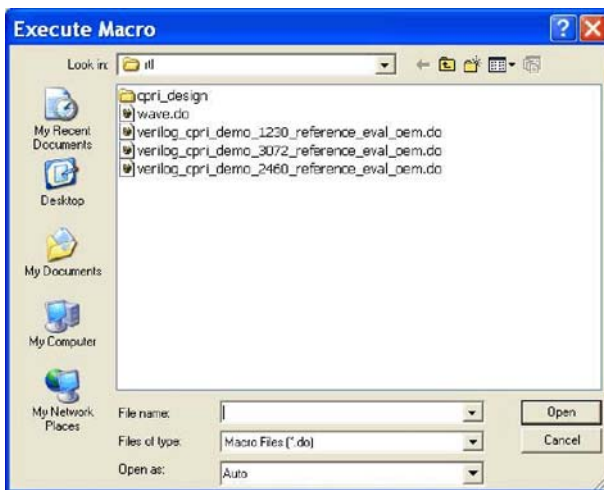
2. Click on **Next** and launch the **Getting started** window. Then click on **Cancel** (don't create a new project).



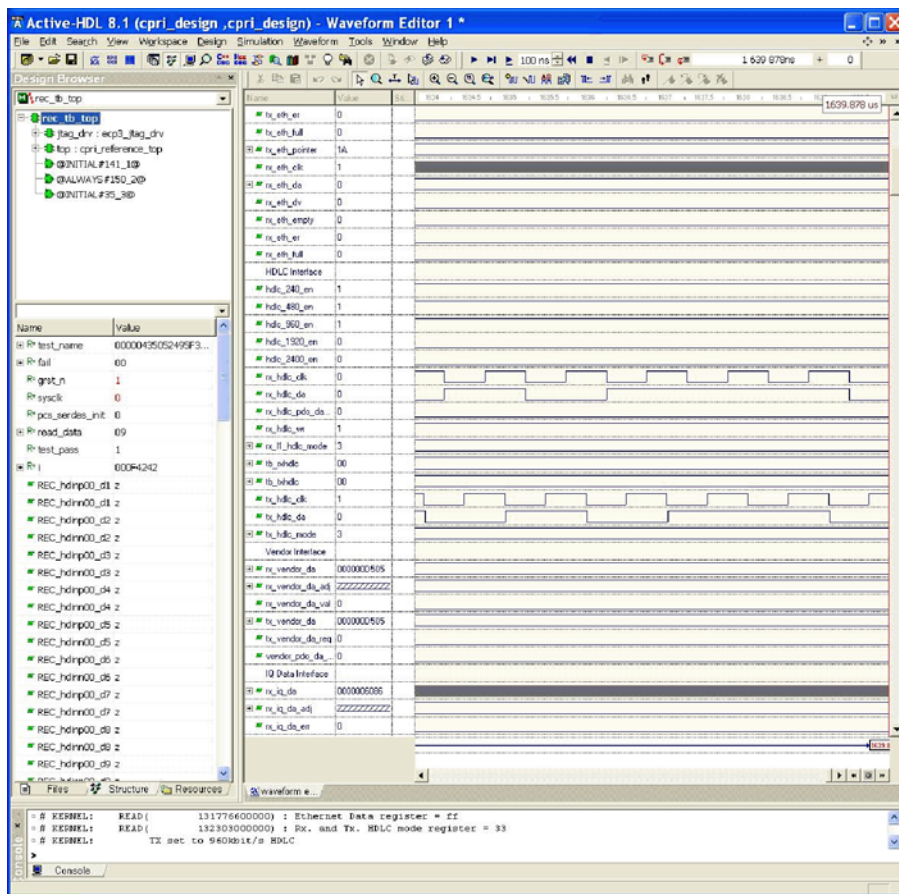
3. Under the **Tools** pull-down menu click on **Execute macro**.



4. Go to the **Script** directory and select the proper do file to start simulation.



- The script compiles all necessary design and testbench files and runs the simulation into the Active-HDL Waveform window shown below. The changing clocks, generated data and loopback data in C&M channels can be viewed in waveform, which indicates a functioning simulation testbench.



Reference Information

The following documents provide more information:

- TN1176 – [LatticeECP3 SERDES/PCS Usage Guide](#)
- EB44 – [LatticeECP3 Serial Protocol Board - Revision D User's Guide](#)
- EB49 – [LatticeECP3 Serial Protocol Board - Revision E User's Guide](#)
- IPUG56 – [CPRI IP Core User's Guide](#)
- IPUG74 – [CPRI IP Core Low Latency Variation Design Considerations](#)

Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2009	01.0	Initial release.
April 2010	01.1	Added JTAG HUB support and Reveal support.
		Added support for RE Data loopback mode in synchronous timing mode at three line rates and capture features.
		Added ispLEVER 8.0 support.
		Added support for RE recovered clock jitter cleaning.
May 2012	01.2	Updated document with new corporate logo.
		Clarified FPGA source of PCS refclk.