SERDES Eye/Backplane Demo for the LatticeECP3 Serial Protocol Board

User's Guide

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UG24_01.4

Introduction

This document provides technical information and instructions on using the LatticeECP3™ SERDES Eye/Backplane Demo Design. The demo has been designed to demonstrate the performance of the LatticeECP3 SERDES I/O at 3.125 Gbps. The document provides a circuit description as well as instructions for running the demo on the LatticeECP3 Serial Protocol Board.

In addition to this user's guide the SERDES Eye/Backplane Demo comes with the following:

- Verilog source code for the FPGA design
- ispLEVER Project Navigator implementation Project file and Aldec® Active-HDL® simulation script
- Bitstream (in format of *.bit)
- ORCAstra Plug-in GUI

Hardware requirement for this loopback application test design:

- LatticeECP3 Serial Protocol Board (Revision C or newer) with LatticeECP3-95, 1156-ball fpBGA device.
- Power module
- PC with ORCAstra (PC not provided)
- 156.25 MHz on-board oscillator for SERDES/PCS QUAD reference clock
- Optional Clock Generator instrument (instrument not provided)
- Backplane with SMAs (not provided)
- Pair of DC Blocks (not provided)
- Eye viewing instrument - DCA, DSO, etc. (not provided)
- SMA cables
- ispVM JTAG to USB download cable

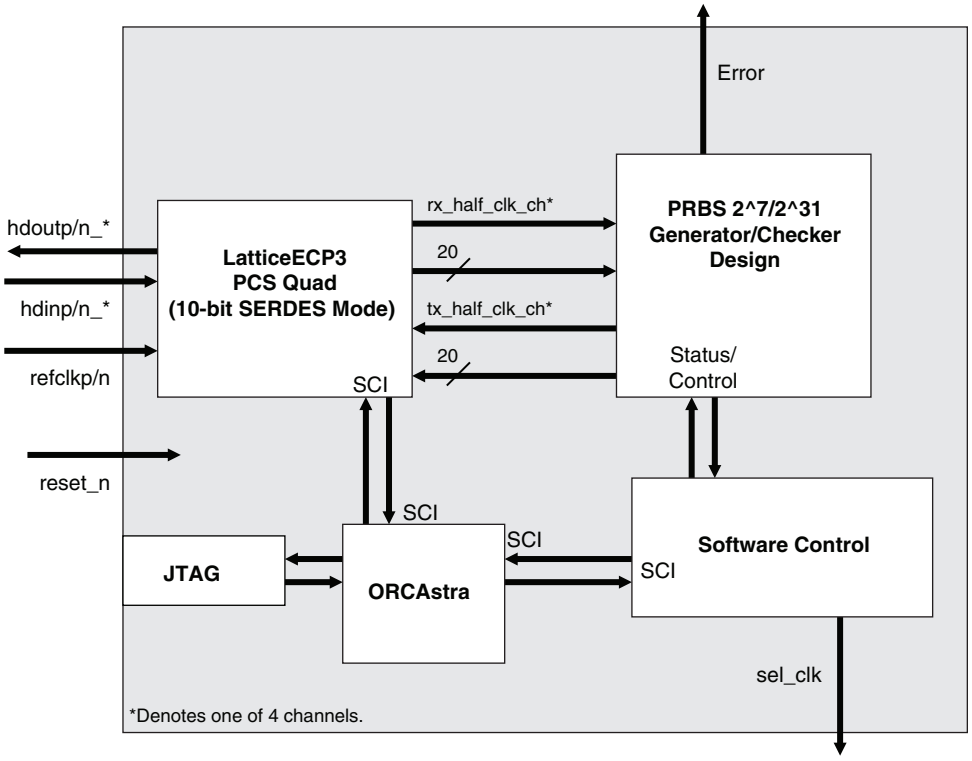
Software application and driver requirements include:

- ispVM™ System software (version 17.4 or later) for FPGA bitstream download
- ispLEVER® design software version 7.2 SP2 or later
- ORCAstra software for user control interface - Included with ispLEVER 7.2 SP2 or later

SERDES Eye/Backplane Demo Design Overview

A block diagram of the demo design is provided in Figure 1.

Figure 1. SERDES Eye/Backplane Demo Design



The basic concept of the design is a quad-based PRBS Generator/checker that transmits four channels of parallel data to a PCS quad. In turn, the PCS SERDES channels serialize the data in the transmit direction, and de-serialize it in the receive direction. The serial data stream can be:

- Looped back via a cable on the evaluation board, or
- Sent to a DCA or DSO for eye viewing.

In both cases, a backplane of variable length can be included in the serial path.

For this demo, PCS quad location PCSB is used. It has been generated in 10-bit SERDES only mode (20-bit data), at 3.2 Gbps per channel (actual demo rate is 3.125 Gbps or equivalent). Note that the reference design implements the LatticeECP3 PCS TX and RX Reset State machines described under the SERDES/PCS RESET section of TN1176, LatticeECP3 SERDES/PCS Usage Guide.

Clock Sources

PCS quad B is clocked by its designated differential external reference clock input, refclkp/n. The reference clock's frequency is 156.25 MHz and has two potential sources: The on-board Y1 differential oscillator or SMA differential inputs J29 (P) and J33 (N) to the board. The clock selection is controlled by an output signal (sel_clk) which is controlled by an internal user register bit. Internally to the PCS, the reference clock is multiplied by a factor of 20 to generate the 3.125 Gbps per channel data rate. At the PCS/FPGA interface, a 20-bit data interface is used. This requires 156.25 MHZ receive and transmit clocks. The PCS-generated rx_half_clk_ch* and tx_half_clk_ch* (see Figure 1) clock the PCS interface as well as the PRBS Generator/Checker RX and TX data.

PRBS Generator/Checker Quad

There is one PRBS Generator/Checker quad block in the demo design. It is associated with PCS Quad B.

The PRBS generator/checker quad has the following characteristics:

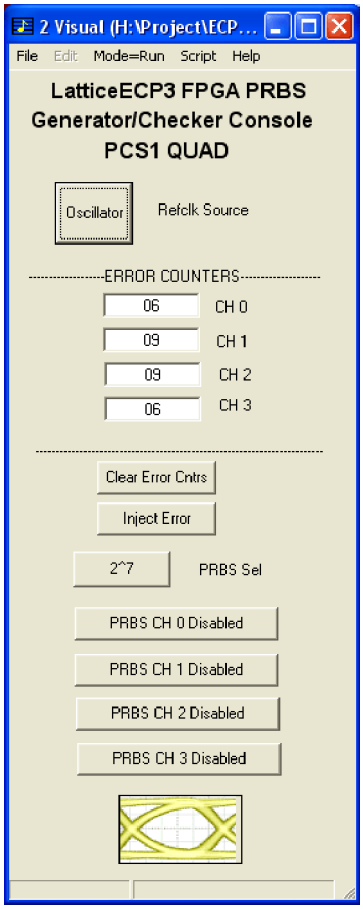
- 4 channels of 20-bit wide data
- 1 PRBS Generator (2^7 and 2^31) per channel (four generators total per quad)
- 1 PRBS Checker (2^7 and 2^31) per channel (four checkers total per quad)
- Control/Status interface to user registers.
- 1 Error Counter per checker (4 total per quad) connected to a user register for monitoring.
- 1 real time Error signal indicator per checker (4 total per quad) connected to an on-board LED.

The ORCAstra block controls all user registers as well as the LatticeECP3 PCS QUAD via the SCI interface. ORCAstra is in turn controlled via the JTAG interface. See Figure 1.

PRBS Generator/Checker QUAD ORCAstra GUI

This demo utilizes a visual window plug-in to the base ORCAstra installation. The visual window is associated with logical LatticeECP3 PCS Quad 1. Figure 2 provides a screen capture of this window.

Figure 2. PRBS Generator/Checker Quad ORCAstra Plug-in Visual Window



REFCLK SOURCE: This button allows the user to select either the on-board differential oscillator or the external SMA differential inputs as the source of the refclkp/n to the PCS SERDES.

PRBS CH 0-3 DISABLED/ENABLED: This enables/disables both the transmission of PRBS data from the generator, and the detection of errors by the checkers of a quad. When this button is disabled, the PRBS ERROR counters

in the visual window stop incrementing, and the real time output PRBS Error signal indicators (see Figure 1 and Table 2) remain low.

2^31/2^7 Button Selection: This button allows the selection of either 2^7 or 2^31 PRBS generation and checking.

Error Counters: There are four hexadecimal error counters, corresponding to the four channel checkers in a quad. Each error counter increments every time errors are detected at the checker. Each counter is only eight bits wide, so the maximum count reached is hFF. When the counter reaches hFF, it does not roll back to zero unless the Clear Error Counters button is checked. A counter will not increment unless the corresponding PRBS channel is enabled.

Clear Error Counters: When checked, it asynchronously clears the content of all 4-channel PRBS checker Error Counters.

Inject Error: The design injects a single incorrect parallel data word in the transmitted PRBS data every time a positive edge occurs on the register bit associated with the Inject Error check box. So, an incorrect data word is inserted every time the Inject Error box is unchecked then checked. The PRBS channel needs to be enabled for this error injection feature to work. Note that in the current version of the PRBS Generator/Checker design, when a channel is in SERDES near-end (HDOUT->HDIN) loopback, a single incorrect data word injected by a channel generator does not always correspond to a single count increment in the checker error counter. The injected error can cause the error counter to increment by as much as three counts. Also, the 4-channel error checker counters may not increment by the same amount in response to an error injection. This is attributed to the nature of the PRBS checker design.

PRBS Generator/Checker User Registers Map

The user registers for the PRBS generator/checker quad are defined in Table 1. All register addresses are in hexadecimal. Also note that register address h00800 (not shown in Table 1) is a read-only register that contains the version number of the design.

Table 1. User Registers Map

GUI Option	PCSB FPGA Registers				Description
	ch0	ch1	ch2	ch3	
PRBS SELECT	08000, bit 0				0=2^7-1 1=2^31-1
PRBS EN	08000, bit 1	08000, bit 5	08000, bit 6	08000, bit 7	0=disable 1=enable
PRBS ERR CNT	08001, bits [0:7]	08002, bits [0:7]	08003, bits [0:7]	08004, bits [0:7]	Count up to flip-flop. Clear on read.
Inject Error	08000, bit 2				Write 0 then 1 to inject error.
Clear Error Counters	08000, bit 3				Write 0 to clear.
Select Clock	08000, bit 4				0 for on-board oscillator, 1 for external clock source

LatticeECP3 Serial Protocol Board (Version C or Newer) Setup

There are two evaluations that can be done using the SERDES Eye/Backplane Demo design. The first demo is to loop the PRBS data back to the LatticeECP3 and check the data. The second demo evaluates the CML eye diagram of the high-speed data signal to a DCA (or DSO). These setups assume the following.

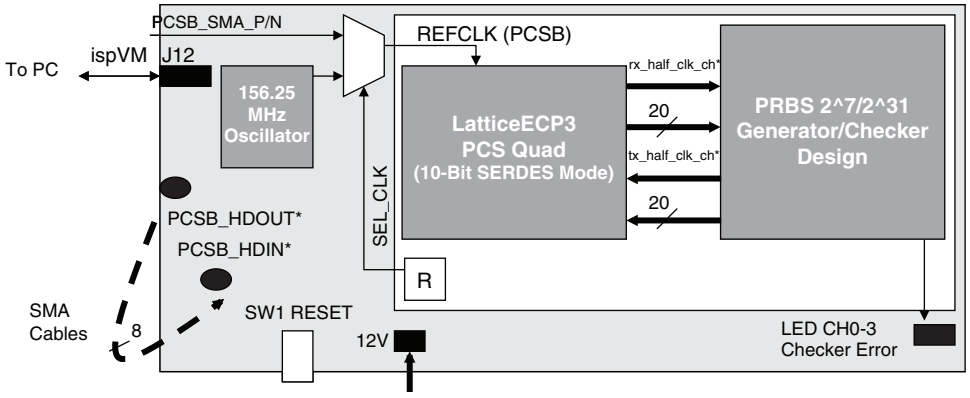
1. ispVM is installed on a PC.
2. ORCAstra is installed on a PC.
3. Internal 156.25 MHz oscillator clock source, or optional 156.25 MHz external CML differential clock source through SMA inputs

4. ispVM download cable connected to the USB port of the PC and to the ispVM JTAG connector on the board.

5. Power is applied to the board via the provided power supply.

Figure 3 shows the power supply, ispVM and the reference clock setup for the reference design.

Figure 3. LatticeECP3 Serial Protocol Board Setup



SERDES Eye/Backplane Demo Design Signal Descriptions

Table 2 lists all the SERDES Eye/Backplane Demo Design signals that are connected on the LatticeECP3 Serial Protocol Board, Version C or newer.

Table 2. Signal Descriptions

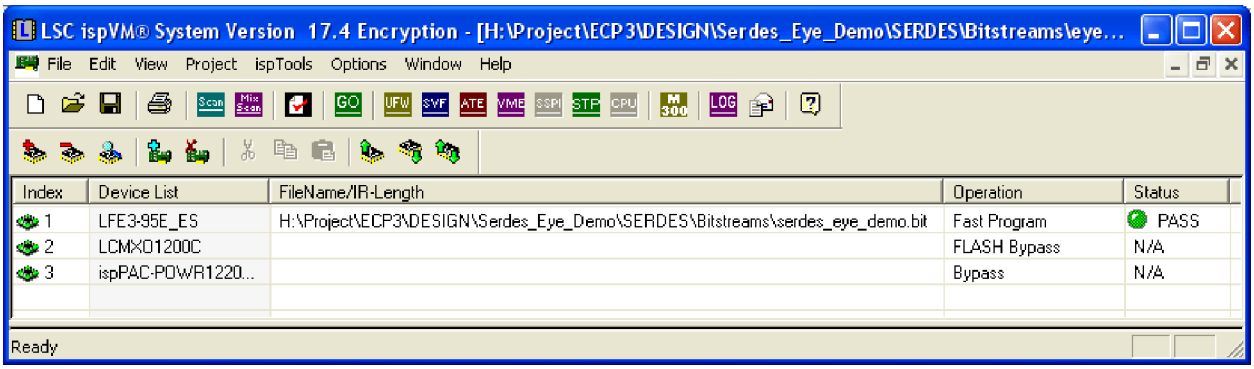
Signal Name	Type	Board Connection	Description
reset_n	I	SW1 Push Button	FPGA global active low reset
tck	I	To on-board JTAG logic	JTAG pins
tdi	I		
tdo	O		
tms	I		
Error_0	O	RED LED D21 (LED1) lights when errors occur	PRBS error indicator for channel 0. Will not light if PRBS EN in Visual GUI is unchecked.
Error_1	O	YELLOW LED D24 (LED2) lights when errors occur	PRBS error indicator for channel 1. Will not light if PRBS EN in Visual GUI is unchecked.
Error_2	O	GREEN LED D25 (LED3) lights when errors occur	PRBS error indicator for channel 2. Will not light if PRBS EN in Visual GUI is unchecked.
Error_3	O	BLUE LED D27 (LED4) lights when errors occur	PRBS error indicator for channel 3. Will not light if PRBS EN in Visual GUI is unchecked.
PCSB_SMA_P/N	I	Sourced from J29 (P) and J33 (N)	Optional SMA differential input reference clock
hdinp_0/ hdinn_0	I	SMA J13 and J14	Channel 0 differential high-speed SERDES inputs
hdinp_1/ hdinn_1	I	SMA J15 and J16	Channel 1 differential high-speed SERDES inputs
hdinp_2/ hdinn_2	I	SMA J21 and J22	Channel 2 differential high-speed SERDES inputs
hdinp_3/ hdinn_3	I	SMA J23 and J24	Channel 3 differential high-speed SERDES inputs
hdoutp_0/ hdoutn_0	O	SMA J17 and J18	Channel 0 differential high-speed SERDES outputs
hdoutp_1/ hdoutn_1	O	SMA J19 and J20	Channel 1 differential high-speed SERDES outputs
hdoutp_2/ hdoutn_2	O	SMA J25 and J26	Channel 2 differential high-speed SERDES outputs
hdoutp_3/ hdoutn_3	O	SMA J27 and J28	Channel 3 differential high-speed SERDES outputs

Loading the LatticeECP3 SERDES Eye Demo Bitstream with ispVM

Follow the instructions below to load the SERDES Eye demo bitstream.

- If ORCAstra is already loaded, make sure **Interface** is set to **None**.
- Start ispVM v.17.4 or higher.
- Click on the **Green Scan** icon (see Figure 4).
- Make sure devices 2 and 3 are in bypass as per Figure 4.
- Make sure device 1 selects LFE3-95_ES or equivalent -95 device on the board.
- Make sure the device 1 bitstream file name points to **<your_project_path>\SERDES\Bit-streams\serdes_eye_demo.bit** and that **Operation** is set to **Fast Program**.
- Click **Go**.
- The bitstream should program successfully

Figure 4. ispVM Setup



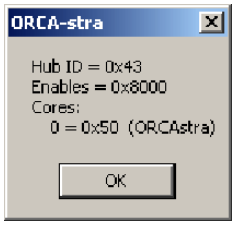
Running a Demo with the ORCAstra PCS View

This section describes the use of the ORCAstra GUI to interactively change/monitor the LatticeECP3 PCS and user register.

Starting ECP3 ORCAstra

Ensure the LatticeECP3 Demo bitstream has been loaded, then:

1. Start ORCAstra version 2.2.34 or later
2. Select **Interface -> 1. ispVM JTAG Hub USB Interface**. If the **Select Target JTAG Device** window comes up, select first device, and click **OK**.
3. You will see the window shown below. Click **OK**.



4. Select **Device -> Lattice ECP3**. Also select **Options** and un-check the check-box mark next to **Display Data in [7:0] Order in Data Box**.

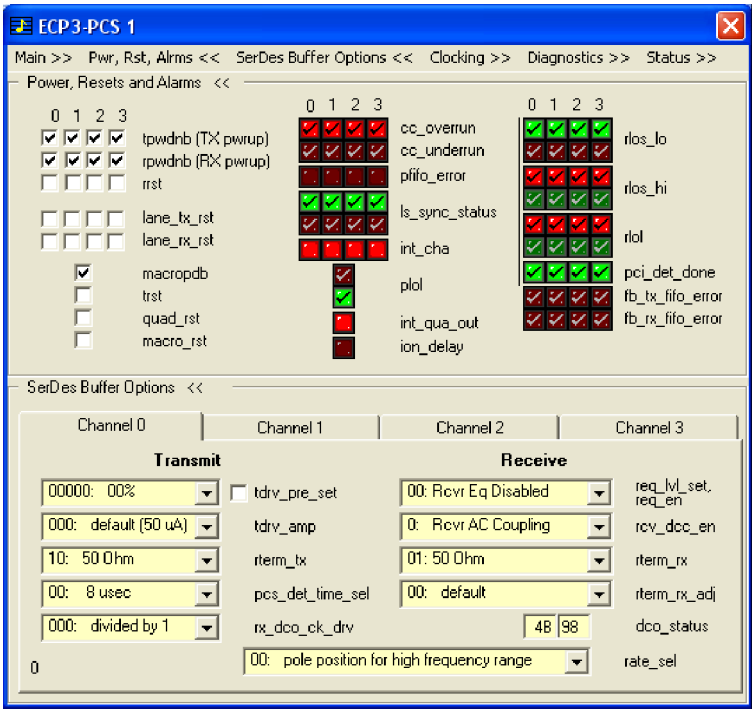
5. Click on the **ECP3 PCS1** option. You will get the ECP3-PCS1 Visual Window. Close the Main tab, and open the **Pwr, Rst, Alrms**, and **SerDes Buffer Options** tab. The resulting window is shown in Figure 5.

6. From the main ORCAstra Visual Window, select **CustomProgrammability-> Visual Window**.

7. In the new window, select **File->Open-> <your_project_path>SERDES\ORCAstra Plug-ins\Eyedemo.vis**. You will see the PRBS Gen./Check Visual Window shown in Figure 2.

8. Make sure **Continuous Polling** is checked in the main ORCAstra window. The resulting GUIs are shown in Figure 5. for the ECP3-PCS1 Visual Window and in Figure 2 for the PRBS Generator/Checker Quad ORCAstra Plug-in Visual Window.

Figure 5. Lattice PCS ORCAstra View



Configuring PCS 1 Options in ORCAstra

Power, Reset and Alarms

The default Pwr, Resets and Alarms section contains the following important information:

- Green/red LEDs (one for whole quad) to indicate that the SERDES transmit PLL (plol) is locking. Green indicates a successful lock.
- Green/red LEDs (one per channel) to indicate Receive CDR lock (rlol). Green indicates a successful lock.

This view also allows the user to identify which channels (or the entire QUAD), are powered down or reset. This view also allows users to reset PCS digital logic (lane_tx_rst and lane_rx_rst), as well as SERDES logic (macro_rst) and the whole QUAD (quad_rst).

SerDes Buffer Options View

This view allows controlling the characteristics of output, input, and reference clock buffers: TX pre-emphasis, TX amplitude, RX equalization, TX and RX buffer termination and coupling.

Typical Backplane Demo Applications

As mentioned earlier, the serial data stream can be:

- Looped back via a cable on the evaluation board, or
- Sent to a DCA or DSO for eye viewing.

The SERDES outputs can be sent to either a DCA (requires external trigger input) or a DSO for eye viewing.

The following sections describe both applications.

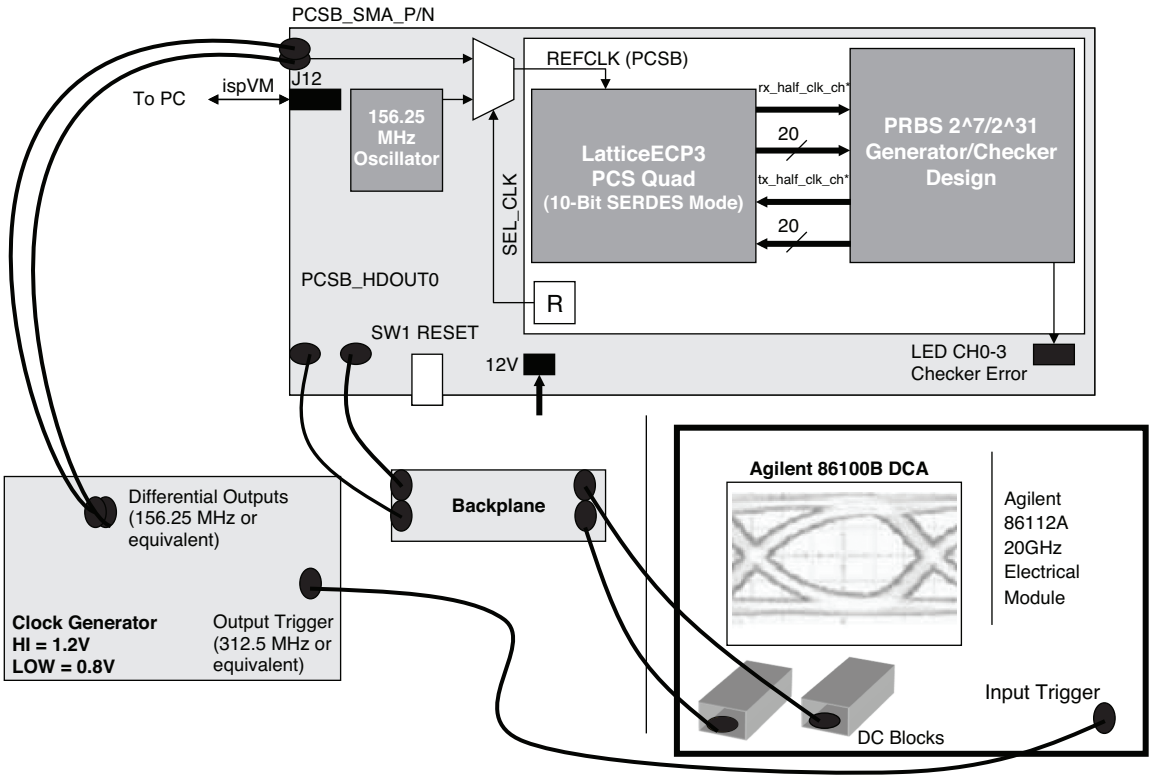
SERDES Eye/Backplane Demo

As mentioned earlier, an eye demo can be performed with either a DSO or DCA instrument. DCA instruments provide a much higher degree of precision eye viewing than DSO instruments. DCA instruments require an external trigger.

DCA Eye Demo

A typical DCA SERDES Eye/Backplane Demo application is illustrated in Figure 6.

Figure 6. Typical DCA SERDES Backplane Eye Demo on PCS Quad PCSB



The setup is as follows:

- External clock generator applies differential clock inputs to PCSB_SMA_P/N (J29 and J33).
- The external clock frequency is 156.25 MHz (or equivalent).
- The external clock levels (per terminal) are VHI=1.2V, VLO=0.8V.
- The external clock generator applies an output trigger to the DCA input trigger.
- Channel 0's high-speed outputs (J17 and J18) are connected via high-speed SMA cables to SMA terminals on the backplane.

- The other terminals on the backplane are connected to DC blocks (directly connected to the DCA input terminals) via high-speed SMA cables.
- The Agilent 86100B instrument setup file is available under <your_project_path>SERDES\DCA_86100B.set

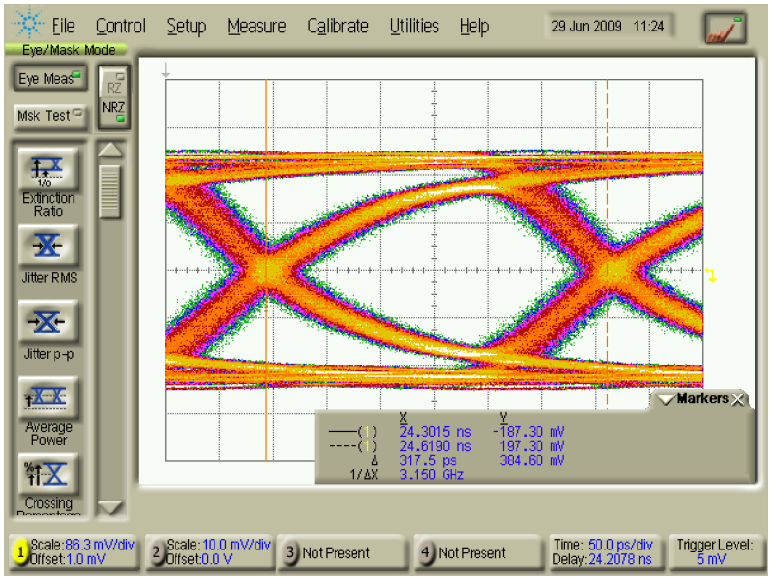
The following steps describe the demo sequence:

1. Make sure power is supplied to the board.
2. Load the LatticeECP3 SERDES Eye/Backplane Demo bitstream.
3. Make sure the external clock generator's outputs are toggling.
4. Start an ORCAstra session and load the LatticeECP3 PCS1 visual basic window and the PRBS Generator/Checker ORCAstra Plug-in Visual Window as previously described.
5. Make sure the Continuous Polling box is checked in the main window.
6. In the Power, Resets, and Alarms tab of LatticeECP3 PCS1 visual basic window, power down channels 1,2 and 3 (uncheck tpwdnb and rpwdnb for channels 1, 2 and 3)
7. In the PRBS visual window (see Figure 2) set the reference clock source to external.
8. In the PRBS visual window, select 2^7 or 2^31 for the PRBS pattern. If you select 2^31, then also set Receive equalization to "11: Long-Reach Eq" in the SERDES Buffer Option tab, ch0, of the LatticeECP3 PCS1 Visual Basic window.
9. In the PRBS visual window, make sure CH0 is enabled.

At this point, a PRBS eye should appear on the DCA screen. As a reference point, Figure 7 illustrates a 3.125 Gbps differential eye obtained after the above steps were performed (2^7 PRBS mode) with the SERDES output SMAS (J17 and J18) connected directly to the DC blocks (no backplane). The default SERDES buffer settings of Figure 5 were used for this measurement.

In a typical backplane application, the SERDES Buffer Options View of PCS1 in ORCAstra (Figure 5) allows real-time modification of output buffer characteristics, as different backplane lengths are utilized to maintain a clean SERDES eye diagram at the DCA input. Changes to the eye of Figure 7 can be observed once any of the TX buffer options (amplitude, pre-emphasis, coupling) are changed.

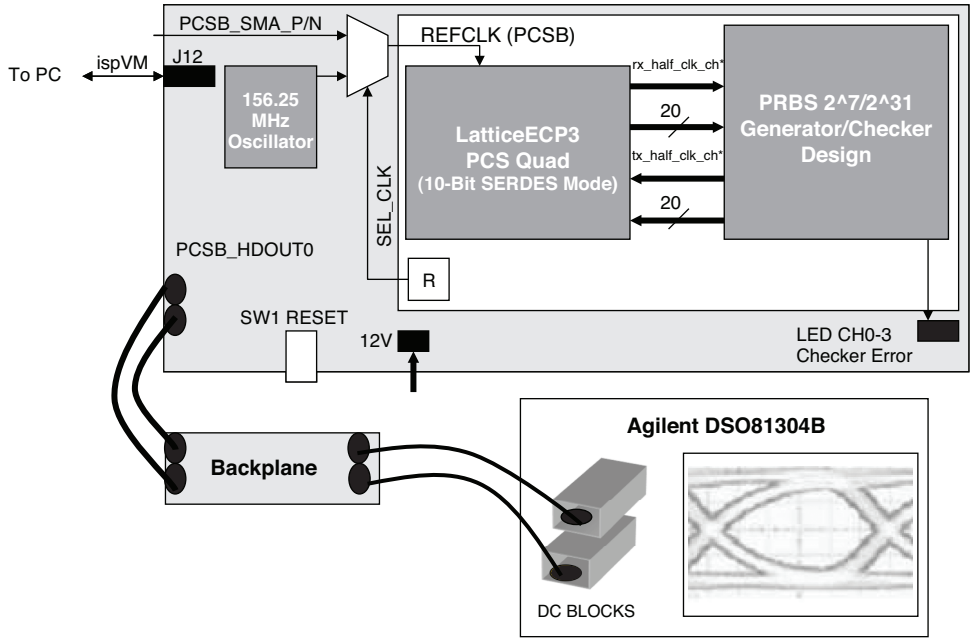
Figure 7. DCA Differential 2^7 PRBS Eye Diagram with PCS Quad PCSB and No Backplane



DSO Eye Demo with PCS quad PCSB

A typical DSO SERDES Eye/Backplane Demo application with PCS PCSB is illustrated in Figure 8.

Figure 8. Typical DSO SERDES Backplane Eye Demo on PCS Quad PCSB



The setup is as follows:

- On-board 156.25 MHz Y1 oscillator applies differential clock inputs to PCSB reference clock input.
- Channel 0's high speed outputs (J17 and J18) are connected via high-speed SMA cables to SMA terminals on the backplane.
- If possible, the other terminals on the backplane are connected to DC blocks (directly connected to DSO Ch1 and Ch2) via high-speed SMA cables.
- The Agilent DSO81304B instrument setup file is available under <your_project_path>SERDES\Misc\ DSO81394B_setup.set

If the DSO is replaced with a DCA instrument, then either SMA J17 or J18 can be used as the trigger to the DCA trigger input.

The following steps describe the demo sequence:

1. Make sure power is supplied to the board.
2. Load the LatticeECP3 SERDES Eye/Backplane Demo bitstream.
3. Start an ORCAstra session and load the LatticeECP3 PCS1 visual basic window and the PRBS Generator/Checker ORCAstra Plug-in Visual Window as previously described.
4. Make sure the Continuous Polling box is checked in the main window.
5. In the Power, Resets, and Alarms tab of LatticeECP3 PCS1 visual basic window, power down channels 1, 2 and 3 (uncheck tpwdnb and rpwdnb for channels 1, 2 and 3)
6. In the PRBS visual window (see Figure 2) set the reference clock source to on-board oscillator.

7. In the PRBS visual window, select 2^7 or 2^31 for the PRBS pattern. If you select 2^31, then also set Receive equalization to “11: Long-Reach Eq” in the SERDES Buffer Option tab, ch0, of the LatticeECP3 PCS1 visual basic window.

8. In the PRBS visual window, make sure CH0 is enabled.

At this point, a PRBS eye should appear on the DSO screen. As a reference point, Figure 9 illustrates a 3.125 Gbps differential eye obtained after the above steps were performed (2^7 PRBS mode) with the SERDES output SMAS (J17 and J18) connected directly to the DC blocks (no backplane). The default SERDES buffer settings of Figure 5 were used for this measurement.

In a typical backplane application, the SERDES Buffer Options View of PCS1 in ORCAstra (Figure 5) allows real-time tweaking of output buffer characteristics, as different backplane lengths are utilized to maintain a clean SERDES Eye Diagram at the DSO input. Changes to the eye of Figure 9 can be appreciated if any of the TX buffer options (amplitude, pre-emphasis, coupling) are changed.

Figure 9. DSO Differential Eye Diagram with PCS Quad PCSB and No Backplane

PRBS Loopback Demo

In a typical PRBS backplane loopback application:

- The FPGA PRBS Generator is used to transmit data from the FPGA to the PCS TXD ports on a given channel.
- The PCS SERDES HDOUT pins are connected to a backplane through SMA cables.
- The other backplane terminals connect to the PCS HDIN channel inputs through SMA cables.
- The PCS RXD ports then feed the recovered data to the FPGA PRBS Quad Checker.

This type of application is illustrated in Figure 3. This setup applies to PCSB.

This application can make use of the PRBS Generator/Checker Quad ORCAstra Plug-in Visual Window from Figure 2 and the SerDes Buffer Options ORCAstra View (see Figure 5). While looping PRBS data on any given channel the first window is used to verify error-free PRBS data is received, while the second window is used to tweak output and input buffer options (as different backplane lengths are used).

The following steps describe how to run through a PRBS loopback demo on channel 0.The assumption is that the HDIN and HDOUT SMA (P, N) pairs are (J13, J14) and (J17, J18) respectively.

1. Make sure power is supplied to the evaluation board.
2. Make sure HDOUT* are looped back to HDIN*.
3. Load the LatticeECP3 SERDES Demo bitstream as previously described.
4. Start an ORCAstra session and load the LatticeECP3 PCS1 visual basic window and the PRBS Generator/Checker ORCAstra Plug-in Visual Window as previously described.
5. Make sure the Continuous Polling box is checked in the main window.
6. In the Power, Resets, and Alarms tab of LatticeECP3 PCS1 visual basic window, power down channels 1, 2 and 3 (uncheck tpwdnb and rpwdnb for channels 1, 2 and 3).
7. In the PRBS Generator/Checker Quad Visual Window:
    A. Select the on-board oscillator or an external clock source on PCSB_SMA_P/N.
    B. Select 2^7 or 2^31 for PATTERN. If you select 2^31, then also set Receive equalization to "11: Long-Reach Eq" in the SERDES Buffer Option tab, ch0, of the LatticeECP3 PCS1 visual basic window.
    C. Clear all counters by pressing the Clear Error Cntrs button.
    D. ENABLE channel 0. The generator and checker for channel 0 are now transmitting and checking PRBS packets. After this step, rlol should be solid green. Also verify that plol is solid green. If any of these indicators are red, then proceed to debugging these indicators as indicated in step 7E.
    E. If the ERR COUNTER for channel 0 increments and/or the D21 error LED lights up, then the PRBS checker is receiving patterns with errors. Note that the error counters will not rollover after reaching hFF. So it is necessary to reset the counter to ensure no new errors are received.
        a. Verify that the Power, Reset and Alarm section of PCS 1 View does not show any PLL loss of lock (plol) or CDR loss of lock (rlol),
        b. A red plol indicates that the reference clock source to the TX PLL is not stable or may have the incorrect frequency.
        c. A red rlol indicates incorrect activity on the HDIN* inputs. The input signals may be too attenuated by the medium.
        d. Try modifying some of the input and output buffer settings in the SerDes Buffer Options section of PCS 1 View (TX pre-emphasis, TX amplitude, RX equalization...) to address the rlol issue.

Implementing and Simulating the Reference Design

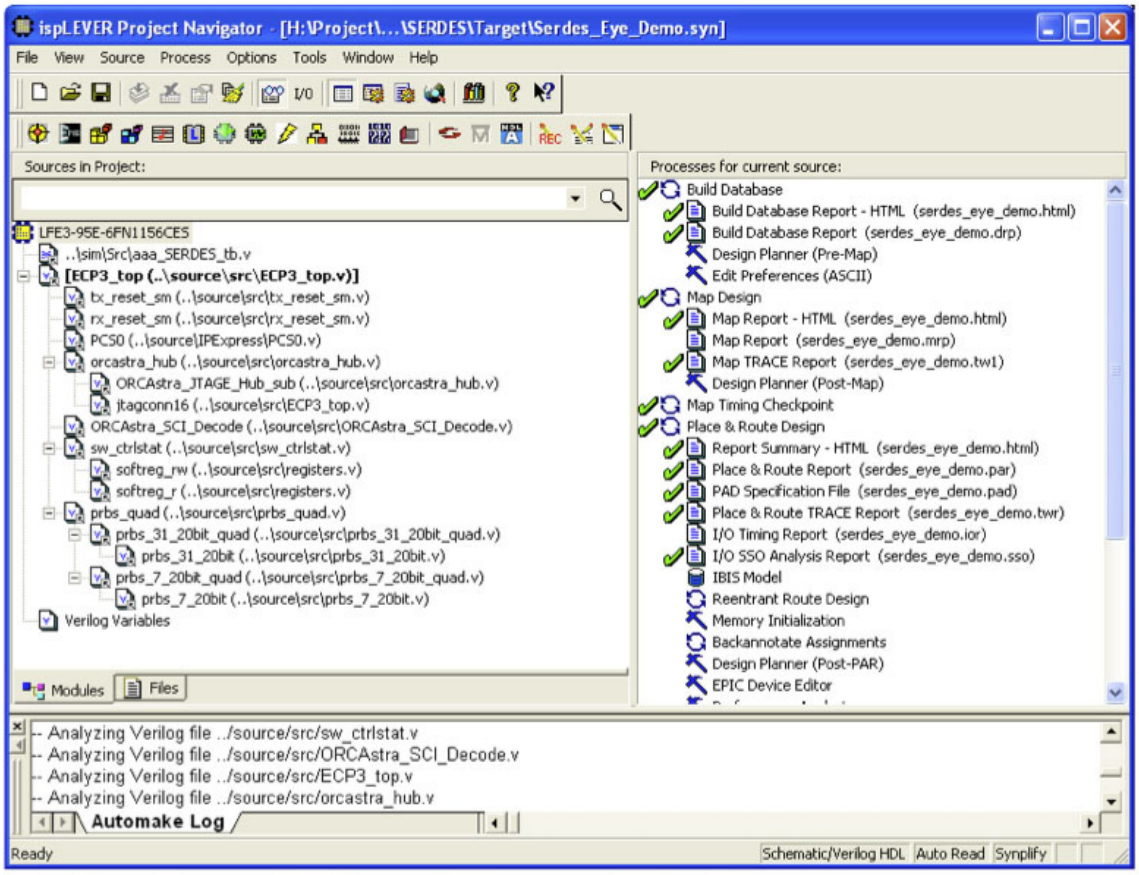
The steps below explain how to run the SERDES Eye/Backplane Demo Reference Design source code through ispLEVER Project Navigator MAP, place and route, bitstream generation, and simulation.

Both implementation and simulation start with the same steps:

1. Start ispLEVER Project Navigator

2. Open **<your_project_path>SERDES\Target\Serdes_Eye_Demo.syn**. This will load the Verilog-based project, as shown in Figure 10.

Figure 10. ispLEVER Project Navigator Verilog HDL Design



Implementation

To implement the design and generate a bitstream, double-click the **Generate Bitstream Data** target in the **Processes** window. This will run through the full synthesis, place and route flow and generate a new serdes_eye_demo.bit file.

Simulation

The simulation process uses the **custom.do** Aldec Active-HDL simulation script located under the **Target** directory. To ensure this script is used, follow the steps below, as illustrated in Figure 11:

1. Select the **aaa_SERDES_tb.v** testbench file in the **Source** window.

2. Select **Verilog Functional Simulation with Aldec Active-HDL** in the **Processes** window, then right-click and select **Properties**.

3. In the **Properties** window, enter **custom.do** for the **Custom Library Do File** entry. Also set **Use Automatic Do File** to **False**. Then click **Close**.

4. Now, double-click the **Verilog Functional Simulation with Aldec Active-HDL** target to start the Aldec-HDL simulation process, which will execute the **custom.do** script. The script compiles all necessary design and testbench files and runs the simulation into the Aldec Waveform window shown in Figure 12.

Figure 11. Configuring Aldec Simulation

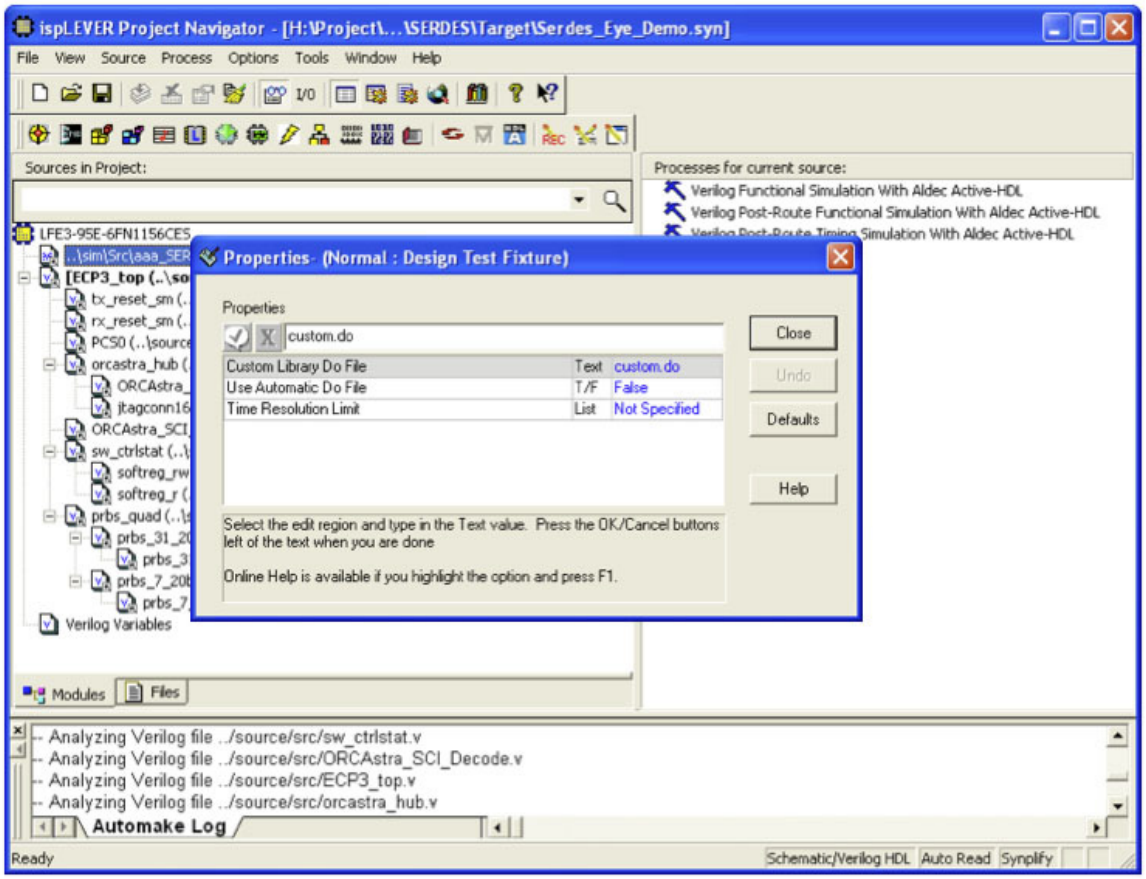
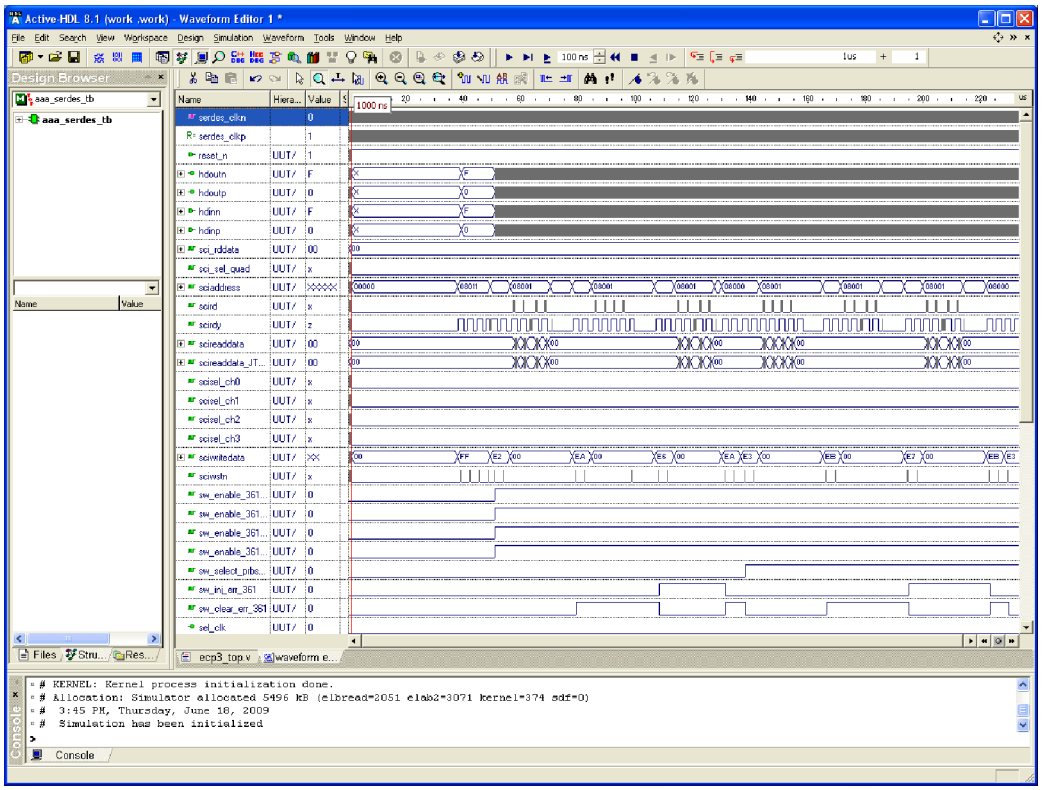


Figure 12. Aldec Active-HDL Simulation



Reference Information

The following documents provide more information:

- TN1176, LatticeECP3 SERDES/PCS Usage Guide.
- EB42, LatticeECP3 Serial Protocol Board – Version C User's Guide

Technical Support Assistance

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Revision History

Date	Version	Change Summary
July 2009	01.0	Initial release.
December 2009	01.1	Updated Typical DSO SERDES Backplane Eye Demo on PCS Quad PCSB figure.
August 2010	01.2	Implemented the LatticeECP3 PCS TX and RX Reset State machines described under the SERDES/PCS RESET section of TN1176.
January 2011	01.3	Added information on seting RX equalization to Long-Reach when running the PRBS 2^31 pattern.
March 2011	01.4	Document title changed to “SERDES Eye/Backplane Demo for the LatticeECP3 Serial Protocol Board”.