Supervisor, WDT and Reset Generation with ProcessorPM

July 2009 Reference Design RD1056

Introduction

The ProcessorPM™ (ispPAC-POWR605) device is shipped from the factory preprogrammed with a design that provides three functions: voltage supervision, watchdog timer, and reset generator. ProcessorPM is provided preprogrammed so that designers can take advantage of a fully functioning Power Manager design similar to that of a factory set off-the-shelf reset or supervisor IC.

This document describes in detail the design that is preprogrammed at the factory. This design is also included in the Examples folder of PAC-Designer® for review or modification by users (file name = POWR605-4-factory-config.pac). While the ProcessorPM comes from the factory preprogrammed it can be reprogrammed with a slight modification to this design or a completely new design just like any other Power Manager device from Lattice Semiconductor Corporation.

ProcessorPM provides six programmable threshold comparators (accuracy +/-0.7%) with individual glitch filters to monitor up to six supply rails. Three comparators are configured for standard power supplies: 3.3V, 2.5V, and 1.8V. The three remaining comparators are configured to 0.699V so they can be configured using external resistor dividers. The comparator outputs are connected to the 16-macrocell, ruggedized on-chip PLD for voltage supervision and reset generation using simple logic equations. The four built-in timers are used to provide input debounce, reset pulse stretching, and watchdog delays. An I/O pin is used to enable or disable a 200ms stretch on the $\overline{\text{Reset\_CPU}}$ output. And two I/O pins are used to digitally select the watchdog timer delay period from 500ms, 2s, 10s, and 1 minute. All device settings are stored using on-chip non-volatile EEPROM that is programmed via a JTAG interface.

Features

- Six supply monitors
  - 3.3V (-5%) supply rail monitor
  - 2.5V (-5%) supply rail monitor
  - 1.8V (-5%) supply rail monitor
  - Three user-selectable voltage monitors
- Watchdog timer with selectable settings of 500ms, 2sec, 10sec, and 1min
- Reset generator with optional 200ms pulse-stretch
- De-bounced manual reset input
- Watchdog timer trigger input

Functional Description

This design has two output functions: reset generation and watchdog timer. The behavior of these two outputs is controlled by the condition of the six VMON inputs, two input pins, and the status of three configuration pins.

The reset generation output pin ($\overline{\text{Reset\_CPU}}$) is active low and is held low when any of the VMON inputs is below the respective trip point threshold or when the input Manual_reset is held low. Each of the voltage monitoring inputs is filtered with a 48-microsecond glitch filter. The $\overline{\text{Reset\_CPU}}$ output will go high after the last VMON input is above its respective trip point and the Manual_reset input is high. If the Stretch_200ms input is low, the $\overline{\text{Reset\_CPU}}$ output will go high with no delay but, if the Stretch_200ms input is high, then the $\overline{\text{Reset\_CPU}}$ output will go high after a 200ms delay. The pin Manual_reset is an active low input that is de-bounced by a 50ms timer circuit. The minimum pulse width of the Manual_reset input is 10us.

The watchdog output pin ($\overline{\text{WDT\_Int}}$) is active low that pulses low when the watchdog timer delay expires. The two input pins WDT_Sel1 and WDT_Sel0 signals are used to select the Watchdog timer delay as listed in Table 1. The watchdog timers are reset by the falling edge of the WDT_Trig input. The minimum pulse width of the WDT_Trig input is 10 microseconds. When the delay between successive WDT_Trig falling edge signals exceeds the watchdog timer delay setting, a low-going pulse is generated on the $\overline{\text{WDT\_Int}}$ output. After generating the output pulse, the watchdog timer is restarted. It continues to generate low-going pulses regularly at watchdog delay set intervals until a falling edge of WDT_Trig signal is received. The watchdog timers are held in reset when the $\overline{\text{Reset\_CPU}}$ output is active and released when the $\overline{\text{Reset\_CPU}}$ output goes high.

Table 1. Programmable Watchdog Timer Delay Selection

WDT_Sel1	WDT_Sel0	Watchdog Timer Delay (Typ.)
0	0	500 ms
0	1	2 sec.
1	0	10 sec.
1	1	1 min.

Table 2. Pin Description

Pin	Function	Name	Type	Description
1	VMON1	Main_3V3_OK	Analog Input	Voltage monitor of 3.3V supply
2	VMON2[1]	IO_2V5_OK	Analog Input	Voltage monitor of 2.5V supply
3	VCC	VCC	Power	Power supply
4	VMON3[1]	IO_1V8_OK	Analog Input	Voltage monitor of 1.8V supply
5	VMON4[1]	Prog1_OK	Analog Input	Voltage monitor of programmable supply
6	VMON5[1]	Prog2_OK	Analog Input	Voltage monitor of programmable supply
7	VMON6[1]	Prog3_OK	Analog Input	Voltage monitor of programmable supply
8	GND	Ground	Ground	Ground
9	GND	Ground	Ground	Ground
10	VCCJ	VCCJ	Power	VCC for JTAG logic interface pins
11	TDO	TDO	Output	JTAG test data out
12	TCK	TCK	Input	JTAG test clock
13	TDI	TDI	Input	JTAG test data in
14	TMS	TMS	Input	JTAG test mode select
15	IN_OUT5	WDT_Sel1	Input	Watchdog timer delay select MSB
16	VCC	VCC	Power	Power supply
17	IN_OUT4	WDT_Sel0	Input	Watchdog timer delay select LSB
18	IN_OUT3	Stretch_200ms	Input	$\overline{\text{Reset\_CPU}}$ pulse stretch: Low=none, High=200ms
19	IN_OUT2	$\overline{\text{WDT\_Int}}$	Output	Watchdog timer interrupt, active low.
20	IN_OUT1	$\overline{\text{Reset\_CPU}}$	Output	Reset generator output, active low.
21	IN2	WDT_Trig	Input	Watchdog timer trigger, negative edge resets WDT.
22	IN1_PWRDN	Manual_reset	Input	Reset generator input, active low.
23	NC	NC	N/A	No connection
24	NC	NC	N/A	No connection
25	Die Pad	NC	N/A	No connection

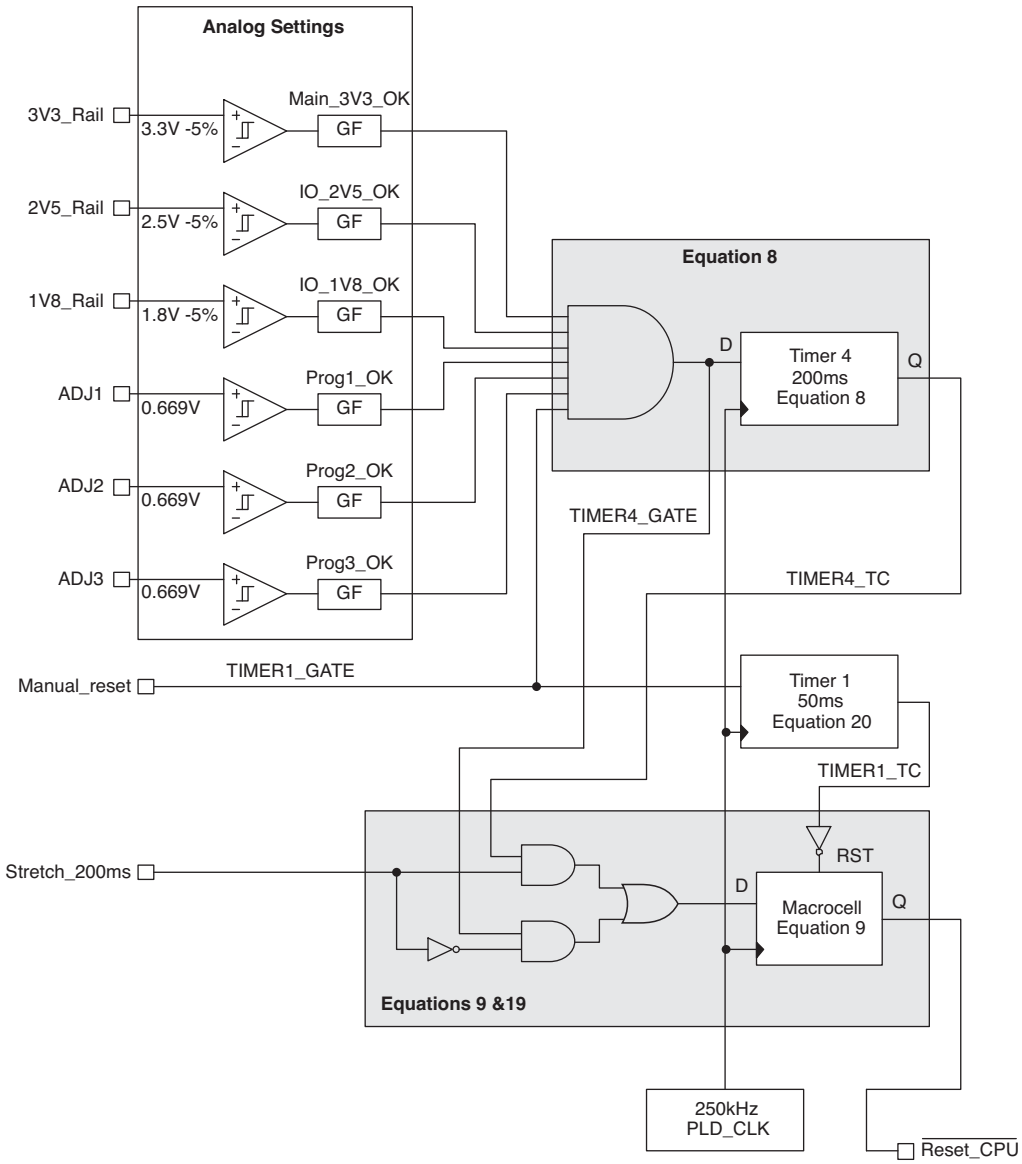
1. Connect unused VMON inputs to VMON1.

Design Description

In order to fit all the functionality of this design into 13 macrocells, the design is realized using Supervisory Logic Equations in PAC-Designer software. This section describes the function and interaction of these equations using block diagrams combined with listings of the 20 Supervisory Logic Equations. First we will discuss the Reset Generator function and then the Watchdog Timer function.

In Figure 1, the reset generator function is represented with four key blocks. The Analog Settings block translates the power supply voltage levels into a logic true for good voltage conditions and false for under voltage conditions. The Glitch Filter (GF) ensures that voltage transients that are less than 48us are blocked from the logic. All of the VMON outputs are ANDed together with the Manual_reset input in Equation 8 to provide the gate signal for Timer 4. When the gate signal of a timer is low, the timer is reset and its output is also low. When the timer gate signal is high, the timer is allowed to run and after the time-out period the Terminal Count output (TC) goes high. Timer 4 is set for 200ms to support the pulse stretch option.

Figure 1. Six-Supply Reset Generator Block Diagram



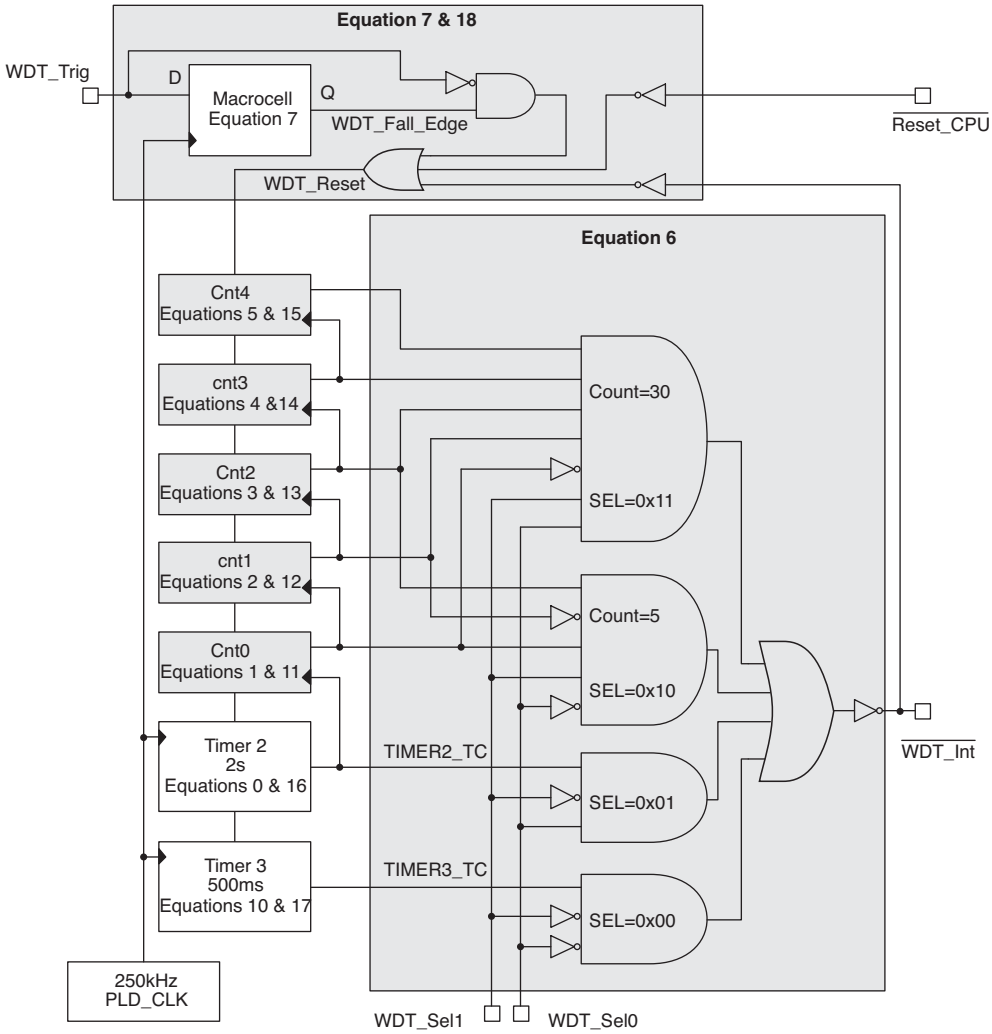
Equation 9 decodes the state of the input Stretch_200ms and combines the status of either the gate or the terminal count condition to drive the $\overline{\text{Reset\_CPU}}$ output. Equation 20 defines the gate of Timer 1 which is used to de-bounce the Manual_reset input. Equation 19 provides the asynchronous reset to the $\overline{\text{Reset\_CPU}}$ output macrocell so the output will go low as soon as Manual_reset is asserted and will stay low as long as Manual_reset is asserted. $\overline{\text{Reset\_CPU}}$ will stay low for at least 50ms after Manual_reset is de-asserted and stable. The 250kHz PLD clock drives the 200ms and 50ms timers and the $\overline{\text{Reset\_CPU}}$ macrocell. Listing 1 contains the equations that make up the Reset Generator Function.

Listing 1. Reset Generator Equations

```
EQ 8  TIMER4_GATE.D = Main_3V3_OK AND IO_2V5_OK AND IO_1V8_OK AND
                      Prog1_OK AND Prog2_OK AND Prog3_OK AND Manual_reset
EQ 9  Reset_CPU.D   = Stretch_200ms AND TIMER4_TC OR
                      NOT Stretch_200ms AND TIMER4_GATE
    .
    . {equations 10 - 18 are used for the watchdog function: see Listing 2}
    .

EQ 19 Reset_CPU.ar  = NOT TIMER1_TC
EQ 20 TIMER1_GATE.D = Manual_reset
```

Figure 2. Selectable Watchdog Timer Block Diagram



In Figure 2 the Watchdog Timer function is represented by two large blocks and several smaller ones. The largest block is Equation 6 that decodes the WDT_Sel1 and WDT_Sel0 inputs and combines the appropriate timer terminal count or counter combination to drive the $\overline{\text{WDT\_Int}}$ output. Equation 7 synchronizes the WDT_Trig input to the internal PLD clock and Equation 18 detects the falling edge to reset the timers and counters. Equation 18 also OR's the $\overline{\text{Reset\_CPU}}$ output and $\overline{\text{WDT\_Int}}$ output to drive the internal node WDT_Reset. Equations 1- 5 define a five-bit binary counter that counts the number of times the 2 second timer has expired. Equations 11-15 provide the asynchronous reset to the binary counter from the internal WDT_Reset node. Equation 0 allows the 2-second timer to self-run, providing the binary counter a time base and Equation 16 provides the asynchronous reset for timer 2. Equation 10 allows the 500ms timer to run regardless of the state of WDT_Trig input and Equation 17 provides the asynchronous reset for timer 3. The watchdog timer equations are shown in Listing 2 and further details of timers 2 and 3 are provided in Figure 3. Table 3 lists the critical timing specifications for the entire design.

Listing 2. Watchdog Timer Equations

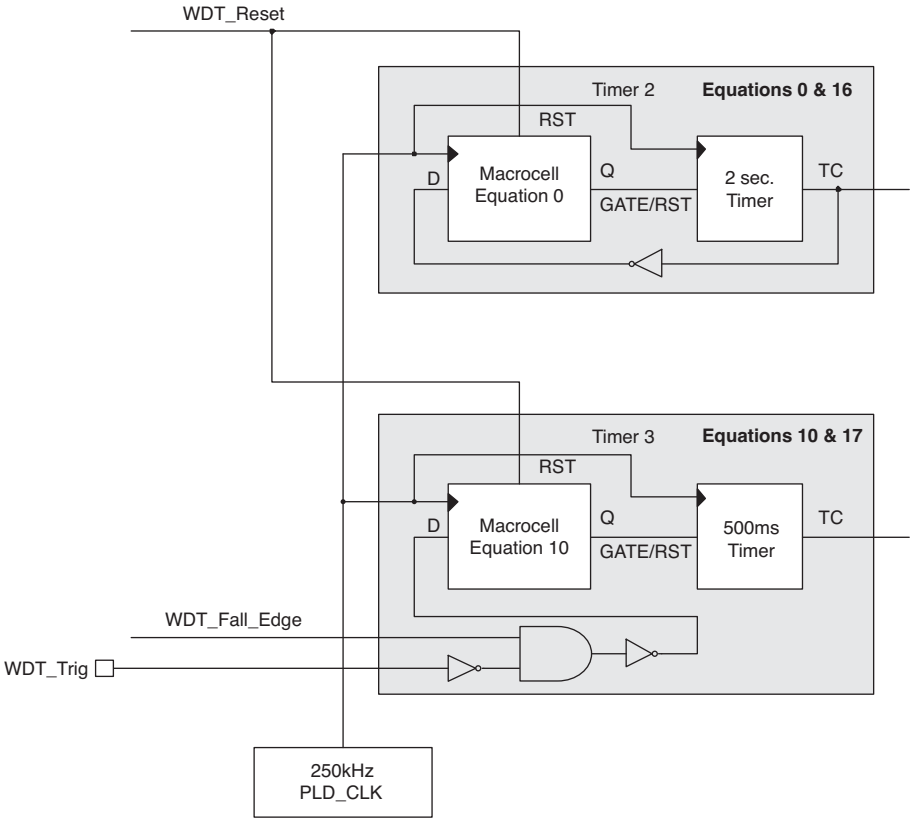
```
EQ  0  TIMER2_GATE.D    =  NOT TIMER2_TC
EQ  1  Cnt0.D           =  Cnt0 AND NOT TIMER2_TC OR NOT Ctr0 AND TIMER2_TC
EQ  2  cnt1.D           =  ( NOT cnt1 AND Cnt0 AND TIMER2_TC ) OR
                           ( cnt1 AND NOT ( Cnt0 AND TIMER2_TC ) )
EQ  3  Cnt2.D           =  ( NOT Cnt2 AND cnt1 AND Cnt0 AND TIMER2_TC ) OR
                           ( Cnt2 AND NOT ( cnt1 AND Cnt0 AND TIMER2_TC ) )
EQ  4  cnt3.D           =  ( NOT cnt3 AND Cnt2 AND cnt1 AND Cnt0 AND TIMER2_TC ) OR
                           ( cnt3 AND NOT ( Cnt2 AND cnt1 AND Cnt0 AND TIMER2_TC ) )
EQ  5  Cnt4.D           =  ( NOT Cnt4 AND cnt3 AND Cnt2 AND cnt1 AND Cnt0 AND TIMER2_TC ) OR
                           ( Cnt4 AND NOT ( cnt3 AND Cnt2 AND cnt1 AND Cnt0 AND TIMER2_TC ) )
EQ  6  WDT_Int.D        =  NOT ( ( NOT WDT_Sel0 AND NOT WDT_Sel1 AND TIMER3_TC ) OR
                           ( NOT WDT_Sel1 AND WDT_Sel0 AND TIMER2_TC ) OR
                           ( WDT_Sel1 AND NOT WDT_Sel0 AND Cnt2 AND NOT cnt1 AND Cnt0 ) OR
                           ( WDT_Sel0 AND WDT_Sel1 AND Cnt4 AND cnt3 AND Cnt2 AND cnt1 AND NOT Cnt0 ) )
EQ  7  WDT_Fall_Edge.D =  WDT_Trig
    .
    . {equations 8 & 9 are used for reset generation: see Listing 1}
    .

EQ 10  TIMER3_GATE.D = NOT ( NOT WDT_Trig AND WDT_Fall_Edge )
EQ 11  Cnt0.ar = WDT_Reset
EQ 12  cnt1.ar = WDT_Reset
EQ 13  Cnt2.ar = WDT_Reset
EQ 14  cnt3.ar = WDT_Reset
EQ 15  Cnt4.ar = WDT_Reset
EQ 16  TIMER2_GATE.ar = WDT_Reset
EQ 17  TIMER3_GATE.ar = WDT_Reset
EQ 18  WDT_Reset.D = ( NOT WDT_Trig AND WDT_Fall_Edge ) OR
                     NOT WDT_Int OR NOT Reset_CPU
```

Table 3. Timing Specifications

Description	Min.	Typ.	Max.	Units
Manual_reset pulse width	10	—	—	us
WDT_Trig pulse width	10	—	—	us
$\overline{\text{WDT\_Int}}$ pulse width	3.8	6	8.4	us
Manual_reset debounce	42.6	49.2	51.7	ms
$\overline{\text{Reset\_CPU}}$ pulse stretch	186.0	213.0	223.7	ms
500ms Watchdog timer delay	432.5	524.3	550.5	ms
2 sec. Watchdog timer delay	1.737	1.966	2.064	seconds
10 sec. Watchdog timer delay	8.68	9.83	10.32	seconds
1 min. Watchdog timer delay	52.1	58.98	61.9	seconds

Figure 3. Timer 2 & 3 Block Diagram



Simulation and Verification

Because the simulator that is included in PAC-Designer is a functional simulator and it produces a result for every PLD clock transition, this design is simulated with reduced timer values as listed in Table 4. By using a timer value that is roughly 1000 times shorter, the simulation time, data file size, and redraw time are all optimized. Also, using a factor of 1000 results in a more straightforward interpretation of the simulation results (1000us = 1ms). One must be sure to reset the timers back to the design value before generating a JEDEC file or programming the device.

Table 4. Timing Specifications

Timer (ms)	Design Value	Simulation Value
Timer 1	49.15	0.048
Timer 2	1966.08	1.92
Timer 3	524.29	0.512
Timer 4	212.99	0.208

Hardware verification of this design is available using the ProcessorPM Evaluation Board (order part number PACPOWR605-P-EVN) as shown in Figure 4. One key difference in the design programmed into the evaluation board and the design that is described in this document is the $\overline{\text{WDT\_Int}}$ output is active high and not active low. This is to support a pulse stretching circuit on the evaluation board to drive an LED. The evaluation board design file is also located in the PAC-Designer Examples folder and is named POWR605-5-Evaluation_Board.pac.

Figure 4. ProcessorPM Evaluation Board

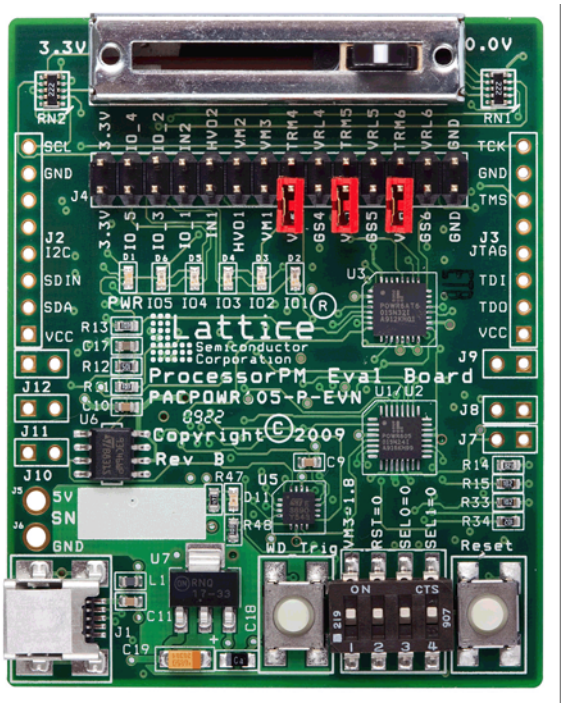


Figure 5. Simulation of De-Bounce

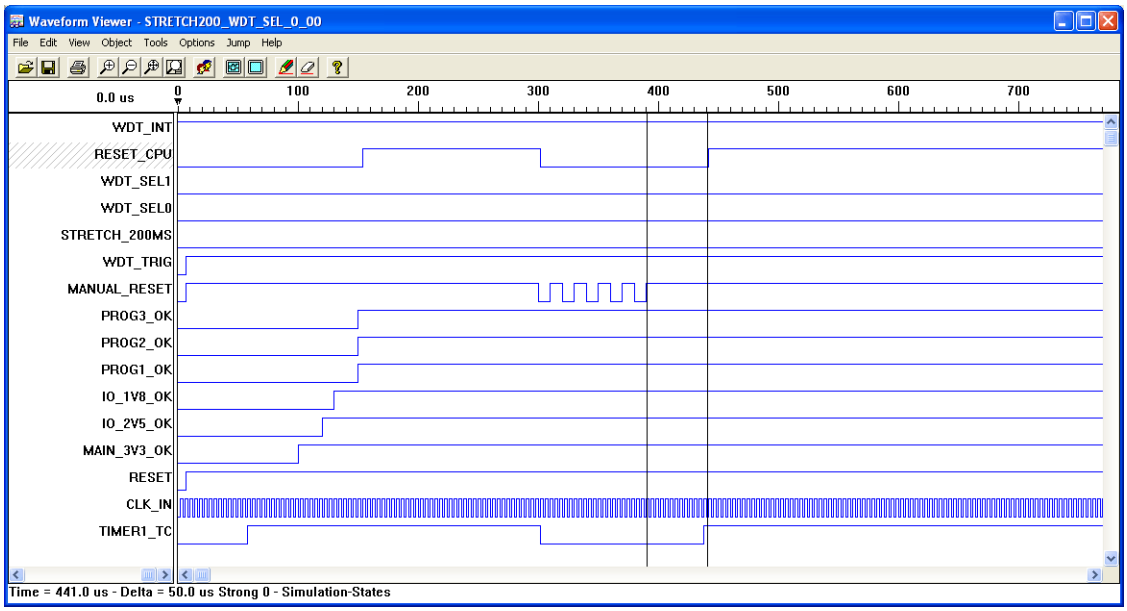


Figure 6. Simulation of Pulse Stretch and 500ms Watchdog

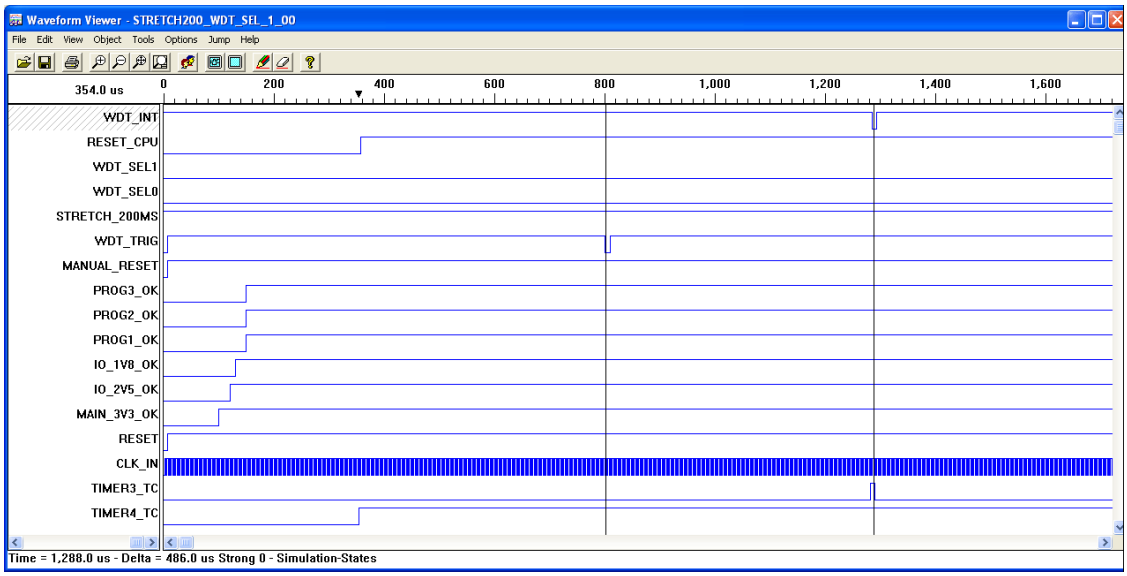


Figure 7. Simulation of Pulse Stretch and 2s Watchdog

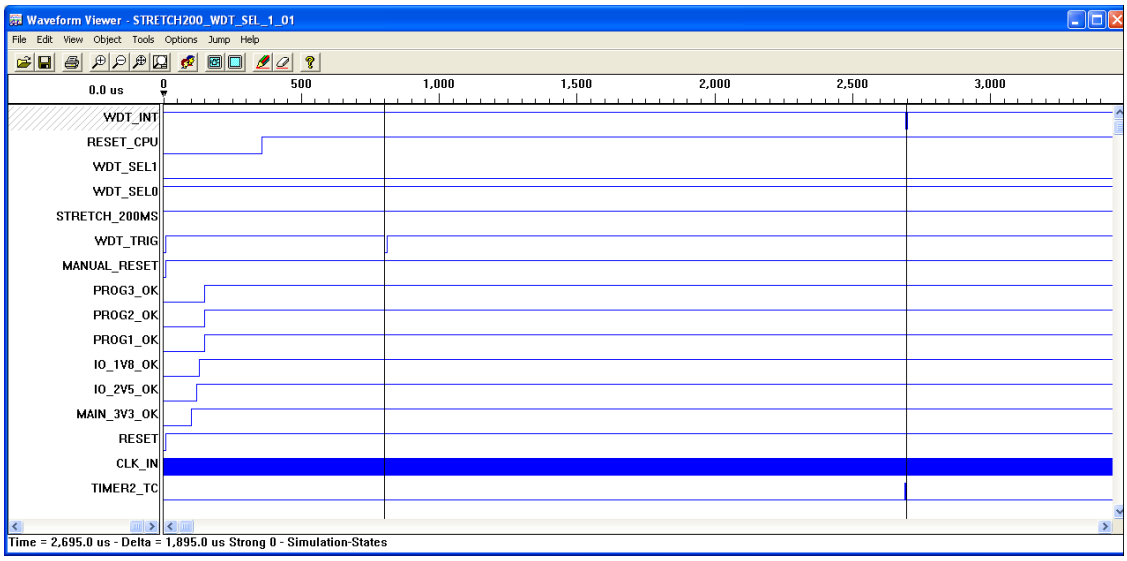


Figure 8. Simulation of Pulse Stretch and 10s Watchdog

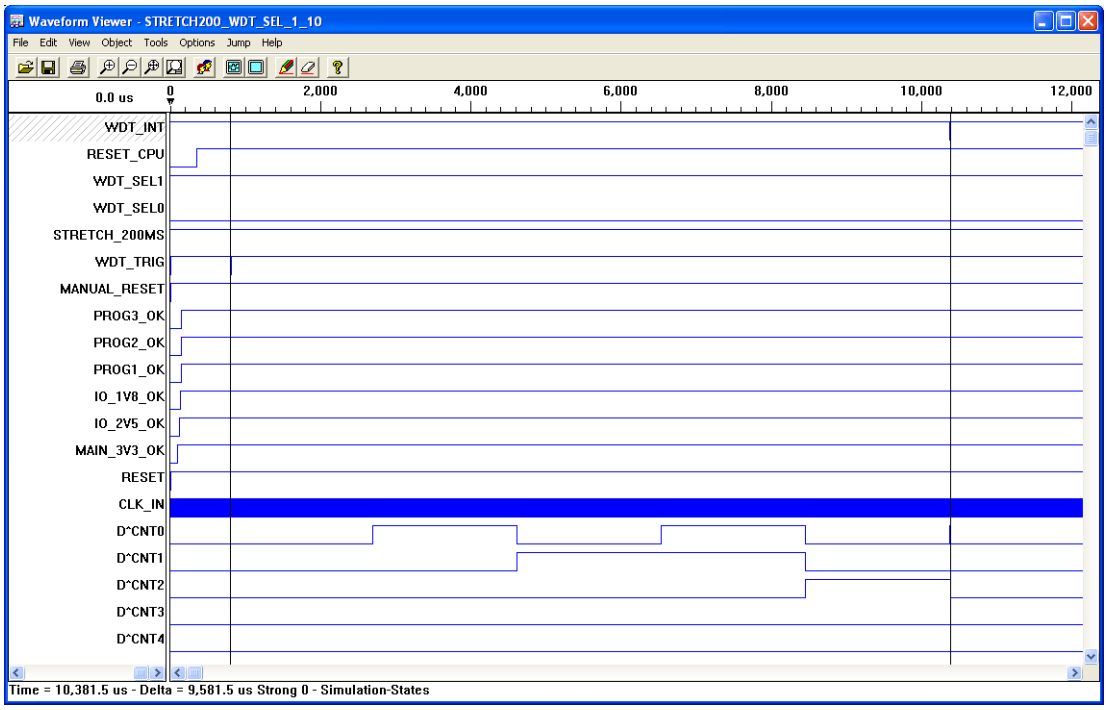
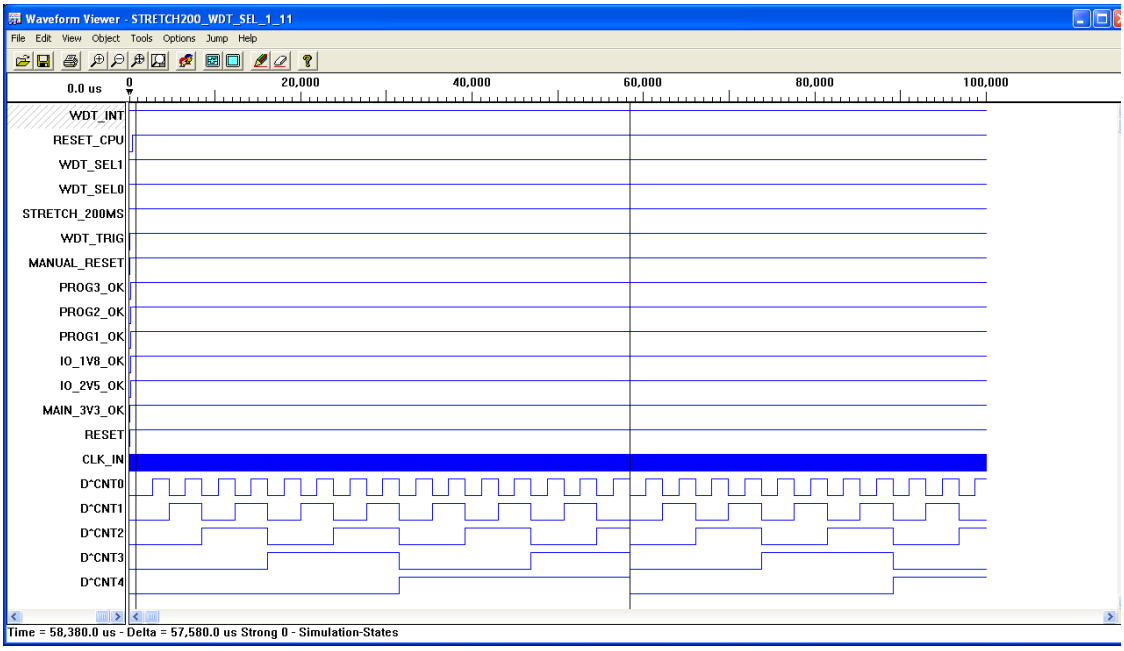


Figure 9. Simulation of Pulse Stretch and 60s Watchdog



Implementation

Table 5. Performance and Resource Utilization[1]

Device Family	Macrocells	Product Terms	VMONs	I/Os	Timers
ProcessorPM-POWR605	13	52	6	7	4

1. Resource utilization characteristics are generated using PAC-Designer 5.1 software. When using this design in a different device, utilization characteristics may vary.

References

- ProcessorPM-POWR605 Data Sheet
- ProcessorPM Development Kit User's Guide
- AN6076 – Optimizing the Accuracy of ispPAC Power Manager Timers

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
July 2009	01.0	Initial release.