NAND Flash Controller

Reference Design

FPGA-RD-02095-1.3

December 2019

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1. Introduction

Flash memory, whether it is in NOR or NAND in structure, is a non-volatile memory that is used to replace traditional EEPROM and hard disks for its low cost and versatility. Because of the difference in the structure of interconnection of the memory cells, NOR Flash is known for its random access capability, while the NAND Flash is known for its compact size. This is especially important in applications where the highest-density memory is offered in the smallest footprint.

This design provides a controller that targets the NAND Flash memory. In general, NAND Flash must be accessed one page at a time, erase must be done on a per-block basis, and NAND Flash must be written sequentially. However, these limitations are often overlooked when designers are looking for the highest memory density available at the lowest possible cost. This is why NAND Flash is widely accepted for non-volatile data storage applications.

2. Features and Limitations

This reference design is targeted at the Samsung K9F1G08R0A NAND Flash. It supports the reset, read ID, block erase, page program and page read commands. The read status command is supported for the program and erase operations. The other commands are not implemented in this design. This design implements a simple host interface which gives the designer the flexibility to modify this interface to meet the requirements of their host interface system.

3. Functional Description

This reference design is used to interface a NAND Flash device and provides a simple host end interface. The host end interface of this design is user-configurable. It provides buffer select signal, buffer write enable signal, address bus, data bus, error status signal, control and handshake signals for the user.

The NAND Flash used for testing this reference design is the Samsung NAND Flash K9F1G08R0A. Samsung K9F1G08R0A is a 128Mx8-bit NAND Flash memory device. The command, data and address are multiplexed through an 8-bit I/O port. The I/O data are latched on the rising edge of WE_n when CE is low. The address is latched in when ALE is high and CLE is low, and the command is latched when ALE is low and CLE is high. When a read operation is implemented, the data are output on the rising edge of RE_n when CE is low. Figure 3.1. shows the interface of this reference design and all the interface signals are listed in Table 3.1. The design meets the NAND Flash access timing as required in the NAND Flash data sheet Figure 3.2. shows the I/O data latch cycle, Figure 3.3. shows the address latch cycle, and Figure 3.4. shows the command latch cycle.

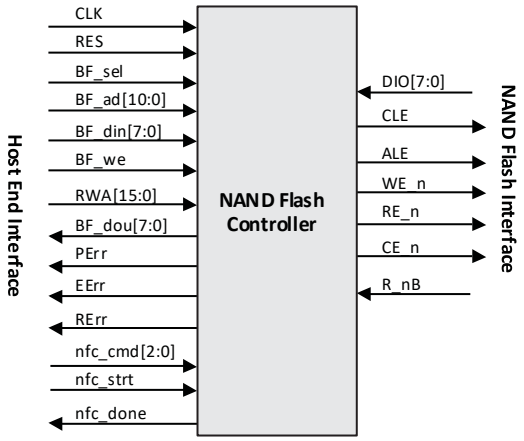

Figure 3.1. NAND Flash Interface

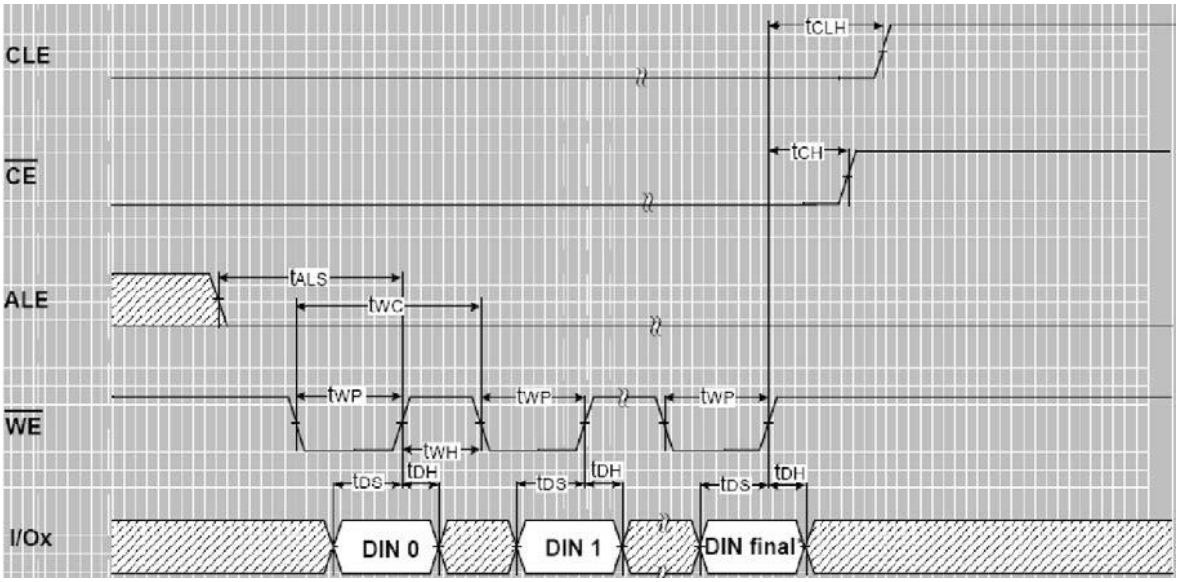

Figure 3.2. I/O Latch Cycle

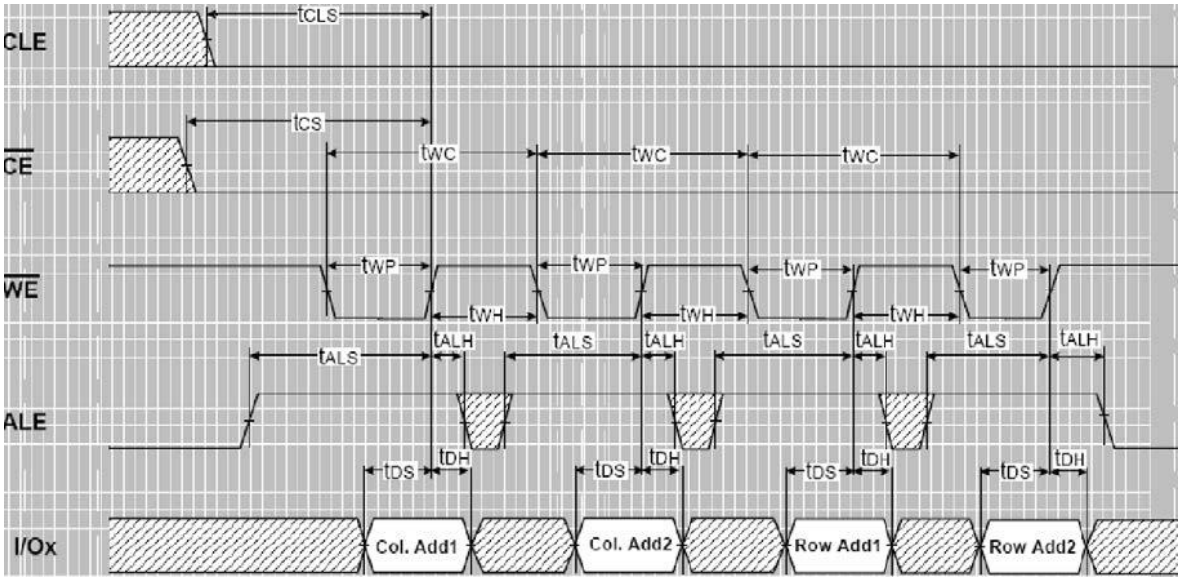

Figure 3.3. Address Latch Cycle

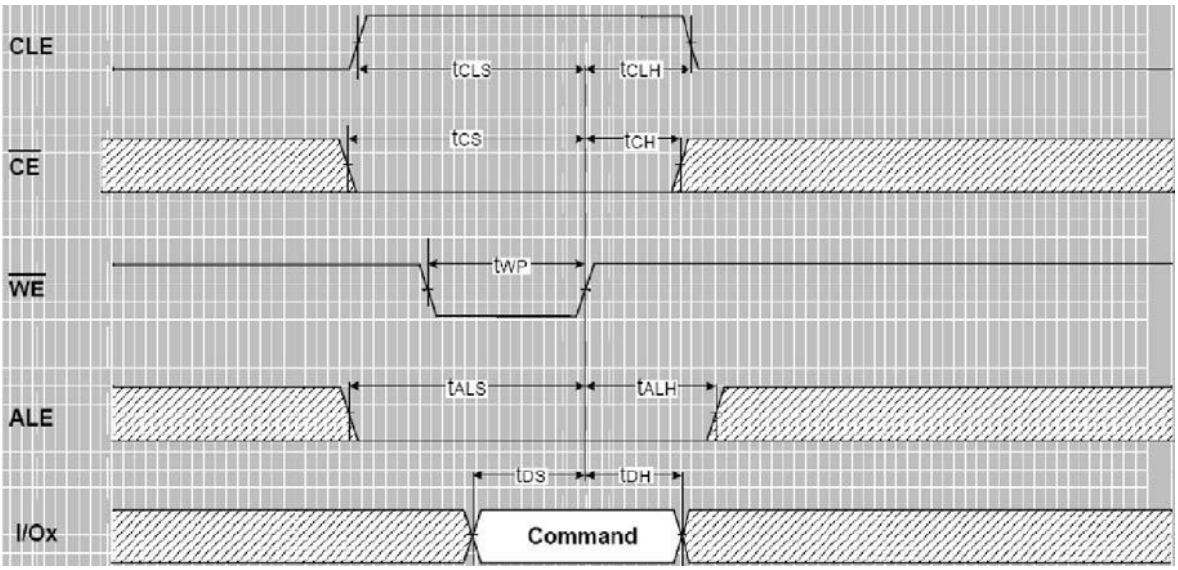

Figure 3.4. Command Latch Cycle

Table 3.1. Pin Descriptions

Signal Name	Signal Direction	Active State	Definition
Host End interface			
CLK	Input	N/A	Clock signal.
RES	Input	High	Reset signal.
BF_sel	Input	High	Dual-port RAM clock enable signal.
BF_ad[10:0]	Input	N/A	Dual-port RAM address signal.
BF_din[7:0]	Input	N/A	These lines are used to pass data to the dual-port RAM.
BF_we	Input	High	Dual-port RAM write signal.
RWA[15:0]	Input	N/A	These address signals are used by the Flash device.
BF_dou[7:0]	Output	N/A	These lines are used to pass data to host.
PErr	Output	High	Page program operation error signal.
EErr	Output	High	Block erase operation error signal.
RErr	Output	High	Page read operation error signal.
nfc_cmd[2:0]	Input	N/A	Command code signal.
nfc_strt	Input	High	When asserted, indicates the host initiates a operation.
nfc_done	Output	High	When asserted, indicates an operation is done.
NAND Flash Interface			
DIO[7:0]	In/Out	N/A	I/O pins used to send commands, address, and data to the Flash, and receive data during read operations.
CLE	Output	High	Command Latch Enable.
ALE	Output	High	Address Latch Enable.
WE_n	Output	Low	Write Enable.
RE_n	Output	Low	Read Enable.
CE_n	Output	Low	Chip Enable.
R_nB	Input	N/A	When this signal is high, the Flash is ready for the next operation. When it is low, an internal operation is in progress.

4. Register Transfer Level (RTL) Implementation

The block diagram of the NAND Flash controller is shown in Figure 4.1.

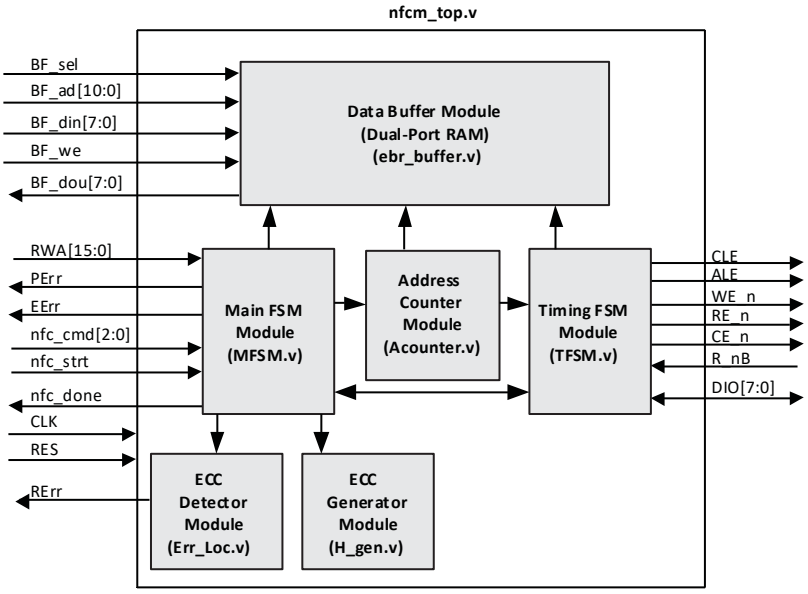

Figure 4.1. Block Diagram

The main FSM module and the timing FSM module, containing two state machines, are the primary modules of the design. These two modules work with each other. The state machine in the main FSM module interprets commands from the host, then passes control signals to the timing FSM module. The state machine in the timing FSM module creates all the necessary control signals for the NAND Flash to execute repeated tasks with strict timing requirements according to the signals from the main FSM module. The data buffer module is implemented by internal dual port RAM which is generated by the Lattice ispLEVER® design tool. This module is used as a data buffer when the host writes data to the Flash and reads data from the Flash. The address counter module generates the address control signals required for the data buffer module based on the state machine in the main FSM module. The ECC generator module generates the Error Correction Code (ECC) during program operation and stores the ECC code in the NAND Flash. The ECC detector module makes use of this ECC code in the Flash memory to detect errors in the data during host read operation.

5. Operation of the NAND Flash Device

This reference design supports the following operations/commands:

- Reset
- Read ID
- Erase (per block basis)
- Program Page (copy content of data buffer into Flash memory)
- Read Page (content of a Flash page is copied into the data buffer)
- Read Status

The command code must be written to the command register before every operation of the NAND Flash. The command register does not occupy any addressable memory location. This register holds the command, along with any address and data information needed to execute the command. Table 5.1. describes Samsung K9F1G08R0A command sets which are implemented by this design.

Table 5.1. Samsung K9F1G08R0A Command Set

Function	Command Code (Hex)	Description
Reset	FFh	The reset function is used to abort write or read operations in the flash.
Read ID	90h	The Flash device contains a product identification mode, this function is used to read these information.
Read	00h and 30h	Read out one page (2K bytes) from the Flash.
Page Program	80h and 10h	Write (2K bytes) to the Flash.
Block Erase	60h and D0h	Erase one block (64 pages) of the Flash.
Read Status	70h	Check the device status to determine if the program and erase operation is failure.

5.1. Reset Operation

When the host interface signal nfc_cmd is set to 011 and the signal nfc_strt is active, it indicates the host initiates reset operation. The state machine in the main FSM module switches from initial state to the state implementing the reset operation. In this state, the main FSM module passes control signals to the timing FSM module to execute writing command code FFh to the NAND Flash. When the writing command code is done the state machine switches to initial state and waits for the next operation. Figure 5.1. shows the reset operation flow chart.

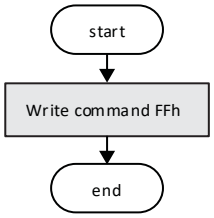

Figure 5.1. Reset Operation Flow Chart

5.2. Read ID Operation

The design initiates read ID operation when the host interface signal nfc_cmd is set to 101 and the signal nfc_strt is active. The state machine in the main FSM module switches from initial state to the states implementing read ID operation. First the state machine writes command code 90h to the Flash, and then writes address code 00h to the Flash. Lastly, the state machine reads ID information from the Flash. The four read cycles sequentially output the manufacturer code (ECh), the device code (for Samsung K9F1G08R0A, this code is A1h), the do not care code XXh, and the fourth cycle ID (for Samsung K9F1G08R0A, this code is 15h). For every step, the state machine calls the timing FSM module to generate the corresponding control signals to access the NAND Flash-based on the NAND Flash timing requirements. When the read ID operation is done, the state machine switches to the initial state to wait for the next operation. Figure 5.2. shows the read ID operation flow chart.

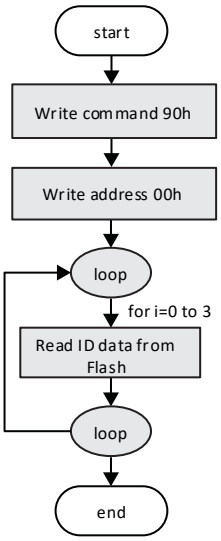

Figure 5.2. Read ID Operation Flow Chart

5.3. Block Erase Operation

The design initiates block erase operation when the host interface signal nfc_cmd is set to 100 and the signal nfc_strt is active. The state machine in the main FSM module switches from initial state to the states implementing block erase operation. First, the state machine writes command code 60h to the Flash, and then writes address code to the Flash. These address code must be set by the host in advance. After writing address is done the state machine writes the command code d0h to the Flash and then wait for tWB time. The tWB is a parameter of Samsung K9F1G08R0A. It indicates the time of WE going high to Busy going high. The state machine then detects the signal R_nB. If the R_nB is set to 1 by the Flash, it indicates the Flash finishes the block erase operation. Then the state machine sends the read status command code 70h to the Flash to test if the block erase operation is successful. If the status returned by the Flash is 1, it indicates the block erase operation is successful. Otherwise, the state machine sets the signal EErr to 1 to tell the host the block erase operation has failed. For every step, the state machine calls the timing FSM module to generate the corresponding control signals to access the NAND Flash with the necessary timing requirements. When the read status operation is done the state machine switches to the initial state to wait for the next operation. Figure 5.3. shows the block erase operation flow chart.

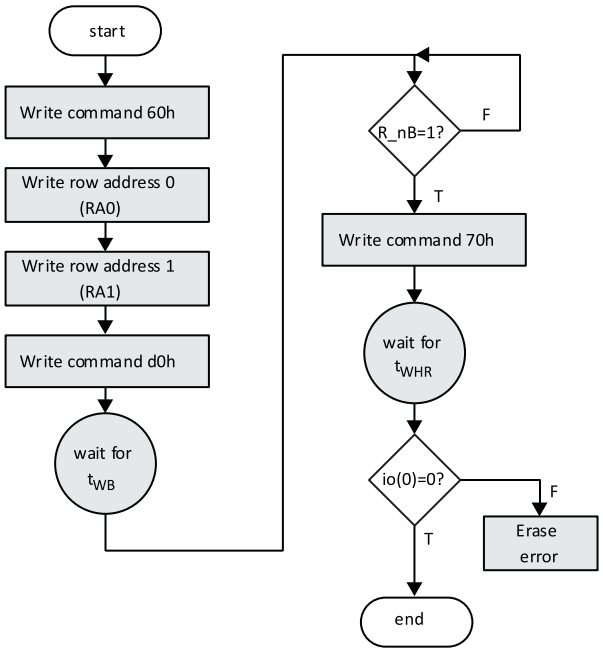

Figure 5.3. Block Erase Flow Chart

5.4. Page Program Operation

The design initiates page program operation when the host interface signal nfc_cmd is set to 001 and the signal nfc_strt is active. The state machine in the main FSM module switches from initial state to the states implementing page program operation. First the state machine writes command code 80h and address code to the Flash. The address code must be set by the host in advance. Then the state machine transmits 2048 bytes to the Flash from the data buffer (dual-port RAM). The address signals of the data buffer are generated by the address counter module based on the control signals sent by the state machine. For Samsung K9F1G08R0A, it can be programmed up to 2112 bytes at a time. This design writes at most 2048 bytes to the Flash at a time. After writing 2048 bytes, the state machine begins to write 12 ECC bytes which are generated by the ECC generator module to the Flash prepared for the ECC detector. First the state machine writes the command code 85h and address and then writes the 12 ECC bytes to the Flash. When all the above steps are complete, the state machine writes the command 10h to the Flash. After tWB period of time the state machine detects the signal R_nB. If the R_nB is set to 1 by the Flash, it indicates the Flash finishes the page program operation. Then the state machine sends the read status command code 70h to the Flash to test if the page program operation is successful. If the status returned by the Flash is 1 it indicates the page program operation is successful. Otherwise, the state machine sets the signal PErr to 1 to tell the host the page program operation fails. For every step, the state machine calls the timing FSM module to generate the corresponding control signals to access the NAND Flash. When the read status operation is done, the state machine switches to the initial state to wait for the next operation. Figure 5.4. shows the page program operation flow chart.

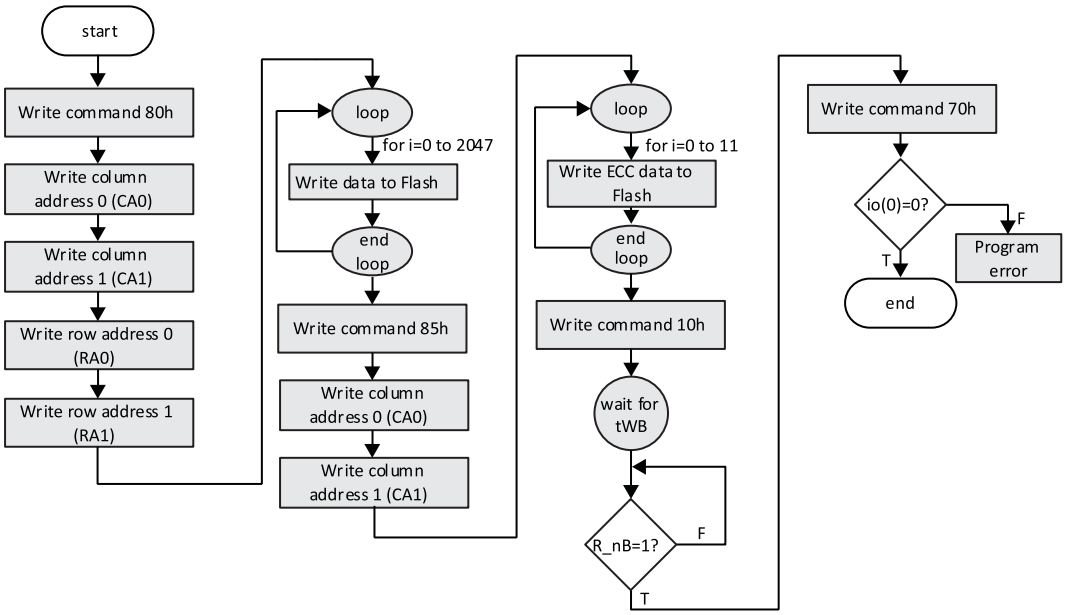

Figure 5.4. Page Program Flow Chart

5.5. Page Read Operation

The design initiates page read operation when the host interface signal nfc_cmd is set to 010 and the signal nfc_strt is active. The state machine in the main FSM module switches from the initial state to the states implementing page read operation. First the state machine writes command code 00h and address code to the Flash. Then the state machine writes the command code 30h to the Flash. After tWB amount of time the state machine detects the signal R_nB. If the R_nB is set to 1 by the Flash, it indicates the Flash is ready to send data. Then the state machine begins to read 2048 bytes from the Flash and stores these bytes in the data buffer (dual port RAM). The address signals of the data buffer are generated by the Address counter module based on the control signals sent by the state machine. After reading 2048 bytes, the state machine begins to read 12 ECC bytes from the Flash. First the state machine writes the command code 05h and address to the Flash and then writes the command code e0h to the Flash. After this is done, the state machine reads 12 ECC bytes from the Flash and calls the ECC detector module to detect if an error occurs in the ECC bytes. If there is error in the ECC bytes, then the state machine sets the signal RErr to 1. For every step, the state machine calls the timing FSM module to generate the corresponding control signals to access the NAND Flash. When the page read operation is done, the state machine switches to the initial state to wait for the next operation. Figure 5.5. shows the page read operation flow chart.

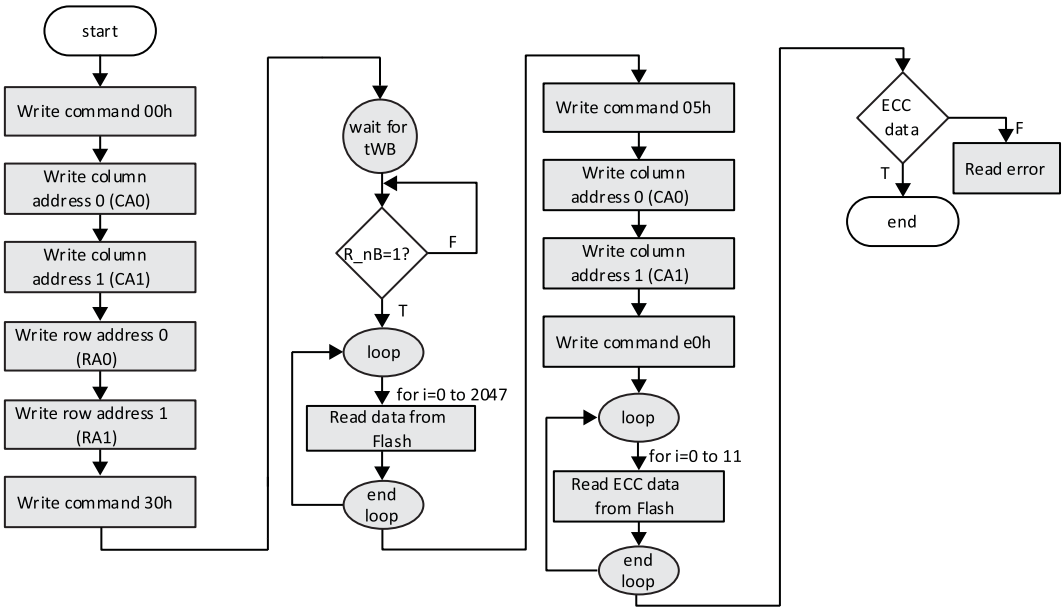

Figure 5.5. Page Read Flow Chart

6. Test Bench Description

The test bench for this design includes the reset task, read ID task, block erase task, page program task and page read task to perform the corresponding operations of the NAND Flash memory.

7. Timing Specifications

The following timing diagrams show the major timing milestones in the simulation.

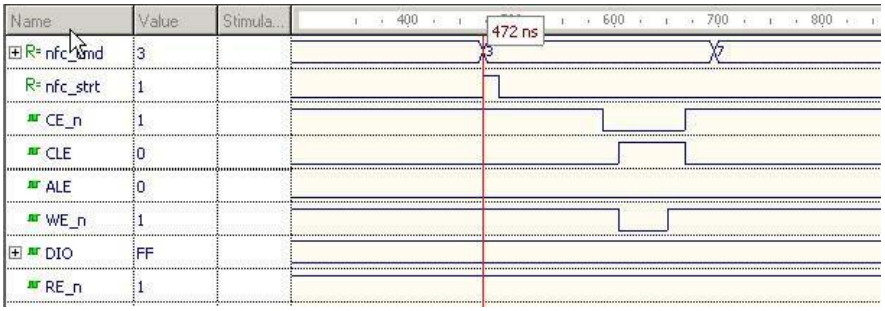

Figure 7.1. Reset Operation

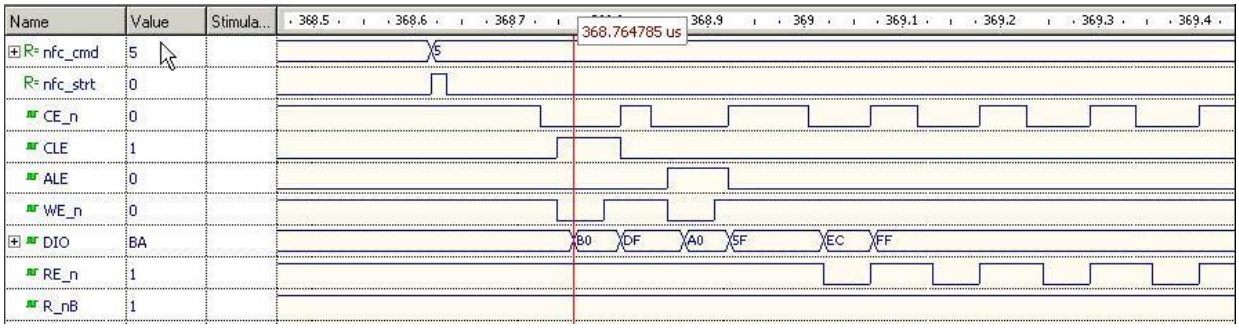

Figure 7.2. Read ID Operation

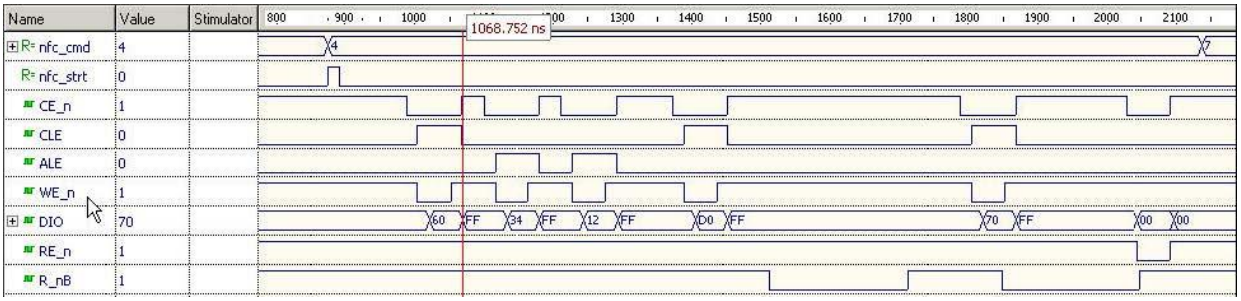

Figure 7.3. Block Erase Operation

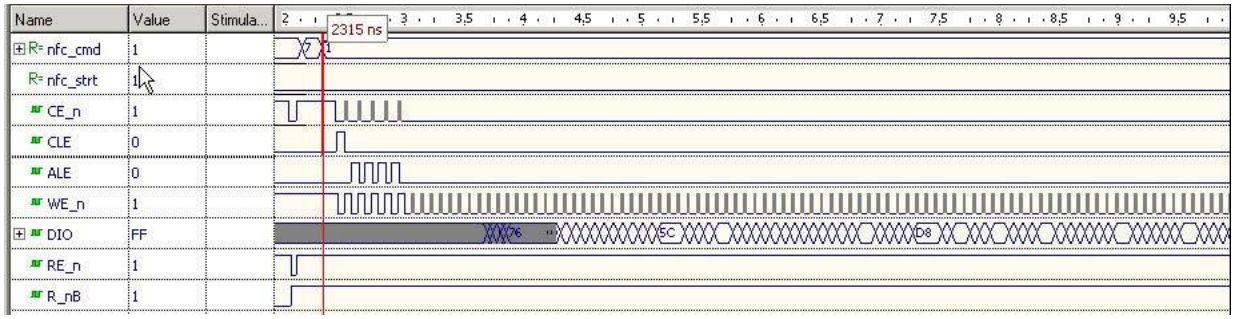

Figure 7.4. Page Program Operation

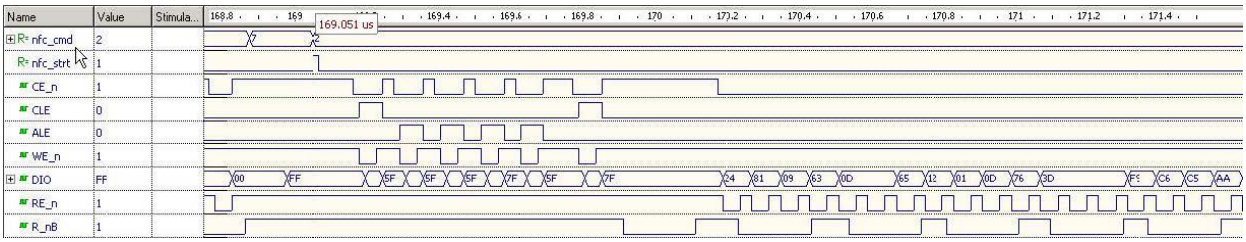

Figure 7.5. Page Read Operation

8. Implementation

Table 8.1. Samsung K9F1G08R0A Command Set

Device Family	Language	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
MachXO2™ [1]	Verilog	-4	434	>80	69	2 EBRs
	VHDL	-4	398	>80	69	2 EBRs
MachXO™ [2]	Verilog	-5	455	>80	69	2 EBRs
	VHDL	-5	459	>80	69	2 EBRs
LatticeXP2™ [3]	Verilog	-7	519	>80	69	1 EBR
	VHDL	-7	515	>80	69	1 EBR

Notes:

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-4TG144CES, with Lattice Diamond™ 1.1 or ispLEVER® 8.1 SP1. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO2280C-5T100C, with Lattice Diamond 1.1 or ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LFXP2-5E-7M132C, with Lattice Diamond 1.1 or ispLEVER 8.1 SP1. When using this design in a different device, density, speed, or grade, performance and utilization may vary.

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Revision History

Revision 1.3, December 2019

Section	Change Summary
All	• Changed document number from RD1055 to FPGA-RD-02095. • Updated document template.
Disclaimers	Added this section.

Revision 1.2, November 2010

Section	Change Summary
Implementation	Added support for MachXO2 device family and Lattice Diamond design software.

Revision 1.1, January 2010

Section	Change Summary
Implementation	• Added support for LatticeXP2 device family. • Added VHDL support.

Revision 1.0, July 2009

Section	Change Summary
All	Initial release.

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