Using Multiple Boundary Scan Port Linker (BSCAN2)

Application Note

FPGA-AN-02017-1.1

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1. Introduction

Although the primary goal of JTAG/IEEE 1149.1 is simplified testability, modern systems may contain more devices than is practical in many cases. Adding to this challenge, are devices that have special restrictions or requirements that may limit test procedures.

The Lattice Multiple Boundary Scan Port Linker (BSCAN2) Reference Design (FPGA-AN-02017) provides a flexible solution to the problems presented by the growing number of IEEE1149.1 capable devices in today's complex systems. BSCAN2 allows a system designer to isolate devices in a way that makes the best sense for the test objectives and types of devices used. Access to any individual chain can then be dynamically controlled during the desired operations.

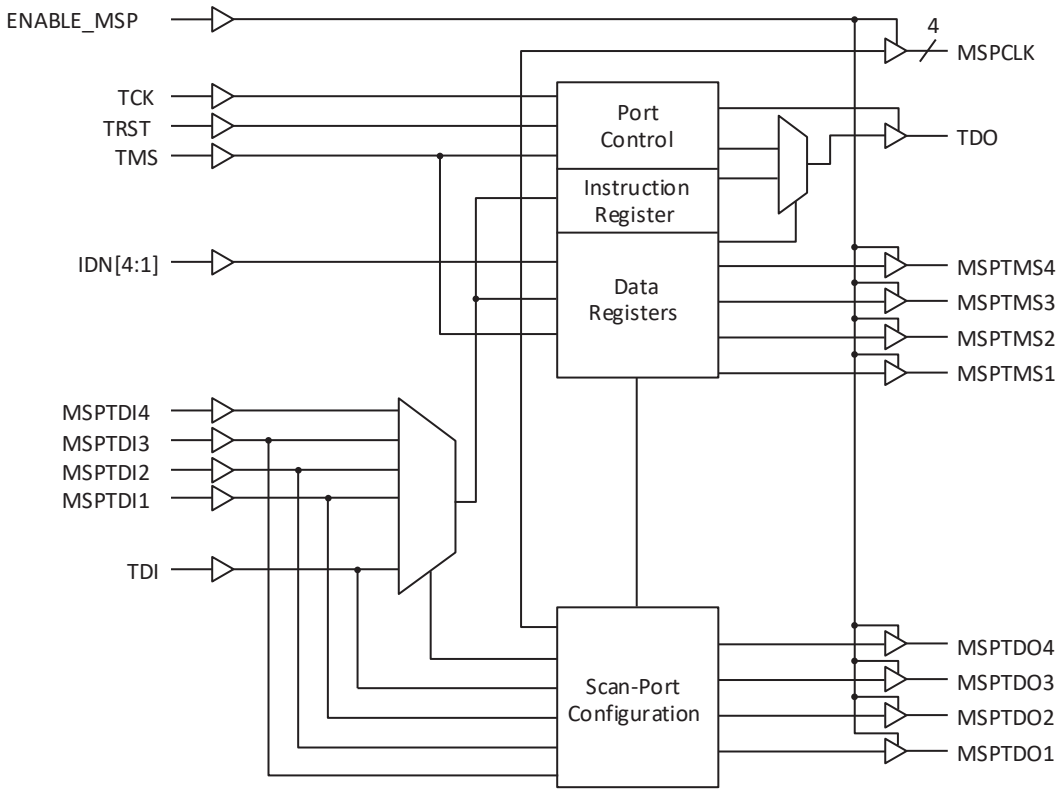

Figure 1.1. BSCAN2 Block Diagram

2. Applications

There are a variety of reasons to segment devices into separate JTAG chains. This section briefly discusses them.

2.1. Simplification

Often, a smaller subset of devices may run more rigorous or more frequent boundary scan procedures. These devices can be consolidated to separate them from less frequently accessed devices.

2.2. Reduce the Need for Buffering

As the number of devices in a JTAG chain increases, the signals that are distributed in parallel – TCK, TMS and TRST – require buffering to reduce the effects of fanout. Creating smaller sub-chains reduces this requirement. Additional I/O buffers can also be used for larger sub-chains to reproduce these signals.

2.3. Mixed JTAG Voltages

Handling multiple voltages in a JTAG chain involves careful consideration and often level translators. The flexible I/O banking structure of Lattice PLDs allows multiple I/O voltages within the same device. This allows the system designer to greatly simplify this task by placing only compatible voltage devices in each sub-chain.

2.4. Removable Subsystems

Modular systems ordinarily require separate JTAG chains or the presence of all daughter cards for boundary scan continuity. Partitioning each sub-chain according to a physical connector allows a flexible method to route around any portion of the system that is not currently present.

2.5. JTAG Chain Faults

The serial nature of JTAG signaling means that a faulty or physically damaged device can render the rest of the devices in the same chain inaccessible. By creating smaller sub-chains, a problem device can be routed around, leaving other sub-chains available. Other system testing can be performed in this case, allowing the ability to test other parts of the system for faults.

2.6. Supply Separation

During portions of boundary scan testing, some devices may be desired or required to be fully powered down. Since an unpowered device disrupts the JTAG chain, separating devices according to supply requirements allows a flexible solution for partially powered conditions.

2.7. Custom Access Requirements

Implementation in a PLD allows flexible configurations to suit custom requirements. It may be desirable to select between two master JTAG ports, or add provisions to connect to a sub-chain directly externally. By adding simple logic outside of the BSCAN2 blocks, alternate access methods are easily achieved.

2.8. Low-Speed Devices

The overall TCK rate is limited to the lowest speed allowed by the slowest device in a chain. A device with a low TCK frequency specification may be a significant bottleneck in performance when other devices are capable of higher speeds. Partitioning slower devices into separate chains allows disabling of these devices to utilize a higher test speed for the remaining devices.

2.9. Devices with Special Requirements

Although most modern devices have no significant IEEE 1149.1 compliance issues, legacy or more obscure devices may be present in a system design that limit the capabilities of the overall JTAG chain. These devices can be isolated to allow a broader range of operation for fully compliant devices.

An example of partitioning a JTAG chain is shown below in Figure 2.1. In this example, an FPGA, CPLD and an ASIC device comprise one 3.3 V chain. A lower voltage 1.8 V chain is assembled in a second, consisting of an ASIC and another FPGA. A third chain contains processor devices, specifically separated from other devices. The fourth and final chain in this example is used to isolate one ASIC device that has been determined to have some special requirements or restrictions.

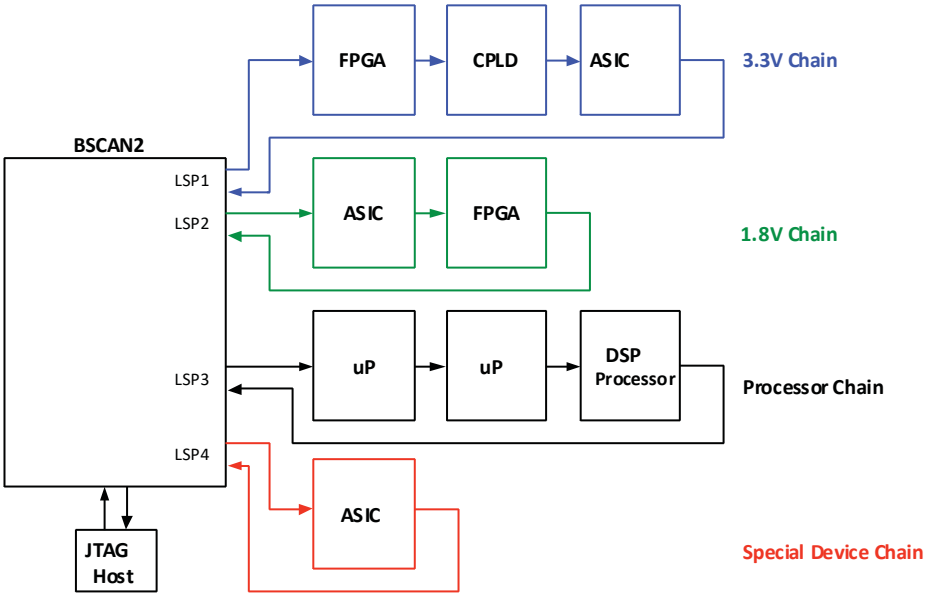

Figure 2.1. Example Chain Setup

After defining the chain partitions and connecting accordingly, the overall chain is now configurable through BSCAN2 register control. Any combination of sub-chains can now be enabled. Figure 2.2. shows a simplified logical data path when all LSPs are active.

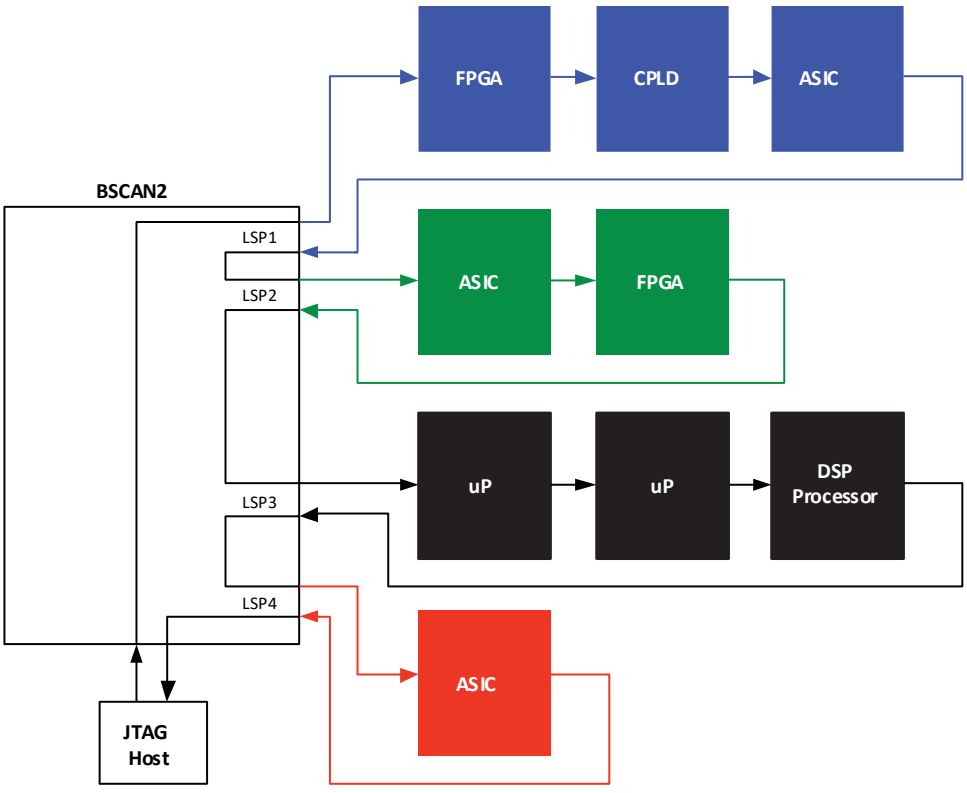

Figure 2.2. All Ports Active

For situations where specific inclusion or exclusion of sub-chains is desired, the selection of sub-chains can be more specific. In the case of programming programmable logic devices, relevant sub-chains can be targeted, as illustrated in

Figure 2.3. In this case, the overall JTAG chain is routed around LSPs three and four, completely excluding them. The TAP controllers of each of the excluded devices remains in a constant state and no data is presented to them.

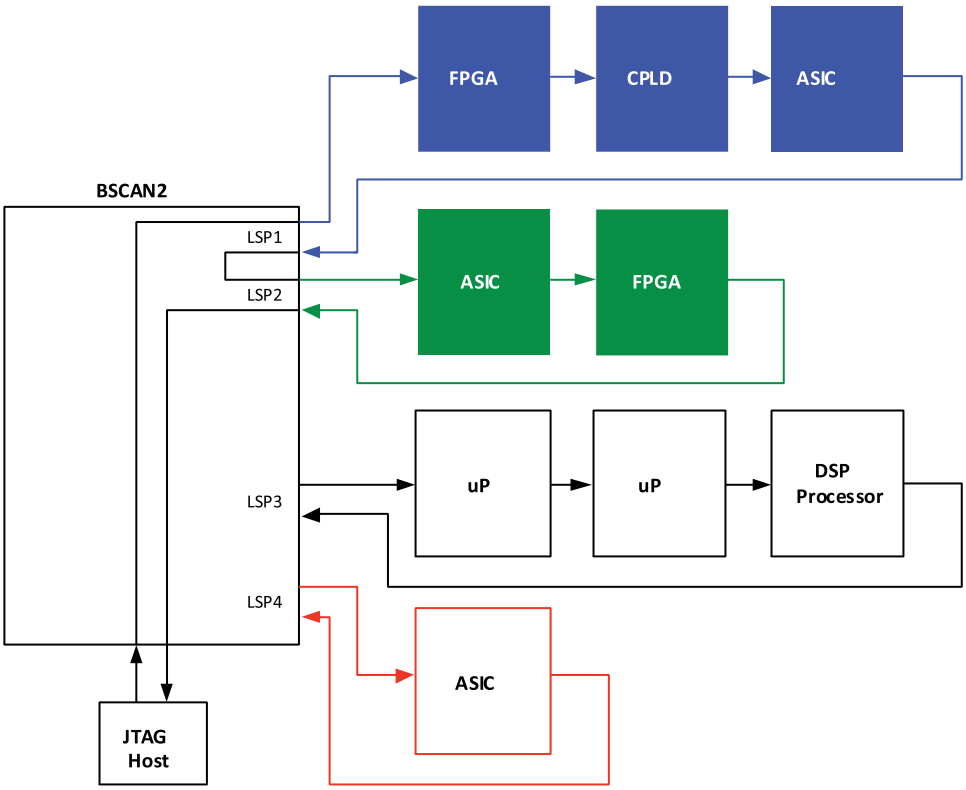

Figure 2.3. Ports 1 and 2 Active

Some devices may have special requirements or have JTAG compliance issues that may disturb other, compliant devices. This problem is easily solved by selection of only the required sub-chain, as shown in Figure 2.4.

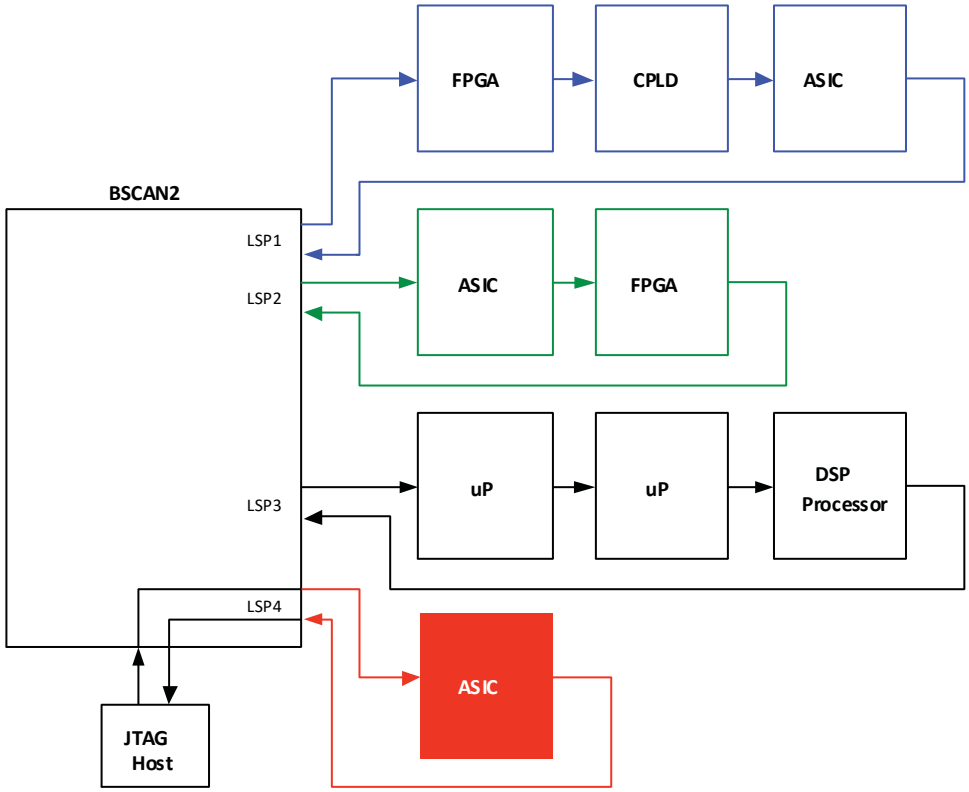

Figure 2.4. Port 4 Active

It may be desirable to target some devices only when very specific conditions have been met. Examples of such devices are microprocessors and microcontrollers that maintain specific functions critical to vital operation of the system. It may be necessary in this case to put the system in a special state or operate from special power supplies before proceeding with a boundary scan or JTAG operation. In the example chain, this is shown as Figure 2.5., where LSP3 is selected.

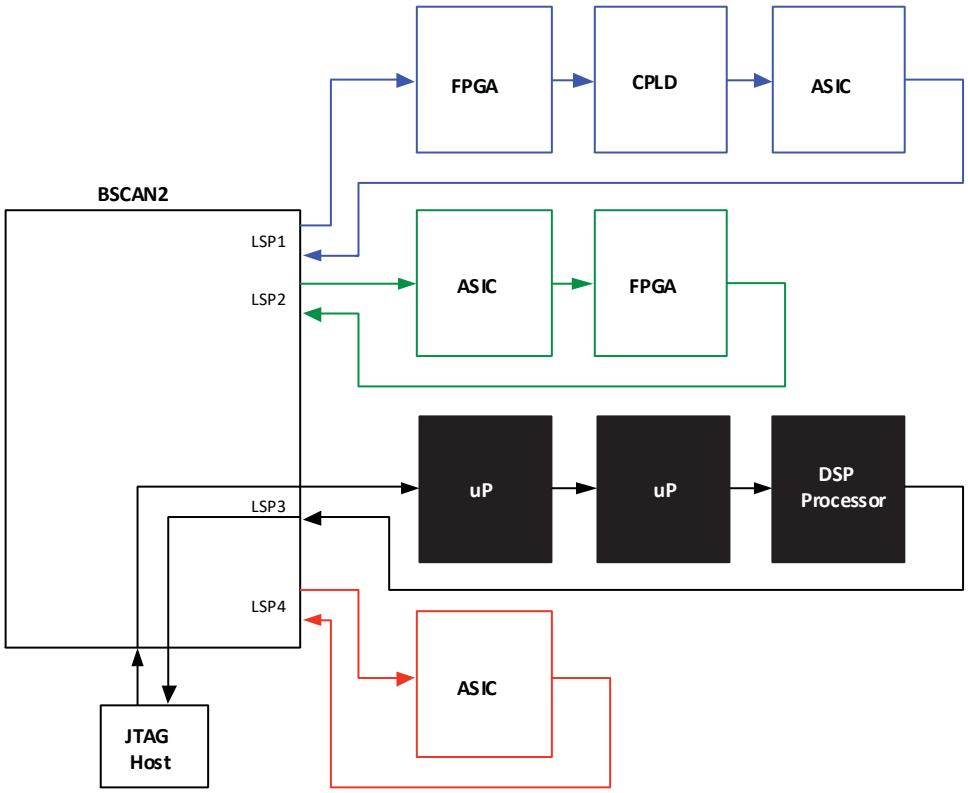

Figure 2.5. Port 3 Active

Although boundary scan is often used to perform thorough board-level connectivity tests with great efficiency, it relies on connectivity of all associated devices in a daisy-chain JTAG configuration. The potential vulnerability in this scheme is obvious when one device is physically damaged, defective, or installed incorrectly, affecting its JTAG port or associated logic. In this case, the malfunctioning device blocks the serial communication of otherwise valid boundary scan commands and data, rendering the test useless.

By partitioning the JTAG devices into smaller sub-chains, the impact of this potential problem is reduced in two ways. First, the chains with proper JTAG continuity can be tested to their full extent, allowing valid boundary scan test information to be collected on the rest of the system. Second, it allows the same test methodology to narrow down which device is malfunctioning, aiding in troubleshooting efforts.

The capability to route around a device's non-functional JTAG circuitry is illustrated in Figure 2.6.

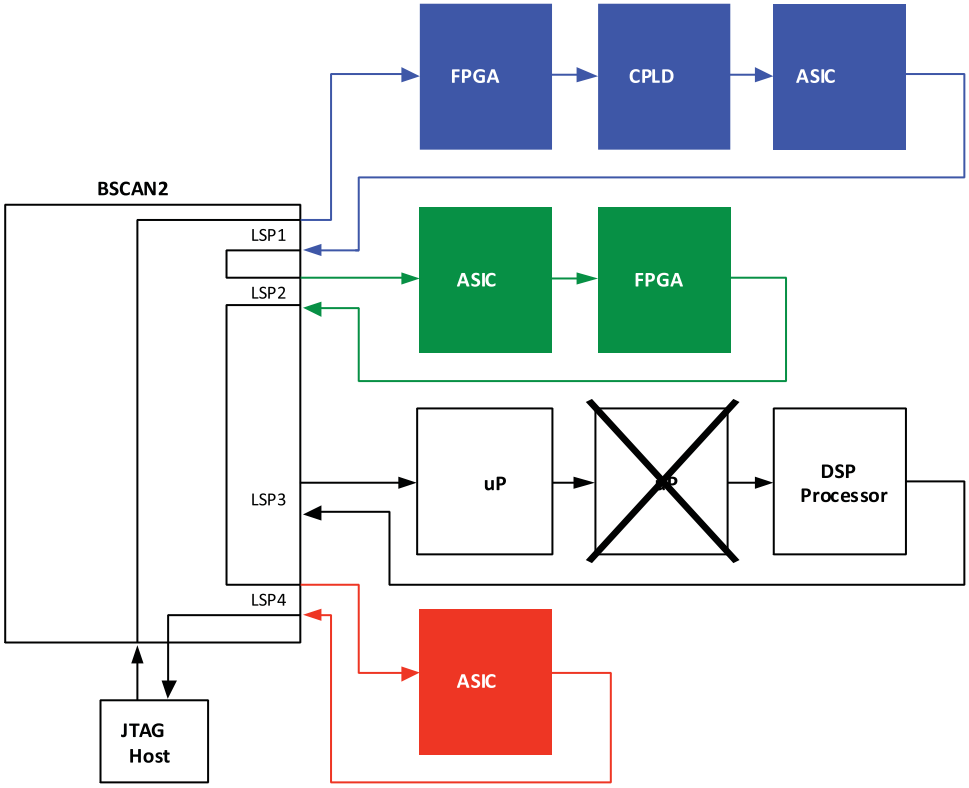

Figure 2.6. Exclusion of a Non-Functioning Device

3. Design Details

A more detailed diagram of the data path is illustrated in Figure 3.1. The conceptual multiplexing scheme as well as the latency of each LSP is shown. Each LSP, when enabled, adds one TCK cycle of latency before entering the local sub-chain. This flip-flop aids in meeting register-to-register timing for improved clock frequencies. One additional register exists at the end of the top_linker module. This register represents either its 8-bit instruction register, or one of the available data registers. A list of these register lengths is provided in Table 3.1.

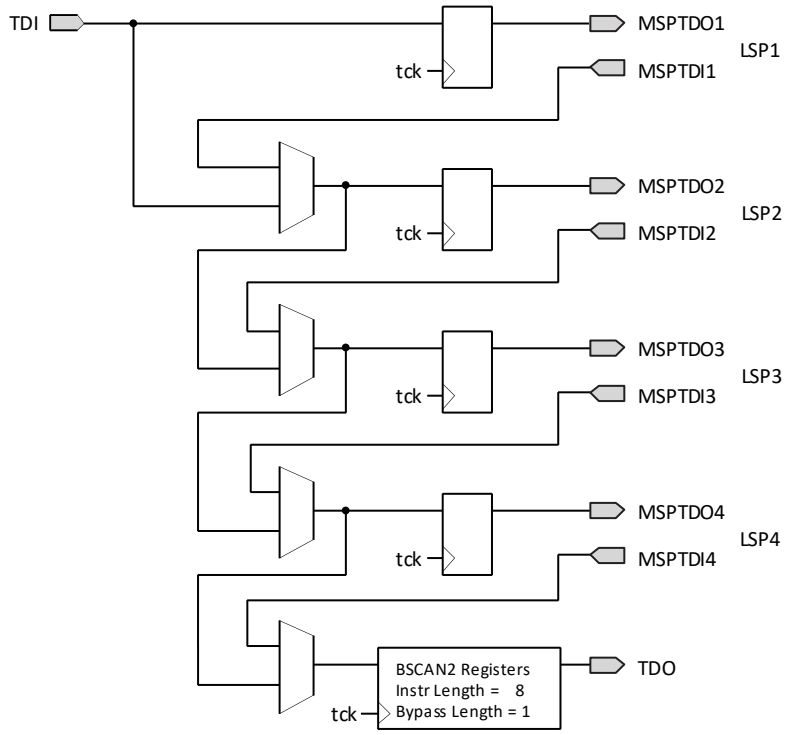

Figure 3.1. Simplified Functional Diagram of BSCAN2 4-Port top_linker Module

Table 3.1. BSCAN2 Register Lengths

Register	4-Port	8-Port Asset	8-Port JTAG
Instruction	8	8	8 + 8[1]
Select	8	16	8 + 8[1]
ID	4	4	4 + 4[1]
Bypass	1	1	1 + 1[1]

Note: 1.1.8-Port JTAG model has two separate registers. The first is between LSP4 and LSP5, and the second after LSP8.

The BSCAN2 module is comprised of a central module named 'top_linker' and associated routing and connections to the device. Tristate buffers are not present within the 'top_linker' block to allow flexibility in connection of the signals.

The most straight-forward connection is to simply bring the signals to the device I/O pins, as shown in Figure 3.2. The 'TDO_enable' signal provides an output enable for TDO, allowing it to be active only in the Shift-IR and Shift-DR TAP controller states for IEEE1149.1 compliance.

The 4-bit IDN bus provides an identification mechanism, allowing the JTAG host to confirm the presence of BSCAN2. This bus can be brought to I/O pins to set externally, or tied to a constant value at the instantiation of the 'top_linker' module.

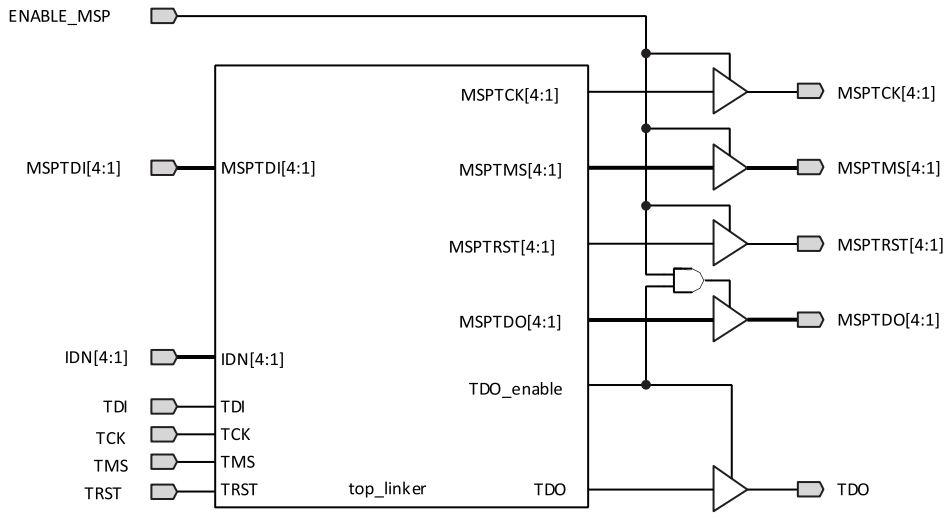

Figure 3.2. Instantiation Connections for BSCAN2 top_linker Module

Notes:

1. Identification (IDN) inputs may be set from input pins or connected to hard-coded value in top_linker instantiation.
2. TRST input optional. Tie to static high in top_linker instantiation to ignore the effects of this signal.
3. ENABLE_MSP is optional. Driving this input low forces the MSP outputs to tristate, allowing an external device to control the lines.
4. MSPTRST[] outputs are optional. If unused, these I/Os may be removed and the output from the top_linker module left open.

Multiple 'top_linker' modules can be chained together to increase the number of available BSCAN2 ports. This is accomplished by connecting TDO of one block to another's TDI, as shown in Figure 3.3.

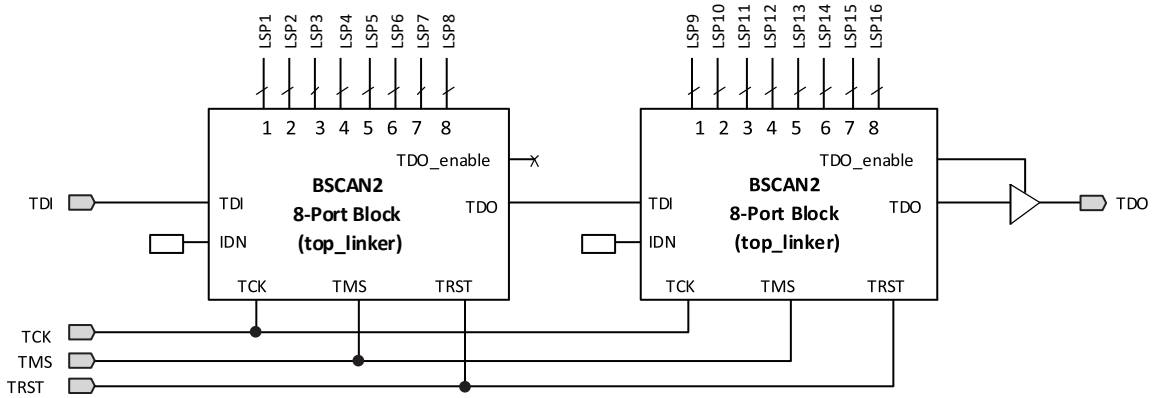

Figure 3.3. Adding Ports by Chaining BSCAN2 top_linker Modules

Notes:

1. Identification (IDN) inputs may be set from input pins or connected to hard-coded value in top_linker instantiation.
2. Detailed MSP signal connections to LSPs not shown. Similar to instantiations of one top_linker block.
3. TRST input optional. Tie to static high in top_linker instantiation to ignore the effects of this signal.
4. TDO_enable output logically equivalent from each top_linker block.

References

- Multiple Boundary Scan Port Linker (BSCAN2) Reference Design (FPGA-AN-02017)
- Lattice Semiconductor BSCAN2 Webpage – www.latticesemi.com/products/intellectualproperty/referencedesigns/multipleboundaryscanportl.cfm

Third-Party Tools

- Asset – www.asset-intertech.com
- Corelis – www.corelis.com
- JTAG Technologies – www.jtag.com

Q & A

Q: How many ports can be supported by BSCAN2?

A: The pre-defined models support either 4 or 8 ports. Since the BSCAN2 modules can be chained, larger implementations can be easily configured.

Q: Can BSCAN2 modules be cascaded?

A: Yes. The BSCAN2 modules can be connected to the LSP ports of other BSCAN2 modules. This configuration is useful when there are multiple removable boards in a large system.

Q: What is the 4-bit IDN input used for?

A: This sets an identification register for the BSCAN2 block. The JTAG host can query this register to ensure the BSCAN2 function is present. The JTAG host software will require that you specify this value if this check is performed.

Q: Are there any limitations of the number of devices supported by BSCAN2?

A: There is no specific limit for the number of BSCAN2 devices or number of JTAG devices attached to any LSP. Signal fanout should be controlled with buffering as necessary. JTAG host software may have limitations for memory or performance reasons. Check with the vendor for specific limits.

Q: Can other unrelated logic be placed in the same PLD that implements BSCAN2?

A: Yes. Other logic can be placed in the PLD, as long as it does not hinder the ability for BSCAN2 to operate.

Q: Can logic be added to BSCAN2 within the PLD?

A: Yes. Added logic, such as multiplexers and buffers can be added. Care should be taken to not impact the logical access of the JTAG host to BSCAN2. In the case of multiplexers, the path from the JTAG host to BSCAN2 and its LSP connections should be configured when running the host software.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, January 2022

Section	Change Summary
All	• Changed document number from AN8081 to FPGA-AN-02017. • Updated document template.
Disclaimers	Added this section.

Revision 1.0, July 2009

Section	Change Summary
All	Initial release.

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