LatticeECP3 Marvell XAUI 10 Gpbs Physical Layer Interoperability

February 2012 Technical Note TN1194

Introduction

This technical note describes a physical layer 10-gigabit Ethernet: XAUI (10 Gbps) interoperability test between a LatticeECP3™ device and the Marvell Alaska 88X2040 device. The test was limited to the physical layer (up to XGMII) of the 10-gigabit Ethernet protocol stack.

The document discusses the following topics:

- Overview of LatticeECP3 and Marvell Alaska 88X2040 devices.
- XAUI Physical layer interoperability setup, testing and results.

XAUI Interoperability

XAUI is a high-speed interconnect that offers reduced pin count and the ability to drive up to 20” of PCB trace on standard FR-4 material. In order to connect a 10-gigabit Ethernet MAC to an off-chip PHY device, an XGMII interface is used. The XGMII is a low-speed parallel interface for short range (approximately 2”) interconnects.

XAUI interoperability is based on the 10-Gigabit Ethernet standard (IEEE Standard 802.3ae-2002). Two XAUI link partners can be directly plugged into a XAUI backplane. Both boards are capable of generating and checking packets.

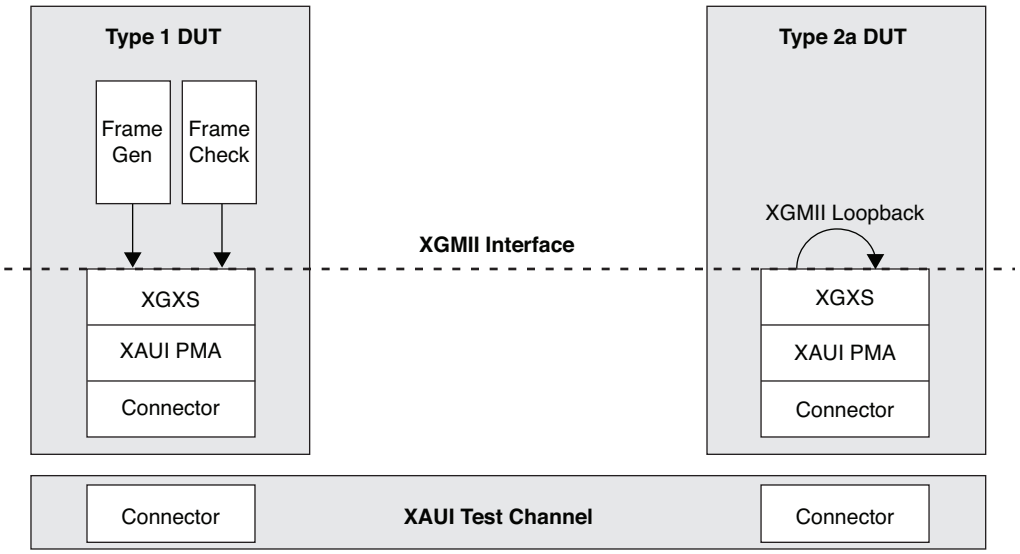
The board that sources packets is capable of keeping a detailed count of the number of packets transmitted while the sink board is capable of keeping detailed statistics on the number of packets received and errors associated with the packets. The XAUI backplane is also called the XAUI test channel. A typical test setup is shown in Figure 1.

Each reference station must be a line card that is directly plugged into the XAUI test channel. Both DUTs are required to have their own clock domain. Synchronous clocking (distributing a single clock to the two DUTs) is not allowed. Local management indicators on the DUT (reference stations) that provide information on link-level errors, such as CRC errors, are also needed. A DUT is called a Type #1 device if it is capable of transmitting and checking packets.

A DUT is called a Type #2a device if it receives packets and does a RX-to-TX loopback through XGMII and sends the packets back to the transmitting station, which is a Type #1 device. The Type #1 device then checks the received packets for errors. Figure 1 shows a setup where one DUT is of Type #1 and the other is of Type #2a.

The LatticeECP3 and Marvell Alaska 88X2040 interoperability exercises the whole physical layer, including XGMII.

Figure 1. Typical XAUI Interoperability Test Setup



LatticeECP3 Overview

LatticeECP3 Features

The LatticeECP3 FPGA family combines a high-performance FPGA fabric, high-performance I/Os and up to 16 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The PCS logic can be configured to support numerous industry-standard, high-speed serial data transfer protocols.

Each channel of PCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfer at data rates up to 3.2 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including GbE, XAUI, PCI Express, SRIO, CPRI, SD-SDI, HD-SDI and 3G-SDI.

LatticeECP3 in XAUI Mode

The LatticeECP3 XAUI reference design was used for the interoperability exercise. The design includes both the LatticeECP3 SERDES/PCS and the LatticeECP3 XAUI soft IP. For more information on the LatticeECP3 XAUI reference design, please refer to UG23, LatticeECP3 XAUI Demo Design User's Guide. The LatticeECP3 SERDES/PCS in XAUI mode along with the Lattice XAUI soft IP, provides full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard.

Transmit Path Functionality (From LatticeECP3 Device to Line)

- Transmit State Machine which performs translation of XGMII idles to proper ||A||, ||K||, ||R|| characters according to the IEEE 802.3ae-2002 specification (LatticeECP3 XAUI IP)
- 8b10b encoding and data serialization (LatticeECP3 SERDES/PCS)

Receive Path Functionality (From Line to LatticeECP3 Device)

- Word alignment based on IEEE 802.3-2002 defined alignment characters (LatticeECP3 SERDES/PCS)
- 8b10b decoding (LatticeECP3 SERDES/PCS)
- Link State Machine functions incorporating operations defined in PCS Synchronization State Diagram of the IEEE 802.3ae-2002 specification (LatticeECP3 SERDES/PCS)
- Multi-channel alignment (LatticeECP3 XAUI IP)
- Clock Tolerance Compensation logic capable of accommodating clock domain differences (LatticeECP3 XAUI IP)
- Receive State Machine compliant to the IEEE 802ae.3-2002 specification (LatticeECP3 XAUI IP)

Marvell Alaska 88X2040 Overview

Marvell Alaska 88X2040

The Marvell 88X2040 Quad transceiver is a fully-integrated serialization/de-serialization device that incorporates four independent lanes, delivering high-speed bi-directional point-to-point baseband data transmission that supports cost-effective IEEE 802.3ae compliant 10-gigabit Ethernet and 10-gigabit Fibre Channel applications.

The 88X2040 Quad can be configured either as four separate high-speed lanes or as a single data path with four synchronized lanes. It supports a wide range of serial data rates from 1.0 Gbps to 3.1875 Gbps. The 88X2040 supports the 32-bit bi-directional 10-Gigabit Media Independent Interface (XGMII) with 8b10b ENDEC option, and the extended Auxiliary Unit Interface (XAUI). The 88X2040 performs the parallel-to-serial, serial-to-parallel conversion with integrated Time Base Generator (TBG) and Clock/Data Recovery Circuit (CDRC).

On-chip synthesis performed by the high-performance, high-frequency, and low jitter phase-locked loop on the 88X2040 transceiver allows the use of cost-effective, low-frequency clock references. On-chip clock synthesis is performed to meet compliance with the bit error rate (BER) requirement of associated ANSI, Bellcore and ITU-T standards.

The 88X2040 supports pre-emphasis on the serial driver to compensate for losses in copper environment.

Marvell Alaska 88X2040 Features

- IEEE 802.3ae/10GFC compliant Quad 3.125 Gbps/lane transceiver
- Supports IEEE 802.3ae/10GFC XGMII parallel interface
- Supports IEEE 802.3ae/10GFC XAUI serial interface
- Allows maximum 20 Gbps full-duplex data throughput
- On-chip 8b10b Encoding/Decoding (ENDEC)
- On-chip Time Base Generator
- Elastic buffering
- Supports pre-emphasis on the serial driver
- On-chip 50-ohm serial receiver termination
- IEEE 1149.1 JTAG test interface
- 1.5V, 3.3V and 1.8V power supplies
- 1.5V or 1.8V HSTL I/O
- Selectable 62.5 MHz, 125 MHz, or 156.25/159.375 MHz reference clock input
- Exceeds IEEE 802.3ae jitter requirement
- Advance 0.15 µm digital CMOS process

Test Equipment

The equipment used in the interoperability test is described below.

Marvell 88X2040 SMA to XGMII Evaluation Board

The 88X2040 is a quad 3.125 Gbps transceiver which serializes XGMII signals and de-serializes XAUI signals. On the 88X2040 board, the XGMII signals are looped back from the receive side to the transmit side and the XAUI signals are connected to SMA connectors. This evaluation board is designed to use the internal packet generator and receive packet counters to evaluate the transceiver.

The board includes:

- The capability to use an on-board 156.25 MHz oscillator clock source or an external source from an SMA input
- MDIO/MDC monitoring/control to both devices
- Eight Transmit SMAs and eight Receive SMAs for access to the 88X2040 SERDES.

Marvell Alaska X 88X2040 Software

The Alaska X 88X2040 software GUI controls the 88X2040 devices and monitors status bits through MDIO/MDC.

The GUI is sub-divided into several sections.

Rate and Pattern Section

- The reference clock is set to 156.25 MHz
- Speed is set to 3.125 Gbps (XAUI rate per channel)
- Either CJPAT or CRPAT can be selected for test pattern

Pattern Generator Section

- Selecting the TX button transmits the above selected pattern to the SERDES outputs. The Packet Transmitted counter keeps track of the number of packets transmitted.
- De-selecting the TX button puts the 88X2040 board in external loopback mode. In this mode, the pattern at the XGMII RX side is looped back to the XGMII TX side and sent to the SERDES SMA outputs.
- Selecting the RX enables the RX counters to count the number and rate of Good and Error received packets (of the selected pattern).

Pre-Emphasis and Amplitude Control Section

This section provides amplitude and pre-emphasis control for all four XAUI SERDES channels.

Link Status Section

This section provides information on the status of the XAUI link. For proper linking, the individual Lane Sync indicators for all four channels, as well as the Aligned and Link indicators should all be green.

LatticeECP3 Serial Protocol Evaluation Board

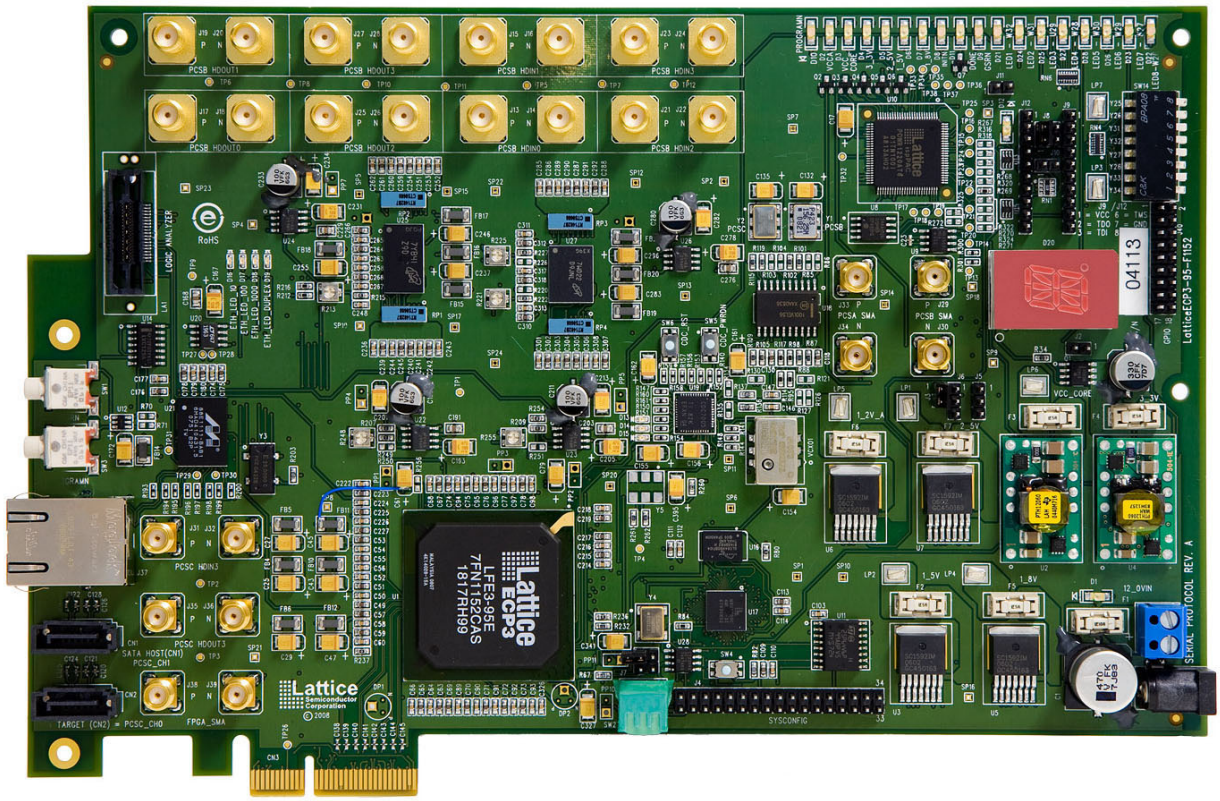
The LatticeECP3 Serial Protocol Evaluation board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeECP3 SERDES and FPGA, or aid in the development of custom designs. The LatticeECP3 Serial Protocol Evaluation Board features:

- PCI Express x4 edge connector interfaces
  - Allow demonstration of PCI Express (x4) interfaces
  - x4 is non-compliant but will demonstrate x4 functionality with an open-frame motherboard
- Allow control of SERDES PCS registers using the Serial Client Interface (ORCAstra)
- Serial ATA interfaces for host and target configurations
- RJ45 interface to 10/100/1000 Ethernet
- On-board Boot Flash.
  - 64M Serial SPI Flash
  - Parallel Flash via MachXO™ Crossover PLD programming bridge
- DDR2 and DDR3 memory components
- Switches, LEDs, displays for demo purposes
- Several debug and analysis connections

- Input connection for lab-power supply
- Power connections and power sources
- ispVM™ programming support
- On-board and external reference clock sources

Figure 2 shows the LatticeECP3 Serial Protocol Evaluation board.

Figure 2. LatticeECP3 Serial Protocol Evaluation Board



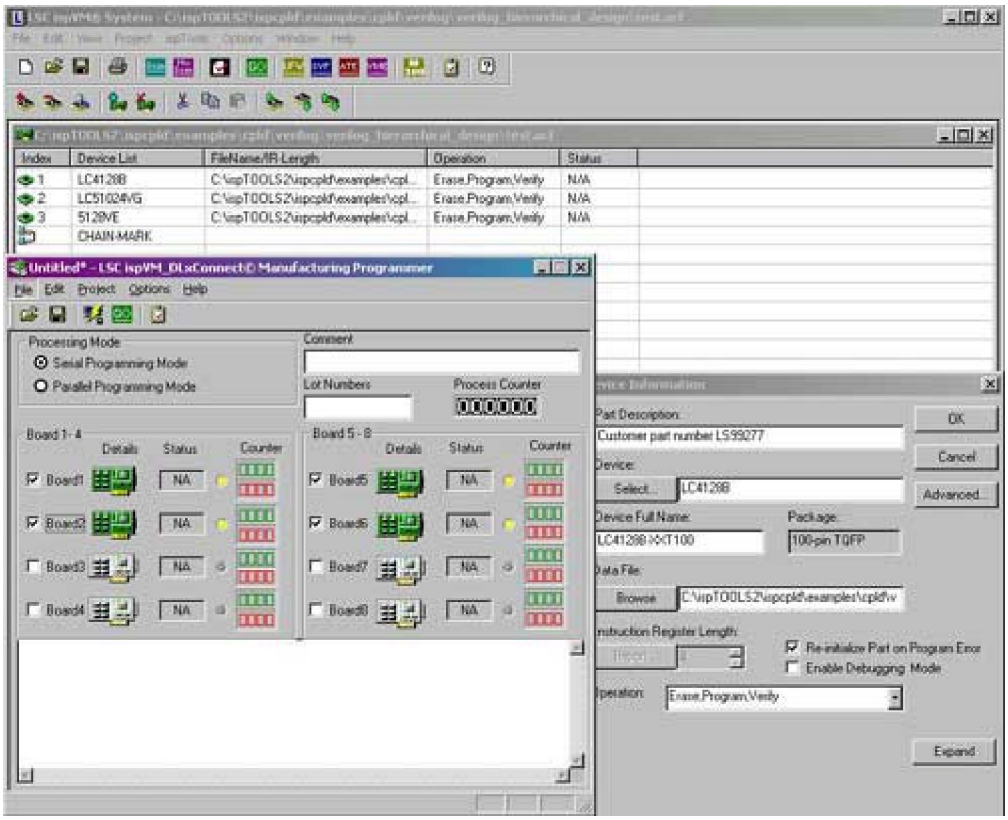
ispVM System

The ispVM System, included with the Lattice ispLEVER® software, is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming in-system programmable devices using JEDEC and bitstream files generated by Lattice, and other, design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM System is used in this interoperability test to download the LatticeECP3 bitstream, which configures the device in 10-gigabit Ethernet mode (XAUI).

Figure 3 shows a screen shot of the ispVM System.

Figure 3. ispVM System



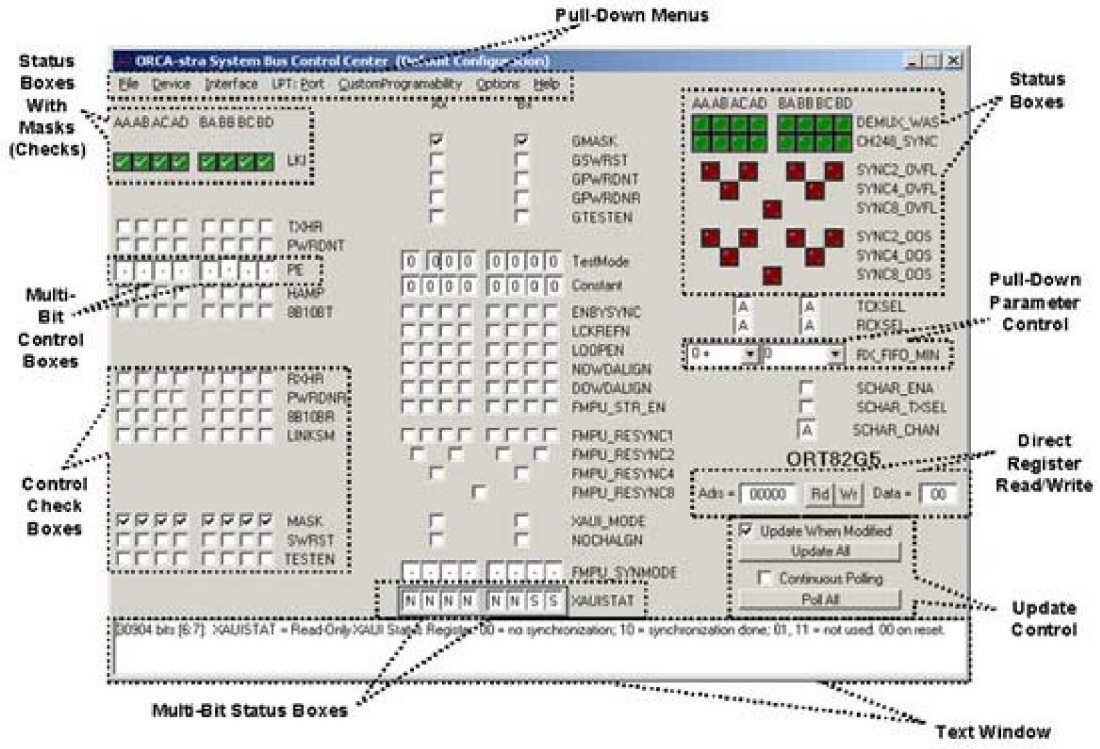
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface for configuring the operational mode of an FPGA by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to their board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the LatticeECP3.

Figure 4 is a screen shot of ORCAstra system

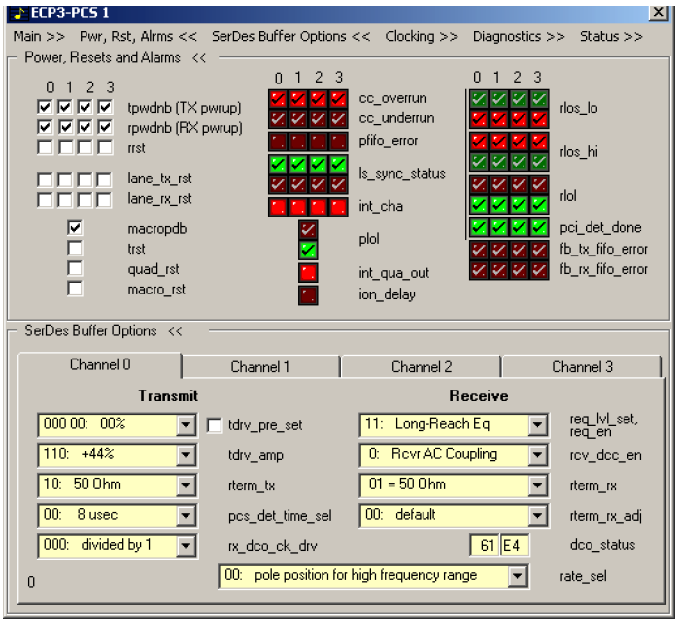
Figure 4. ORCAstra System



LatticeECP3 PCS ORCAstra View

The LatticeECP3 PCS ORCAstra window allows access to the PCS internal registers. Two important sections of this window are the Power, Reset and Alarms view and the SerDes Buffer Options View. Both views are shown in Figure 5.

Figure 5. LatticeECP3 PCS ORCAstra View



Power, Reset and Alarms: The default Power, Resets and Alarms section contains the following important information:

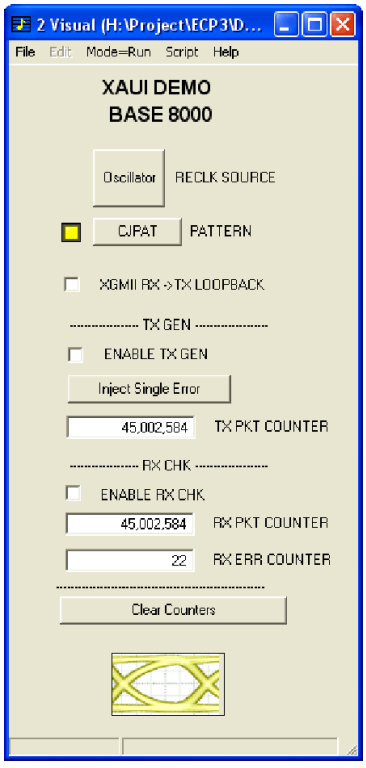
- Green/red LEDs (one per channel) to indicate that the receive link state machines are synchronized (ls_sync_status). Green indicates successful synchronization.
- Green/red LEDs (one for whole quad) to indicate that the SERDES transmit PLL (plol) is locking. Green indicates successful lock.
- Green/red LEDs (one per channel) to indicate Receive CDR lock (rlol). Green indicates successful lock.

This view also allows the user to identify which channels (or the entire quad), are powered down or reset. This view also allows users to reset PCS digital logic (lane_tx_rst and lane_rx_rst), as well as SERDES logic (macro_rst) and the whole quad (quad_rst).

SerDes Buffer Options View: This view allows controlling the characteristics of output, input, and reference clock buffers: TX pre-emphasis, TX amplitude, RX equalization, TX and RX buffer termination and coupling.

XAUI Generator/Checker ORCAstra GUI
The LatticeECP3 XAUI reference design utilizes a visual window as a plug-in to the base ORCAstra installation Figure 6 provides a screen capture of this window.

Figure 6. XAUI Generator/Checker ORCAstra Plug-in Visual Window



The following is a description of the control and status elements for the visual window.

REFCLK SOURCE: This button allows the user to select either the internal differential oscillator or the external SMA differential inputs as the source of the refclkp/n to the PCS SERDES.

XGMII RX->TX LOOPBACK: The logic allows the XGMII RX data at the XAUI PCS soft IP interface to be looped-back in the TX direction. This allows the XAUI PCS reference design to act as a DUT type #2 device as described by the IEEE 802.3ae-2002 specification.

PATTERN: This button allows the user to select either CRPAT or CJPAT. There is also a yellow LED to the left of the button that glows when CJPAT is selected.

ENABLE TX: When checked, it enables the transmission of XAUI (CJPAT or CRPAT depending on what the PATTERN button is set to) packets from the generator.

ENABLE RX: When checked, it enables the detection of errors (CJPAT or CRPAT depending on how the PATTERN button is set) by the checker of the XAUI quad.

TX PKT COUNTER: The TX PACKET counter keeps count of the number of packets (CJPAT or CRPAT depending on how the PATTERN button is set) transmitted in the TX XGMII direction. The counter will count up as long as ENABLE TX is checked. Clicking on the Clear Counters button resets this counter. The counter is software-based. ORCAstra periodically loads a snapshot of the TX PKT counter (tx_pkt_counter_snap) into a software accumulator. The software accumulator value is displayed in the counter field.

RX PKT COUNTER: The RX PACKET counter keeps count of the number of packets (CJPAT or CRPAT depending on what the PATTERN button is set to) received by the checker in the RX XGMII direction. The counter will count up as long as ENABLE RX is checked and valid packets (with proper SOP and EOP) are received. Clicking on the Clear Counters button resets this counter. The counter is software-based. ORCAstra periodically loads a snapshot of the RX PKT counter (rx_pkt_counter_snap) into a software accumulator. The software accumulator value is displayed in the counter field.

RX ERR COUNTER: The RX ERR counter keeps count of the number of packets (CJPAT or CRPAT depending on how the PATTERN button is set) with one or more incorrect bytes received by the checker in the RX XGMII direction. The counter will count up as long as ENABLE RX is checked and valid packets (with proper SOP and EOP) are received. Clicking on the Clear Counters button resets this counter. The counter is software-based. ORCAstra periodically loads a snapshot of the RX ERROR counter (rx_error_counter_snap) into a software accumulator. The software accumulator value is displayed in the counter field.

Clear Counters: When checked, it asynchronously clears the content of the TX PKT, RX PKT, and RX ERR counters.

Inject Single Error: The TX generator inserts a single 64-byte data error when the Inject Single Error button is pushed. This will happen as long as ENABLE TX is checked. The incorrect DATA byte is inserted on the next CJPAT/CRPAT frame after the Inject Single Error is pushed.

Interoperability Testing

This section provides details on the XAUI interoperability test between the LatticeECP3 device and the Marvell 88X2040 device. The purpose of the test is to implement interoperability between one Type #1 DUT (LatticeECP3) and one Type #2 DUT (88X2040).

The test has the following characteristics:

- Independent (asynchronous) +/- 100 ppm clock sources clock the LatticeECP3 and 88X2040 devices. For these particular devices, the data rate across four lanes is 4*8/10*20*F, where F is the source clock frequency. The data rate in XAUI mode is 10 Gbps. This means an independent clock source of 156.25 MHz (+/- 100 ppm) or larger clocks each device.
- The LatticeECP3 device transmits CJPAT data to the 88X2040 device.
- The 88X2040 device loops the data at its XGMII interface back to the LatticeECP3 device.

By the end of the test:

- The 88X2040 device visual window RX ERR counter should remain at zero
- The LatticeECP3 device visual window RX ERR counter should remain at zero

- The LatticeECP3 device visual window counters should report as many TX packets generated as RX packets received
- The amount of test time should be longer than 30 minutes to ensure the error rate is less than 10-12 with 99.999999% accuracy.

XAUI Interoperability Hardware Test Setup

The setup includes:

- A Tyco Backplane (using the 16” HM-ZD slots)
- Marvell 88X2040 evaluation LB SMA board (with the 88X2040 devices)
- LatticeECP3 Serial Protocol Evaluation board with LFE3-95E 7FN1156CES part on a socket.
- One SMA to HM-ZD daughter card to go from the Marvell SMA connections to the Tyco HM-ZD slot
- One SMA to HM-ZD daughter card to go from the LatticeECP3 SMA connections to the Tyco HM-ZD slot
- A PC for software control/monitoring
- On-board 156.25 MHz differential LVDS clock oscillator to provide the reference clock to the LatticeECP3 PCS/SERDES quad. The Marvell 88X2040 board also contains a built-in oscillator.
- About 24” of SMA cable to connect the Marvell board to its daughter card
- About 24” of SMA cable to connect the LatticeECP3 board to its daughter card

Figure 7 shows the Marvell 88X2040 board, the LatticeECP3 board, and the Tyco backplane connections.

Figure 8 is a block diagram of the test setup.

Figure 7. Board Connections

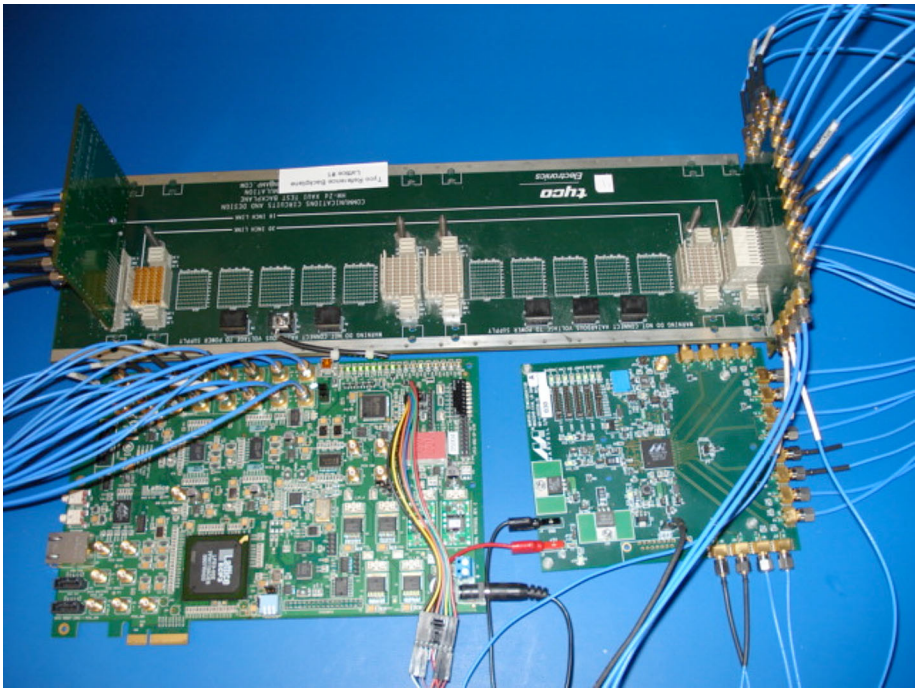
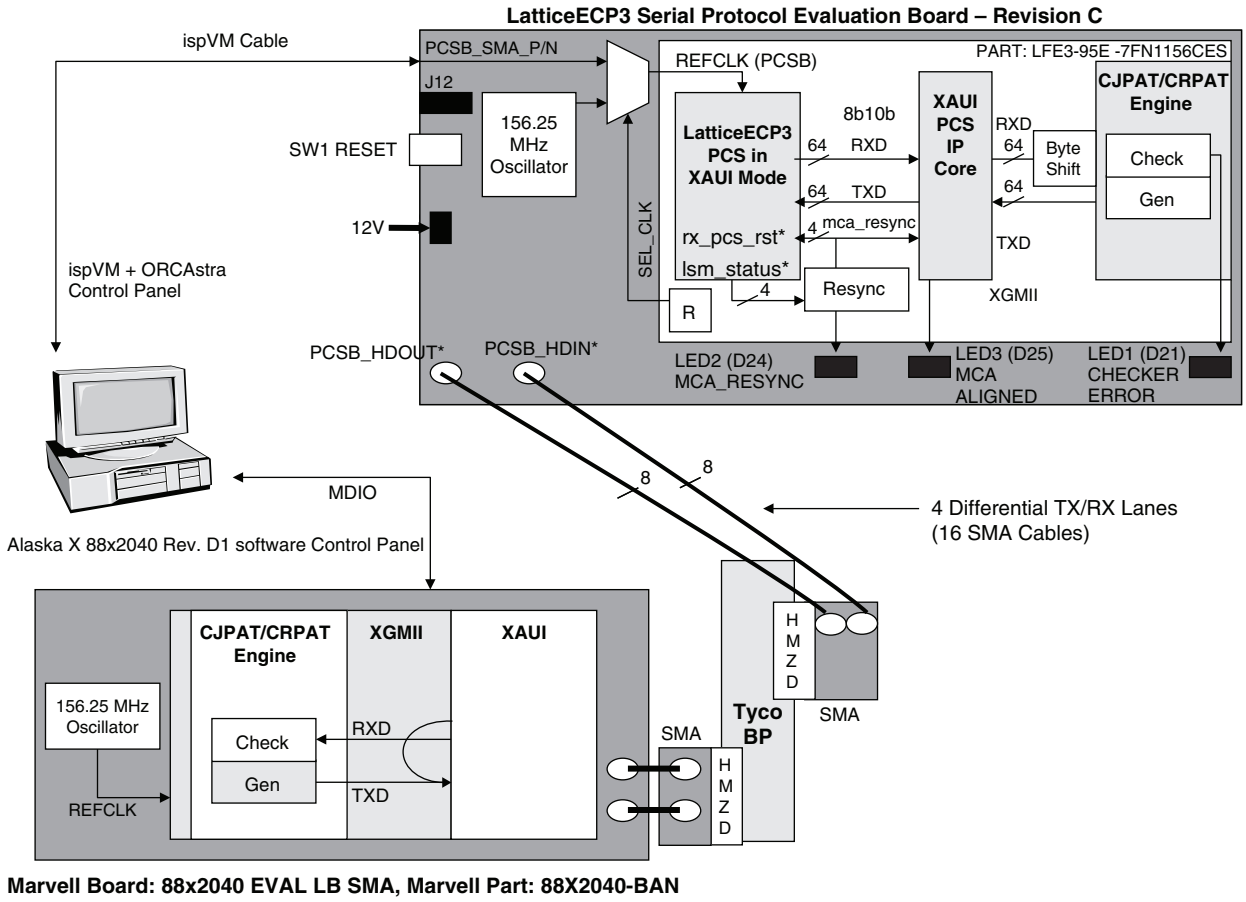


Figure 8. Test Setup Block Diagram



Marvell Board: 88x2040 EVAL LB SMA, Marvell Part: 88X2040-BAN

Test Description

This section describes how each interoperability partner is set up for 10-gigabit Ethernet physical layer interoperability.

Marvell 88X2040 Board

The built-in 156.25 MHz clock oscillator sources the Marvell 88X2040 reference clock for XAUI. The reference clock is multiplied internally by 20 to achieve a 10 Gbps data rate (12.5 Gbps aggregated rate). The Marvell 88X2040 checks full protocol-compliant 10-gigabit Ethernet (10 Gbps) CJPAT packets at the XGMII interface. The 88X2040 also loops back the XGMII data back into the TX direction. The 88X2040 device then transmits the packets back to the LatticeECP3 device.

LatticeECP3 Serial Protocol Evaluation Board

The internal 156.25 MHz clock oscillator sources the LatticeECP3 PCS reference clock to the PCS/SERDES quad. The reference clock is multiplied internally by 20 to achieve a 10 Gbps data rate (12.5 Gbps aggregated rate).

The LatticeECP3 XAUI generator transmits CJPAT packets through the XAUI PCS soft IP and the LatticeECP3 XAUI PCS to the Marvell 88X2040 device.

In the RX direction, The LatticeECP3 SERDES recovers the packets from the Marvell 88X2040 device and the XAUI IP converts them into XGMII format. The XAUI checker then checks the received patterns.

I/O Software Configurations

The following describes how SERDES buffers parameters were set to achieve error-free XAUI interoperability across the SMA link and the 16” of FR-4 backplane material.

- **LatticeECP3 SERDES Buffer Settings:** The LatticeECP3 SERDES buffers on all channels were set identically to the SerDes Buffer Options view of the LatticeECP3 PCS1 XAUI visual window shown in Figure 5.
- **88X2040 Buffer Settings:** The Marvell 88X2040 buffer settings were the following: Pre-emphasis set to 67%, and Amplitude set to 3/4 of MAX. These settings were identical on all channels.

Results

The setup ran for about one hour and 40 minutes. Throughout the test, the Lattice/Marvell RX error counters remained at zero. At the end of the test, the LatticeECP3 XAUI Generator/Checker TX and Rx packet counter were identical in value. There were a total of 4,958,904,946 packets transferred across the system.

Summary

In conclusion, the LatticeECP3 FPGA family is fully XAUI interoperable with the Marvell 88X2040 device.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
June 2009	01.0	Initial release.
February 2012	01.1	Updated document with new corporate logo.