PRELIMINARY

Embedded Sensor Setup and Imaging Pipeline (monochrome)

for Aptina MT9V022, -V023, -V024 -V032, -V033, -V034

ver 1.0

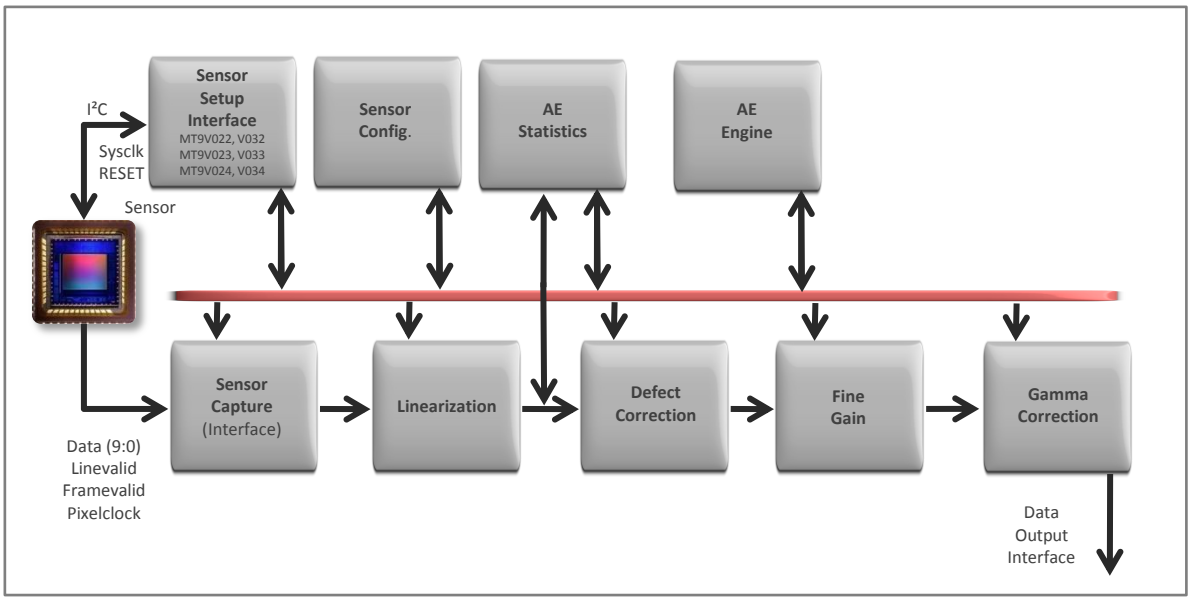
OVERVIEW

Helion's experience in image processing enables camera designers to use pre-engineered high quality algorithms directly on their camera system.

KEY FEATURES

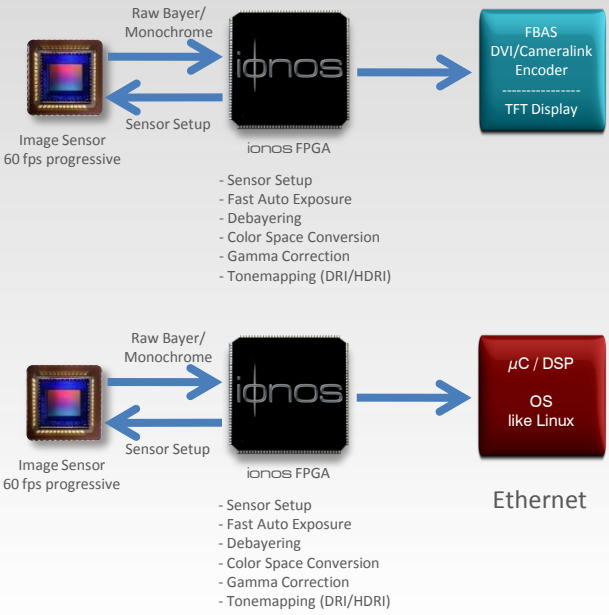
- Fast auto exposure with antiflicker and ROI support
- Fast automatic image sensor setup
- Automatic gain control
- Noise reduction for low light conditions
- Gamma correction
- True 72dB DR support
- APIX Transmit Interface with APIX setup
- Output interface for DSP with FiFo
- Output interface for CMOS/TTL TFT panel
- Parameter inserting
- Testpattern generator
- Overlay with graphical bitmap objects
- I²C configuration

BLOCK DIAGRAM



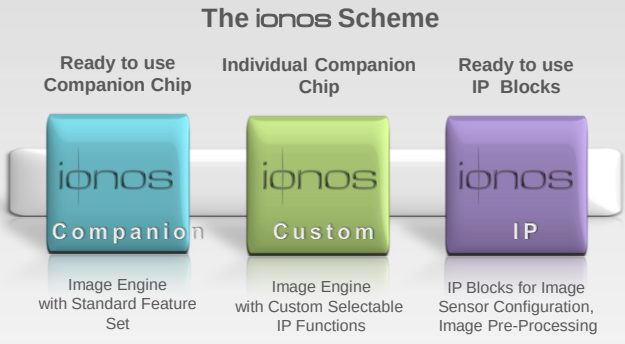
APPLICATION

- Image pre- and post-processing
- Image sensor control
- FPGA algorithms
- DSP algorithms



LICENSING

The flexibilty of the ionos concept allows fast and at the same time cost-effective camera designs. The creation of an image sensor signal chain can easily be achieved by Helion's ionos-IP. Camera designers can choose ionos IP-blocks from the IP-Pool for customized applications.



DELIVERABLES

- Encrypted, or plain text EDIF netlist
- Active-HDL automatic simulation macros
- Test with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support (optional)
  - IP Core implementation support
  - 3 month maintenance
    - Deliver the IP Core updates, minor or major version changes
    - Delivery the documentation updates
    - Email support

PERFORMANCE

Device	Slices	EBR	MULT	Max. Pixelclock
XP2	2869	13	1x 36x36 1x 18x18	42 MHz