Using a Discrete Crystal as a PLD Clock Source

Application Note

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1. Introduction

Clocks are a necessary part of synchronous PLD designs (e.g. Lattice Semiconductor's ispMACH® 4000ZE and MachXO™). Designers will typically use integrated oscillators but there are other, less expensive options. This document will discuss the generation of a clock signal using an inexpensive crystal circuit to minimize board costs.

2. The Crystal Oscillator Circuit

Discrete crystals are two terminal passive devices that are made from a piezoelectric material. Circuits that use crystals as part of the feedback path are known as crystal oscillator circuits. Crystal oscillator circuits oscillate at a specific frequency that is based upon the mechanical resonance of the crystal device. Figure 2.1. shows an example of a crystal device (a), the crystal schematic symbol (b), and the electrical equivalent of a crystal (c).

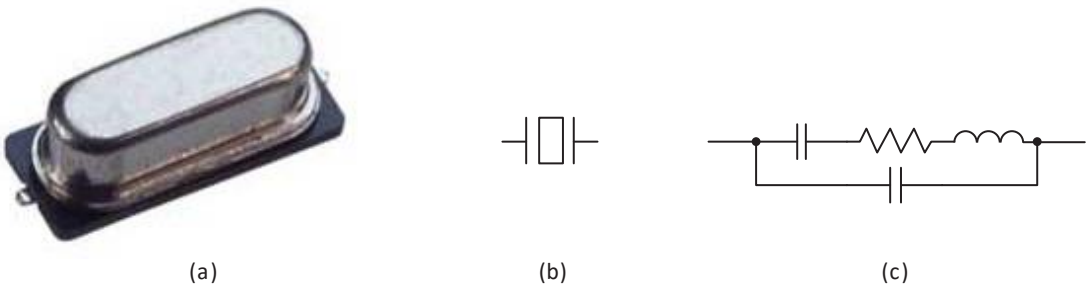

Figure 2.1. Crystal (a) Device, (b) Symbol, (c) Electrical Equivalent

Crystals are specified to operate at a given frequency and in a given mode. The basic mode of operation is referred to as the fundamental mode and is available in frequencies that range from about 30 kHz to 50 MHz. To obtain higher frequencies a crystal is specified to operate in a 3rd or 5th overtone mode which is close in frequency to the 3rd and 5th harmonic of the fundamental frequency (operating at exact multiples is less stable because, the crystal will prefer the fundamental mode). Overtone crystal oscillator circuits are significantly more complex, more sensitive to component variations, and not recommended for use with a PLD. Therefore, the first step in designing a crystal oscillator with a PLD is to select a crystal with the desired fundamental frequency.

To operate a crystal at the fundamental frequency, the Pierce circuit can be realized using an inverter inside a PLD combined with some external resistors and capacitors as shown in

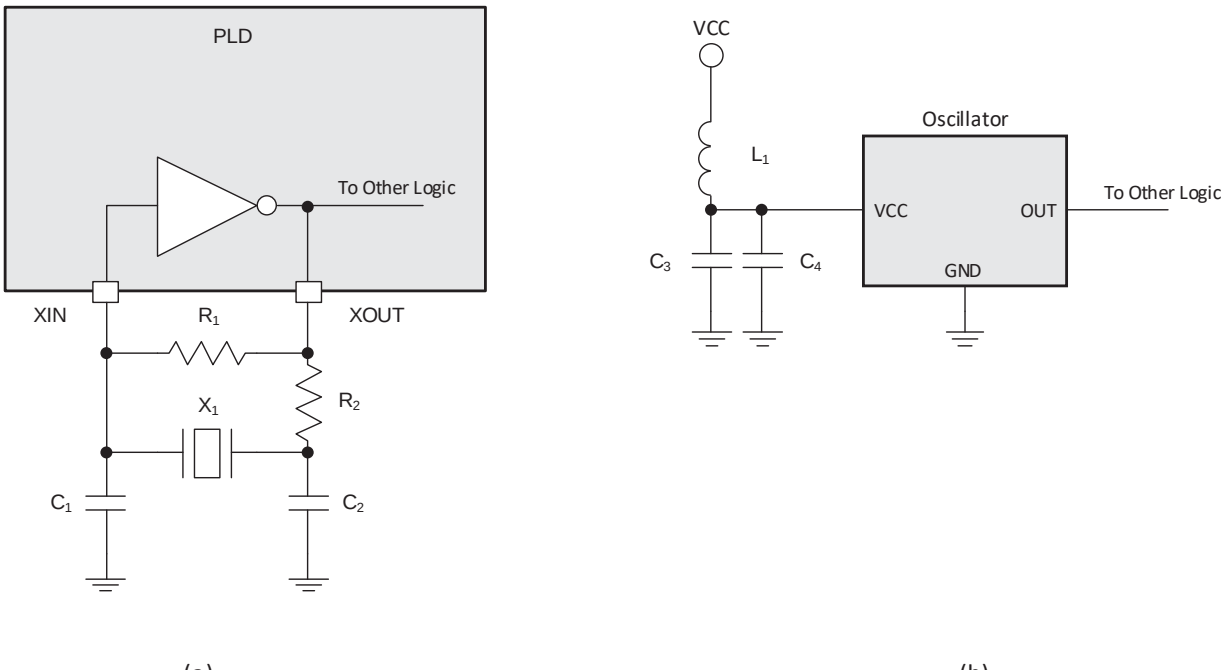

Figure 2.2. (a). Typically this type of oscillator circuit is built with a series of three inverters to provide enough phase delay for oscillation to take place. However, this in not required when using Lattice Semiconductor PLDs. The input buffer and output buffer (not shown) provide enough delay that a single inverter is all that is needed for the oscillator circuit to function. The two capacitors C1 and C2 are part of the load capacitance (CL) which is specified in the crystal data sheet. The resistor R1 is part of feedback path while R2 limits the drive power seen by the crystal. Crystal manufactures usually provide documentation with recommended values for the resistors and capacitors.

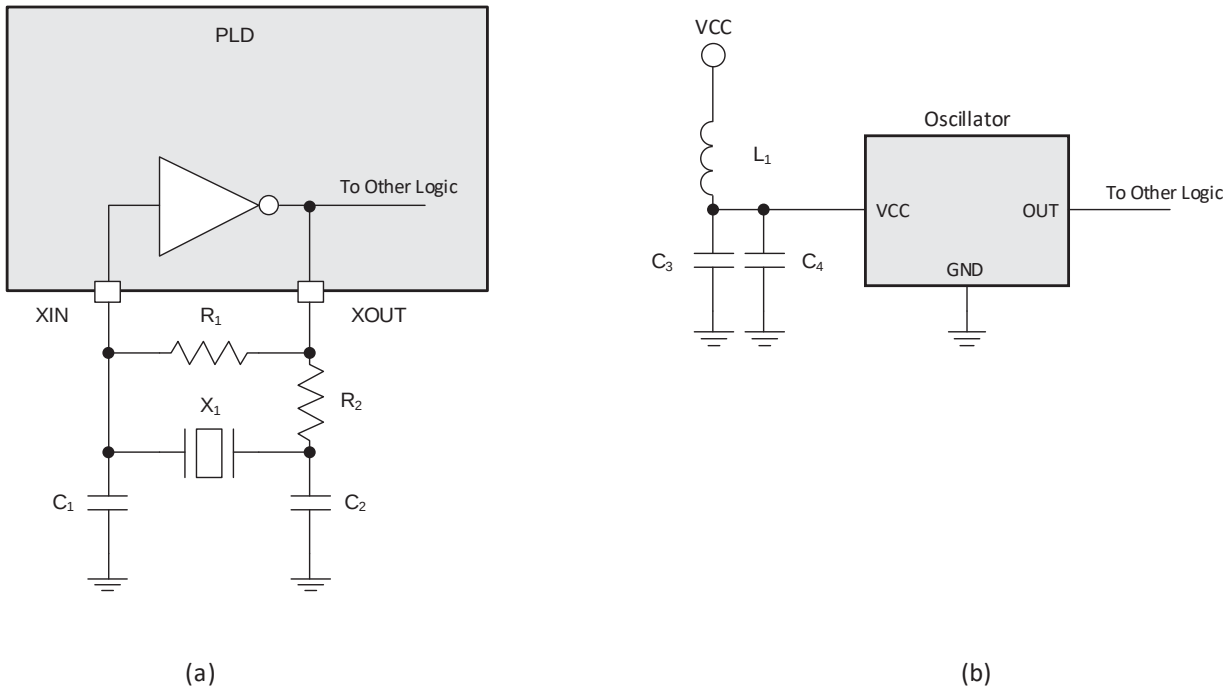

Figure 2.2. Oscillator Circuit using an Inverter within a PLD (a) vs. Integrated Oscillator (b)

3. Comparing Crystal/Pierce Circuit vs. Oscillator

The fundamental advantage of using a discrete crystal as a clock source rather than an integrated oscillator is lower board cost. The Pierce circuit does, however, require extra passive components, which will slightly increase design and assembly effort. The tradeoffs are shown in Table 3.1.

Table 3.1. Comparing Crystal/Pierce Solution vs. Oscillator

	Crystal/Pierce	Oscillator
Approximate cost*	$0.30 to $0.80	$1.80 to $3.00
Design effort	Pierce circuit must be designed	Minimal / none
Component count	5 (crystal, 2 resistors, 2 capacitors)	4 (oscillator, 1 ferrite, 2 bypass capacitors)
Lab testing	Pierce circuit must be verified	Minimal / none
Jitter	Affected by PLD logic and I/O	Not affected by PLD logic and I/O
Frequencies available	~30 kHz to 50 MHz	1 MHz to 250 MHz

***Note**: Based on 2009 component costs.

4. Pierce Circuit Crystal Components Selection

The first step in designing the Pierce oscillator circuit is selecting the crystal (X_1) based upon the required clock frequency supported by the fundamental mode of operation. Further consideration would be given to package size and parts cost.

The crystal data sheet will specify the load capacitance (C_L). The load capacitance is the total capacitance which will be seen on either side of the crystal. Based on the circuit shown in

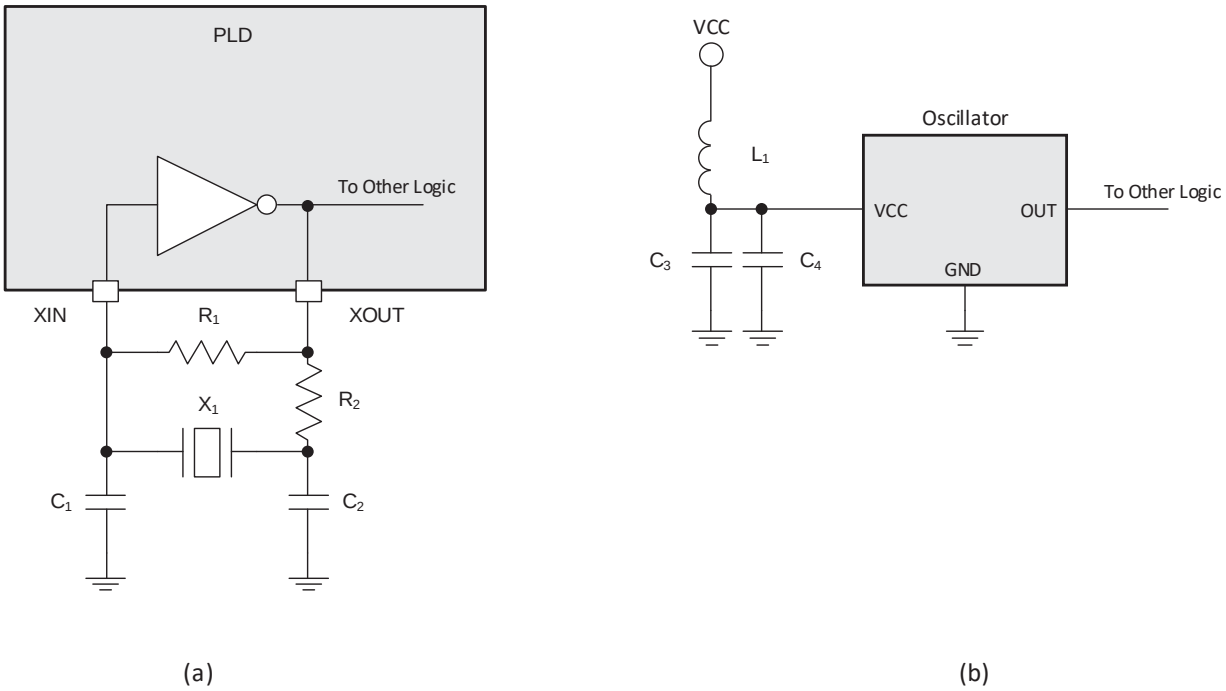

Figure 2.2. (a), the ideal calculation for (C_1) and (C_2) is:

$$CL = \frac{C1 \text{ X } C2}{C1 + C2} + C_{STRAY} \quad (1)$$

Where C_{Stray} is the stray capacitance around the crystal such as: PLD input and output capacitance, the crystal mounting pads, mounting pads of the resistors, and PCB trace capacitance (listed in order of significance). In equation form, this would look like:

$$C_{STRAY} = C_{PLD\_IO\_BUFFER} + C_{CRYSTAL\_PAD} + C_{R\_PAD} + C_{BOARD\_TRACES} \quad (2)$$

In order of significance this equation is broken down as follows: where $C_{PLD\_IO\_BUFFER}$ is the input and output capacitance of the PLD buffer. The output capacitance is only included if the value of R_2 is near zero ohms. These values can be found in the PLD manufacturer's data sheet.

$C_{CRYSTAL\_PAD}$ is the capacitance value associated with the PCB mounting pad of the crystal. This capacitance can be calculated using the following equation where A is the area of the pad (in square inches), d is the thickness of the board (in inches) between the pad and the ground plane (or power plane, which ever is closer), and ε is the dielectric constant of the PCB material. Some typical mounting pad capacitance values are presented in Appendix A.

$$C_{CRYSTAL\_PAD} = \frac{0.224 \text{ X } \varepsilon \text{ X } A}{d} \quad (3)$$

C_{R_PAD} is the capacitance value associated with the PCB mounting pads of R_1 and R_2. This capacitance can be calculated using the same equation that was used for the crystal mounting pads. Typically the capacitance value for surface mount 0805 or 0603 devices is significantly less than the capacitance value of either the PLD I/O or the crystal mounting pad and can be ignored in most cases.

C_{BOARD_TRACES} is the capacitance associated with the traces that connect the crystal to the resistors, capacitors, and PLD pins. All the components should be placed as close to the PLD as possible for two reasons. First, so that the trace capacitance value can be estimated to be zero and thus ignored. Secondly, and more importantly, so that the circuit is protected from surrounding signals that may affect the operation of the crystal oscillator.

The Pierce circuit is fairly robust when using a fundamental mode crystal. As a result, the values of C_1 and C_2 are often selected to be the same since this simplifies assembly and reduces inventory costs.

5. Precautions and Rules of Thumb

When implementing a crystal/Pierce circuit there are some precautions and rules of thumb to be aware of:

- Always select a crystal that is specified to operate in fundamental mode.
- Always refer to the crystal manufacturer data sheets and technical notes to optimize and revise the component values of the oscillator circuit.
- When laying out the board use routing and Via keepouts to prevent stray signals from running under of near the crystal circuit which may affect the performance of the oscillator circuit.
- To help isolate the crystal circuit, enclose it with a ground guard ring.
- Place the crystal circuit as close to the PLD as possible to reduce stray capacitance (by minimizing trace lengths).
- Provide a clean, quiet, and stable power supply for the VCCIO bank that contain XIN and XOUT pins to minimize jitter.
- When assigning pins in the PLD design flow, place XIN and XOUT so that both are as close to the crystal as possible.
- When assigning pins in the PLD design flow, isolate XIN and XOUT to a bank that does not have a lot of other I/O activity to minimize jitter.
- Configure the PLD I/O pull mode to OFF for XIN and XOUT or the circuit may not start.
- Test the circuit across temperature to ensure functionality.
- Since the XIN and XOUT pins are not specifically designed as analog crystal interface pins, this application may have accuracy and jitter issues that might be unsuitable as a reference clock for high speed applications, such as Ethernet or USB.

6. Pulling It All Together

The recommended implementation steps for a proper crystal/PLD Pierce circuit are as follows:

1. Specify PLD pins (XIN, XOUT) based upon the recommended rules of thumb.
2. Select a crystal based upon its fundamental frequency.
3. Design the Pierce circuit per the defined capacitance calculations assuming:
   a. $C_1 = C_2$
   b. Assume C_{BOARD_TRACES} and C_{R_PAD} to be 0 pF.
   c. Select resistor R_1 and R_2 values based upon crystal manufacturer recommendations.
   d. Check crystal manufacturer datasheets and technical notes for further refinements of the Pierce circuit.
4. Design the board, rigorously following the defined rules of thumb.
5. Lab test the circuit across temperature range to ensure reliable crystal operation. If necessary, revise the values of C_1 and C_2 until the Pierce circuit yields desired operation. If C_L is too little or too much, the frequency of oscillation may be low or high respectively.

7. Summary

Crystals are a low-cost and accurate clocking alternative that can be used in a number of state machine and PWM applications. Crystals are available in frequencies from 30 kHz to 50 MHz using the fundamental resonant frequency. A Pierce circuit is recommended for crystal implementation, due to its simplicity, low cost, and robustness. The designer should use the C_L formulas and rules of thumb to specify initial values for C_1 and C_2 and use bench testing to finalize these values. Due to potential jitter issues, an external crystal is not recommended as a reference clock for high speed applications such as data sampling, Ethernet, or USB.

Appendix A. Example Calculation

This example calculation is based on the MachXO Mini Evaluation Board. The Citizen HCM49 crystal is available at 25 MHz in Fundamental mode. The "Reference for Selecting Constants of Oscillation Circuit" technical note from Citizen Crystal lists the values as follows:

R_1 = 1 MΩ

R_2 = 1 kΩ

C_1 = 18 pF

C_2 = 18 pF

C_L = 16 pF

The dielectric constant for FR4 is about 4.5 and the recommended mounting pads for the HCM49 are 5.5 mm by 1.5 mm. In a typical 4-layer circuit board, the thickness of the dielectric from the top layer to the ground plane layer is 0.0115 inches. This results in a crystal mounting pad capacitance of 1.1 pF (for each pad). The PLD input capacitance from the MachXO Family Data Sheet is typically 8 pF. The PLD output capacitance is ignored as it is isolated from the crystal by R_2. Setting C_1 equal to C_2 and using the values above results in the following:

$$16 \text{ pF} = \frac{C2}{(2C)} + 10.2 \text{ pf} \quad (4)$$

Solving this equation; we find C = 11.6 pF, so we can use a standard value of 12 pF for both C_1 and C_2.

If we now change the design to use a 6-layer circuit board the dielectric thickness drops to 0.0064" (almost half). This results in the crystal mounting pad capacitance of 2.0 pF (almost double) per pad. Solving again, we find that C = 8 pF for both C_1 and C_2.

Related Literature

- MachXO Family Data Sheet (FPGA-DS-02071)
- ispMACH 4000ZE Family Data Sheet

References

- Citizen HCM49 data sheet (used on the MachXO Mini Evaluation Board) available on the Citizen Crystal web site at www.citizencrystal.com
- Citizen crystal design technical note, “Precautions in Oscillation Circuit Design” available on the Citizen Crystal web site at www.citizencrystal.com
- Citizen crystal design technical note, “Reference for Selecting Constants of Oscillation Circuit” available on the Citizen Crystal web site at www.citizencrystal.com
- The ARRL Handbook, available on the AARL web site at www.arrl.org

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Revision History

Revision 1.1, November 2020

Section	Change Summary
All	• Changed document number from AN8080 to FPGA-AN-02016. • Updated document template.
Disclaimers	Added this section.
Pierce Circuit Crystal Components Selection	Added footnote and Jitter row to Table 3.1. Comparing Crystal/Pierce Solution vs. Oscillator.
Precautions and Rules of Thumb	Added items regarding jitter and applications.
Summary	Clarified applications.

Revision 1.0, June 2009

Section	Change Summary
All	Initial release.

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