Tri-Rate SMPTE SDI Demo

User's Guide

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Introduction

Video and television technology has been migrating from analog to digital over the past two decades. The technology used for transmitting data between digital systems has also been migrating from parallel to high-speed serial over the past decade. The SDI video standard is an uncompressed digital video standard that transmits high speed serial video stream through a coaxial cable.

Once video is captured by a professional video camera, no matter if it is pre-stored in a media or not, it must go through a few broadcasting systems before reaching consumers. SD-SDI, HD-SDI and 3G-SDI are common video standards used in these professional/broadcasting systems. With SDI, the high resolution video stream can be transmitted through a 75 Ohm coaxial cable for as long as several hundreds meters.

This user's guide shows the capability of the LatticeECP3™ SERDES with an SD/HD/3G design example. The design is implemented using the LatticeECP3 Video Protocol Board. It includes a pattern generator and a pattern checker along with the Lattice's Tri-Rate SDI PHY IP core. The IP core supports automatic detection between three video standards: 270 Mbps SD-SDI, 1.485 Gbps HD-SDI and 2.97 Gbps 3G-SDI.

Features

- Supports two SD-SDI formats, eight HD-SDI formats and twenty-two 3G-SDI formats
- Supports video formats with fractional frame rate (M factor = 1.001)
- Automatic detection between different video formats with the tri-rate feature of the IP core
- Color adjustment function for tuning Contrast/Brightness/Hue/Saturation in Pass-Through mode
- Color bars generation supports three types of color bars: SMPTE color bars, 75% color bars and 100% color bars
- Pathological signal analysis with three different test patterns: Matrix SDI check-field, EQU SDI check-field and PLL SDI check-field
- 16-segment LED for displaying which pathological patterns the generator and the checker is currently using
- Built-in pattern checker for tests with color bar patterns or pathological signal patterns using single or multiple boards
- Detailed pattern-checking errors reported through a UART port for capturing overnight test results (RS-232 port set to 115200, 8, 1, N)
- Character LCD module for displaying Rx/Tx status, video standards, current operational mode, Contrast/Brightness/Hue/Saturation values and control settings
- Seamless switching between video standards that guarantees the switching is between frame boundaries

Functional Description

This design supports two operational modes, Pass-Through mode and Pattern-Generation mode. The mode switching and the controls of these two modes are done by the on-board switch and push-buttons.

When in Pass-Through mode, the serial video stream is received, descrambled and word-aligned by the IP core receiver. Then, the Contrast/Brightness/Hue/Saturation adjustment module can optionally process the received parallel video data. Finally, the parallel video data is sent to the IP core transmitter for data scrambling, line number insertion and CRC insertion before being sent out.

When in Pattern-Generation mode, an internal pattern generator will generate patterns for the IP core transmitter to send out color bars or pathological signals. The receiver can also be enabled in this mode for comparing the received video data with an internal pattern checker. The comparison errors will be sent out through a UART/RS-232 port and captured into a PC text file. A typical application is to generate test patterns and loop them back exter-

nally through an SDI cable to the checker. The test patterns can be pathological test patterns for EQU/PLL tests or simply color bar patterns through a very long SDI cable.

The video standards supported by the Tri-Rate SDI PHY IP core are all implemented in this design which include the two SD standards, the eight HD standards and the 22 3G-SDI standards listed in Tables 1 to 3.

Table 1. Supported Video Formats and Corresponding Switch Settings

Standard	SD-SDI		HD-SDI							
Bit Rate	270Mbps		1.485Gbps/M							
Serial SMPTE Standard	259M		292M							
Parallel SMPTE Standard	125M		260M	295M	274M					296M
SW4[3]	0	0	0	0	0	0	0	0	0	0
SW3[1:4]	0xx0	0xx1	1000	1001	1010	1011	1100	1101	1110	1111
Total words per line	1716	1728	2200	2376	2200	2200	2640	2640	2750	1650
Total lines per frame	525	625	1125	1250	1125	1125	1125	1125	1125	750
Active words per active line	720	720	1920	1920	1920	1920	1920	1920	1920	1280
Active lines per frame	487i	576i	1035i	1080i	1080p	1080i	1080p	1080i	1080p	720p
Frame rate (Hz)	29.97	25	30/M	25	30/M	30/M	25	25	24/M	60/M
Fields per frame	2	2	2	2	1	2	1	2	1	1
Bits per word	10	10	20	20	20	20	20	20	20	20
Word rate (MHz)	27	27	74.25/M	74.25	74.25/M	74.25/M	74.25	74.25	74.25/M	74.25/M
Pixel sample rate (MHz)	13.5	13.5	74.25/M	74.25	74.25/M	74.25/M	74.25	74.25	74.25/M	74.25/M
Sampling structure	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2
Pixel depth	10	10	10	10	10	10	10	10	10	10

Note: In Pattern-Gen mode, the factor M is 1 for video formats with integer frame rate formats and 1.001 is for video formats with fractional frame rates. This factor is selected by SW1-2.

Table 2. Supported Video Formats and Corresponding Switch Settings (3G-SDI Part 1)

Standard	3G-SDI											
Bit Rate	2.97Gbps/M											
Serial SMPTE Standard	SMPTE 425M 3Gb/s Mapping, SMPTE 424M 3Gb/s serial interface											
Parallel SMPTE Standard	274M		296M		274M	296M	274M	296M	274M	296M	274M	
SW4[3]	1	1	1	1	1	1	1	1	1	1	1	1
SW3[2:4],SW4[1:2]	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011
Total words per line	2200	2640	1650	1980	2200	3300	2640	3960	2750	4125	2200	2640
Total lines per frame	1125	1125	750	750	1125	750	1125	750	1125	750	1125	1125
Active words per active line	1920	1920	1280	1280	1920	1280	1920	1280	1920	1280	1920	1920
Active lines per frame	1080p	1080p	720p	720p	1080p	720p	1080p	720p	1080p	720p	1080i	1080i
Frame rate (Hz)	60/M	50	60/M	50	30/M	30/M	25	25	24/M	24/M	30/M	25
Fields per frame	1	1	1	1	1	1	1	1	1	1	2	2
Bits per word	20	20	20	20	20	20	20	20	20	20	20	20
Word rate (MHz)	148.5/M	148.5	148.5/M	148.5	148.5/M	148.5/M	148.5	148.5	148.5/M	148.5/M	148.5/M	148.5
Pixel sample rate (MHz)	148.5/M	148.5	148.5/M	148.5	148.5/M	148.5/M	148.5	148.5	148.5/M	148.5/M	148.5/M	148.5
Sampling structure	4:2:2	4:2:2	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4	4:4:4:4
Pixel depth	10	10	10	10	10	10	10	10	10	10	10	10

Note: In Pattern-Gen mode, the factor M is 1 for video formats with integer frame rate formats and 1.001 is for video formats with fractional frame rates. This factor is selected by SW1-2.

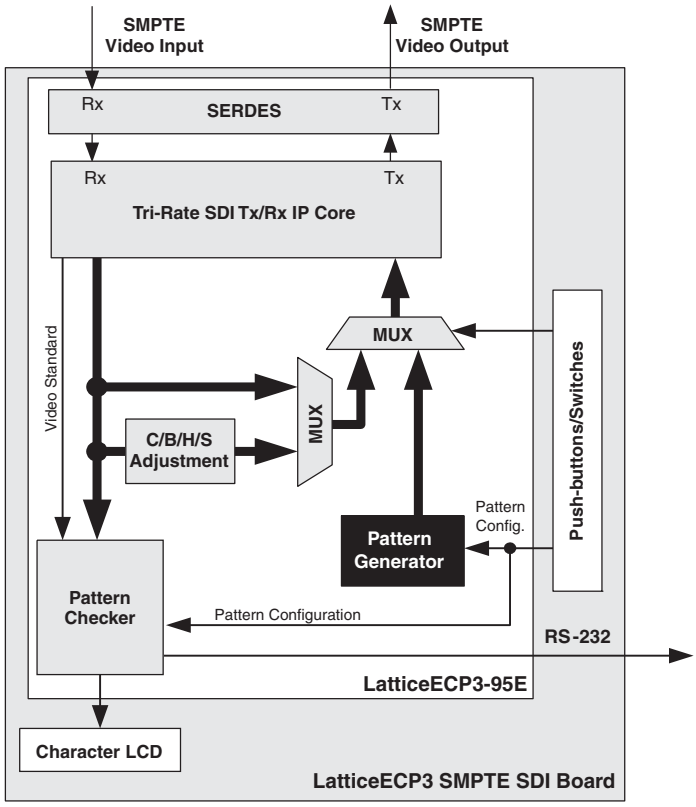
Table 3. Supported Video Formats and Corresponding Switch Settings (3G-SDI Part 2)

Standard	3G-SDI									
Bit Rate	2.97Gbps/M									
Serial SMPTE Standard	SMPTE 425M 3Gb/s Mapping, SMPTE 424M 3Gb/s serial interface									
Parallel SMPTE Standard	274M									
SW4[3]	1	1	1	1	1	1	1	1	1	1
SW3[2:4],SW4[1:2]	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101
Total words per line	2200	2640	2750	2200	2640	2200	2640	2750	2200	2640
Total lines per frame	1125	1125	1125	1125	1125	1125	1125	1125	1125	1125
Active words per active line	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920
Active lines per frame	1080p	1080p	1080p	1080i	1080i	1080p	1080p	1080p	1080i	1080i
Frame rate (Hz)	30/M	25	24/M	30/M	25	30/M	25	24/M	30/M	25
Fields per frame	1	1	1	2	2	1	1	1	2	2
Bits per word	20	20	20	20	20	20	20	20	20	20
Word rate (MHz)	148.5/M	148.5	148.5/M	148.5/M	148.5	148.5/M	148.5	148.5/M	148.5/M	148.5
Pixel sample rate (MHz)	148.5/M	148.5	148.5/M	148.5/M	148.5	148.5/M	148.5	148.5/M	148.5/M	148.5
Sampling structure	4:4:4	4:4:4	4:4:4	4:4:4	4:4:4	4:2:2	4:2:2	4:2:2	4:2:2	4:2:2
Pixel depth	12	12	12	12	12	12	12	12	12	12

Note: In Pattern-Gen mode, the factor M is 1 for video formats with integer frame rate formats and 1.001 for video formats with fractional frame rates. This factor is selected by SW1-2.

The functional block diagram of the demo is shown in Figure 1. The IP core does not include the SERDES, so the SERDES's PCS block is required to be generated from IPexpress™ and then connected to the IP core.

Figure 1. Functional Block Diagram of the Design



The pattern generator shown in Figure 1 can generate different test patterns for all the 32 video formats. As shown in Figure 2, there is another instance of this pattern generator in the pattern checker module. The pattern generator shown in Figure 1 is controlled by the on-board switches. However, depending on the operational mode, the pattern generator in the checker module may be controlled either by the on-board switches or the output signals of the IP core.

The block diagram of the pattern checker is shown in Figure 2. The Sync Control module monitors the parallel video data received by the IP core and releases the reset of the pattern generator at the exact right time so that the pattern generator can generate the data that is synchronized with the data received by the IP core. With that, the CMP comparator can compare the two data buses and registers the results in the Timer/FCNT module. The Timer/FCNT is a module that includes a 100-hour timer and a frame counter. The timer provides the timestamp for the tests. This timestamp can not be reset after power on. The frame counter counts the number of successfully passed frames before hitting a comparison error. When an error occurs, the time and the location of the mismatch in the video format will be reported. The LatticMico8™ microprocessor in this design is used for sending out the design status to the 20x2 character LCD module. It also sends the test results through the UART to an external terminal. A personal computer with serial RS-232 port can be used to run the HyperTerminal application. By using the HyperTerminal's text capturing feature, the overnight or over-the-weekend test results can be stored in a text file.

Figure 2. Functional Block Diagram of the Pattern Checker

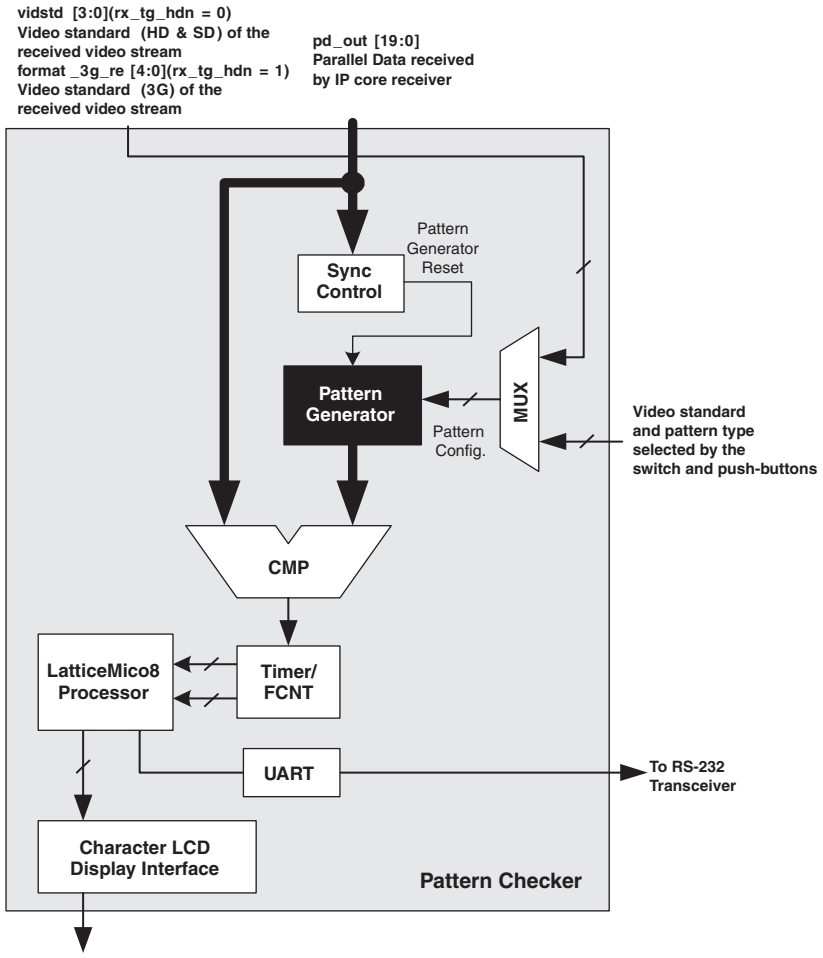
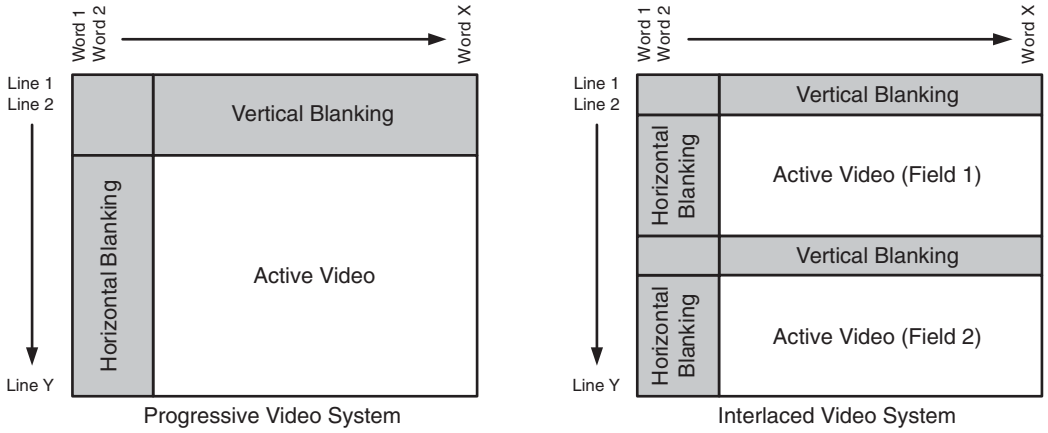


Figure 3 shows the basic data structure of a SDI video frame. It is similar to the timing format of the analog system. As seen in Figure 3, the progressive standard and the interlaced standard have different numbers of fields per frame. Other than that, the total lines per frame, the total words per line, and the sizes of the vertical/horizontal blanking periods are also different from one video format to another. Refer to Table 1 for the actual numbers.

Figure 3. Basic Data Structure of the SDI Systems



X: Total words per line
Y: Total lines per frame
Bit rate = X * Y * Frame rate * Bits per word

Figure 4 shows some examples of the words in a line of the SD-SDI, HD-SDI and 3G-SDI systems.

For the HD and 3G system, these data words are generated at the same clock frequency as the pixel clock. However, for the SD system, they are running at only half of the pixel clock frequency.

Figure 4. SDI System Data Stream Examples

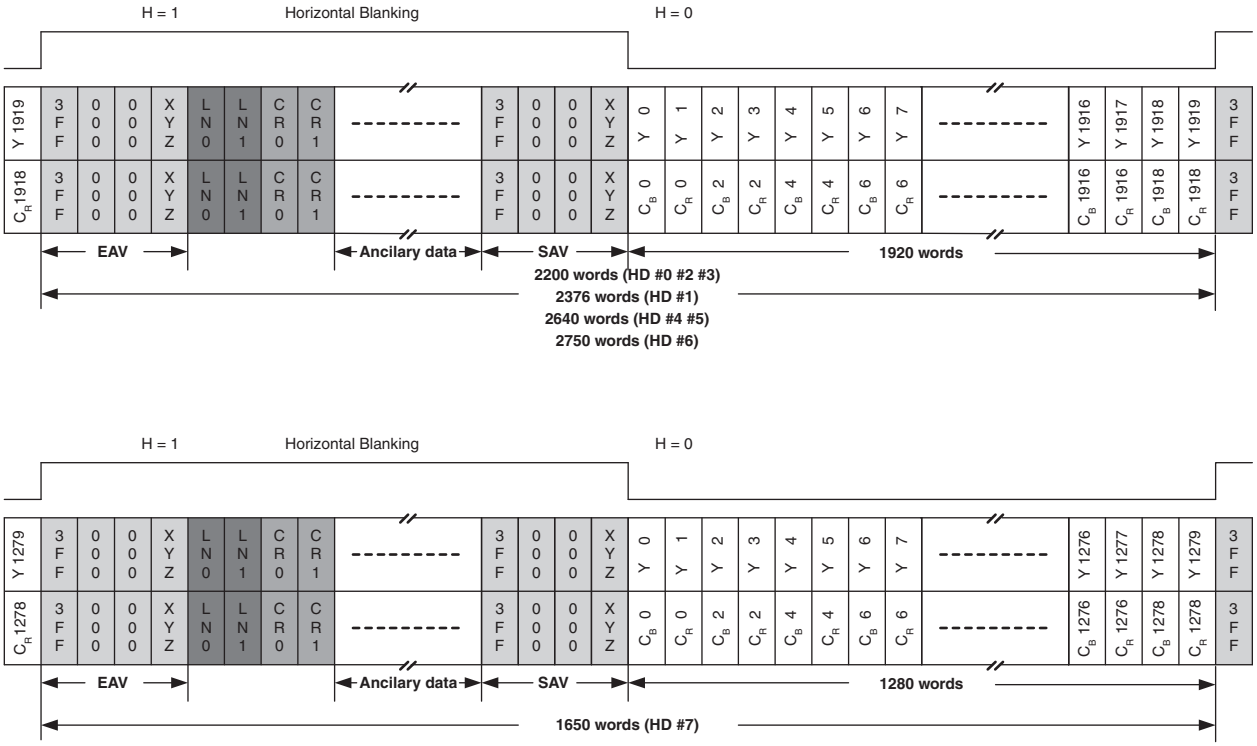
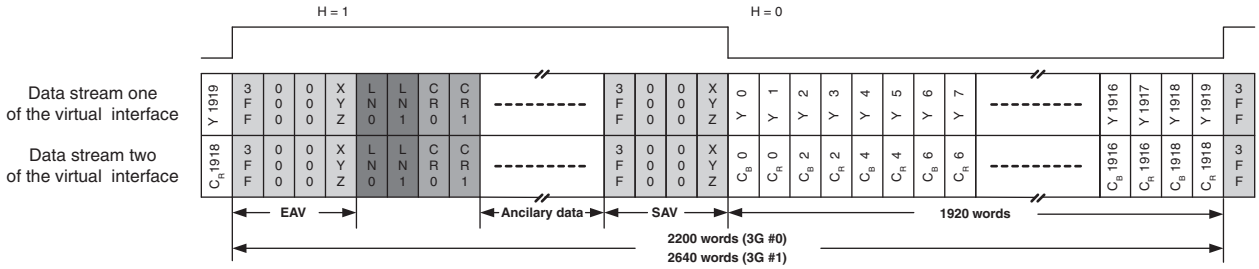
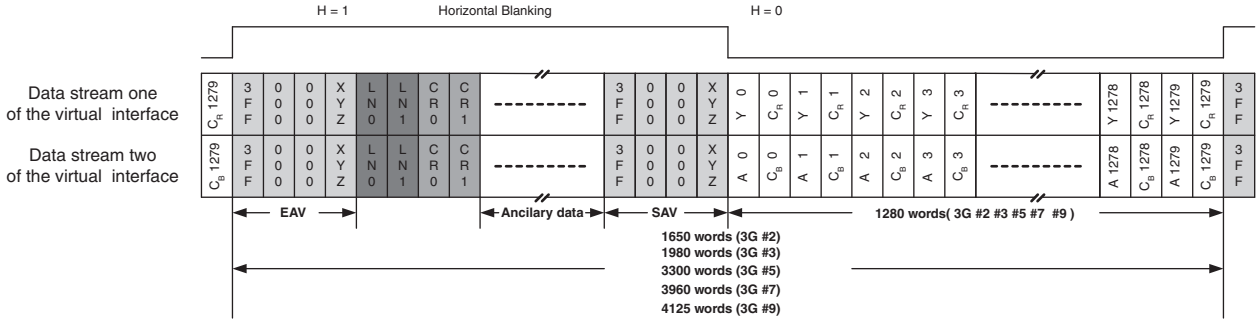


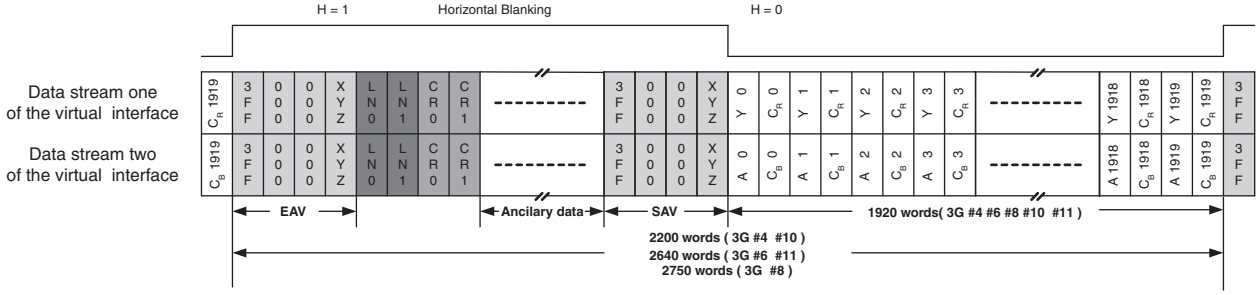
Figure 4. SDI System Data Stream Examples (Cont.)



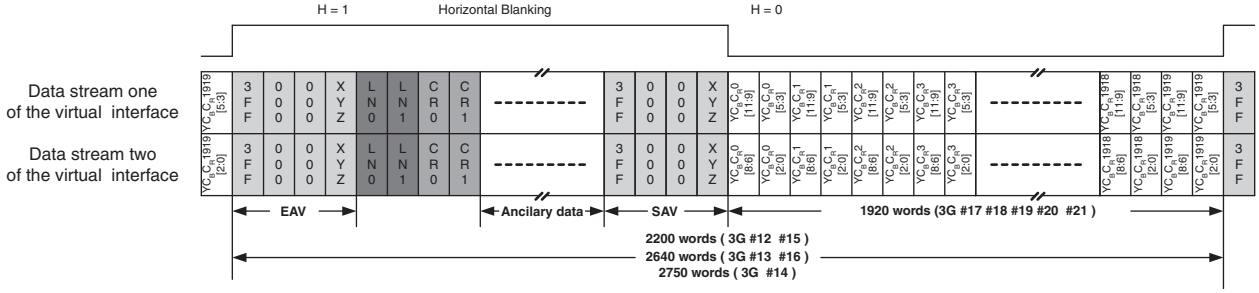
Mapping structure 1 (4 : 2 : 2 (YC_BC_R)/10bit)



Mapping structure 2 (4 : 4 : 4 : 4 (YC_BC_R + A)/10bit)



Mapping structure 2 (4 : 4 : 4 : 4 (YC_BC_R + A)/10bit)

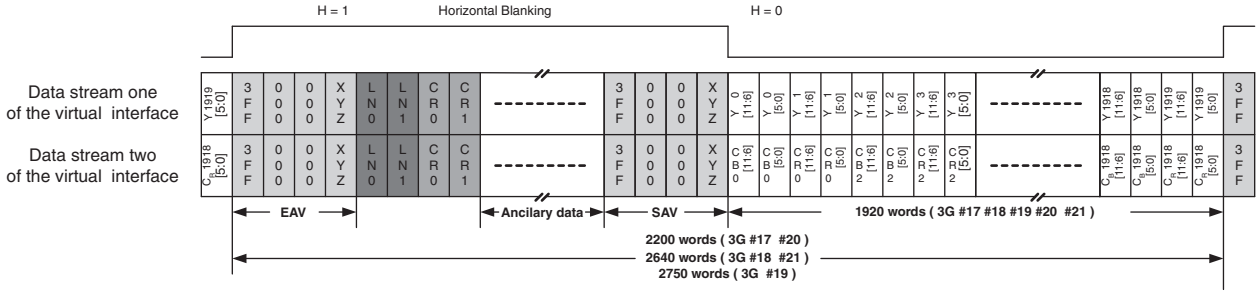


Mapping structure 3 (4 : 4 : 4 YC_BC_R / 12bit)

Figure 4. SDI System Data Stream Examples (Cont.)

	Bit number									
Data stream	9	8	7	6	5	4	3	2	1	0
Data stream one first word of sample	~B8	C_R[11:9]			Y[11:9]			C_B[11:9]		
Data stream one second word of sample	~B8	C_R[5:3]			Y[5:3]			C_B[5:3]		
Data stream two first word of sample	~B8	C_R[8:6]			Y[8:6]			C_B[8:6]		
Data stream two second word of sample	~B8	C_R[2:0]			Y[2:0]			C_B[2:0]		

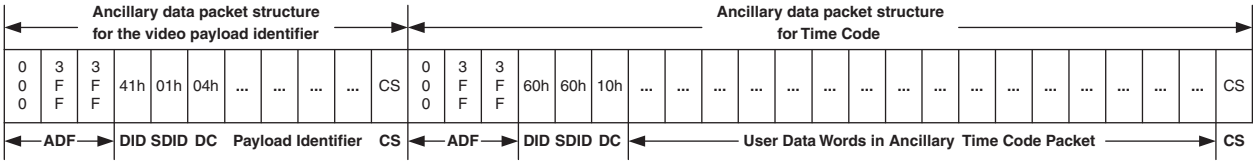
Bit structure for mapping structure 3



Mapping structure 4 (4 : 2 : 2 YC_BC_R / 12bit)

	Bit number									
Data stream	9	8	7	6	5	4	3	2	1	0
Data stream one first word of sample	1	Res			Y[11:6]					
Data stream one second word of sample	1	Res			Y[5:0]					
Data stream two first word of sample	1	Res			C_B[11:6]					
Data stream two second word of sample	1	Res			C_B[5:0]					
Data stream two third word of sample	1	Res			C_R[11:6]					
Data stream two fourth word of sample	1	Res			C_R[5:0]					
NOTE : Res = reserved, set to '0'										

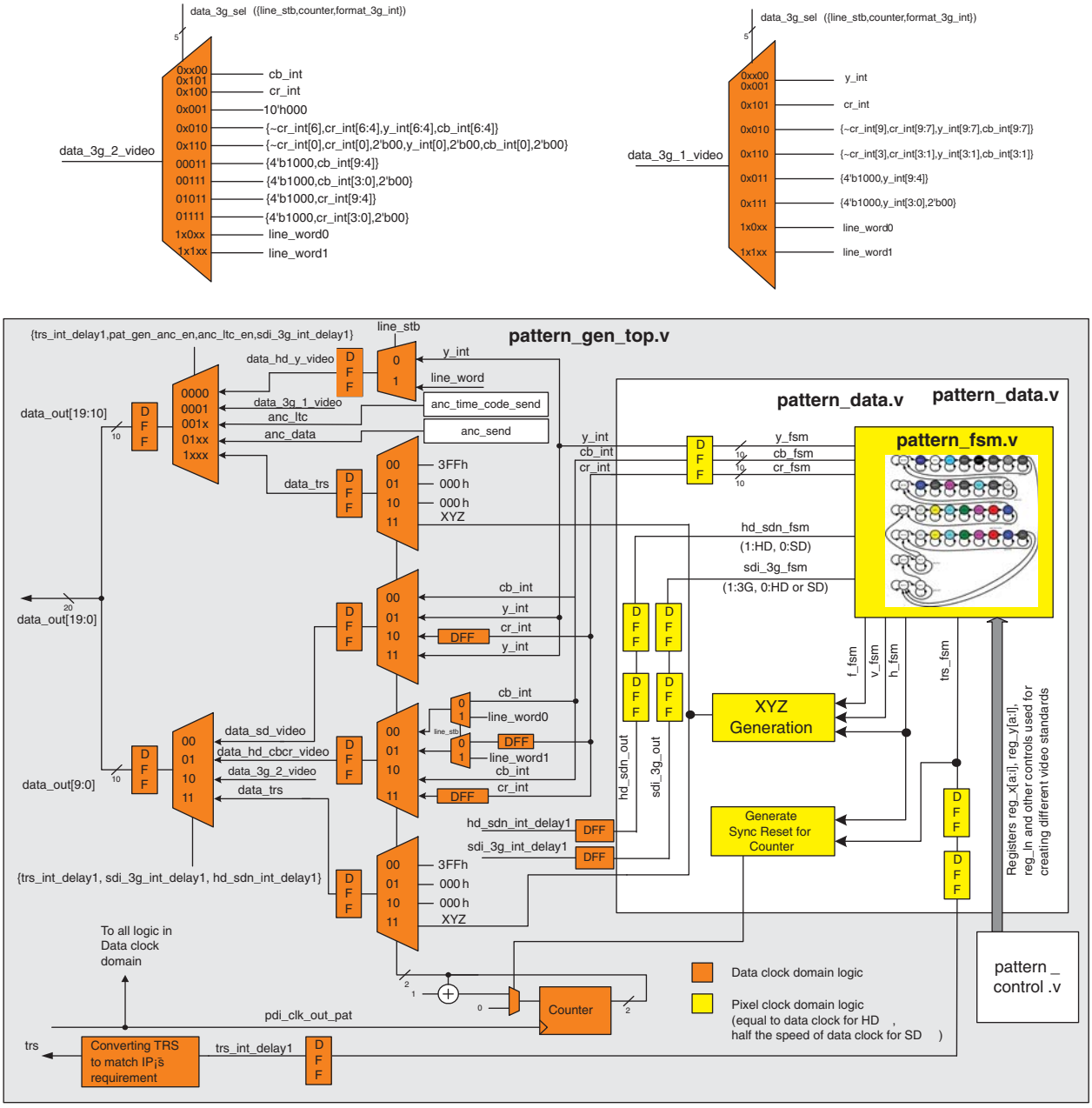
Bit structure for mapping structure 4



Instead of using lookup tables for supporting the 32 different video standards, the pattern generators employ a finite state machine so that they can be easily configured from one to another. Figure 5 shows the block diagram of the pattern generator. The finite state machine is controlled by parameters stored in configuration registers, which can be updated with different values based on the standards and patterns selected by the switches. This is completed by the Pattern_Control module shown in the block diagram. The outputs of the finite state machine are the Y, Cb, Cr video pixel data and the field, vertical blank and horizontal blank information. The field, vertical blank and horizontal blank are used for creating the XYZ word in the Pattern_Data module. The Y, Cb and Cr outputs of the

finite state machine are in YCbCr 4:2:2 format. There are another two modules, anc_send and anc_time_code_send, which are used to insert the ancillary data. The ancillary data packets are inserted between the CRC and the SAV, and the packets with payload identification and time code are inserted in this demo.

Figure 5. Block Diagram of the Pattern Generator



Video Clocking Scheme

This section describes the reference clocks used in the Rx side and Tx side SERDES. The SERDES reference clock can be sourced from either the external dedicated package pins or the internal FPGA fabric. The external dedicated refclk pins are shared for the SERDES within the same quadrant. Hence, if Rx and Tx need to use different reference clocks, they must come from different sources.

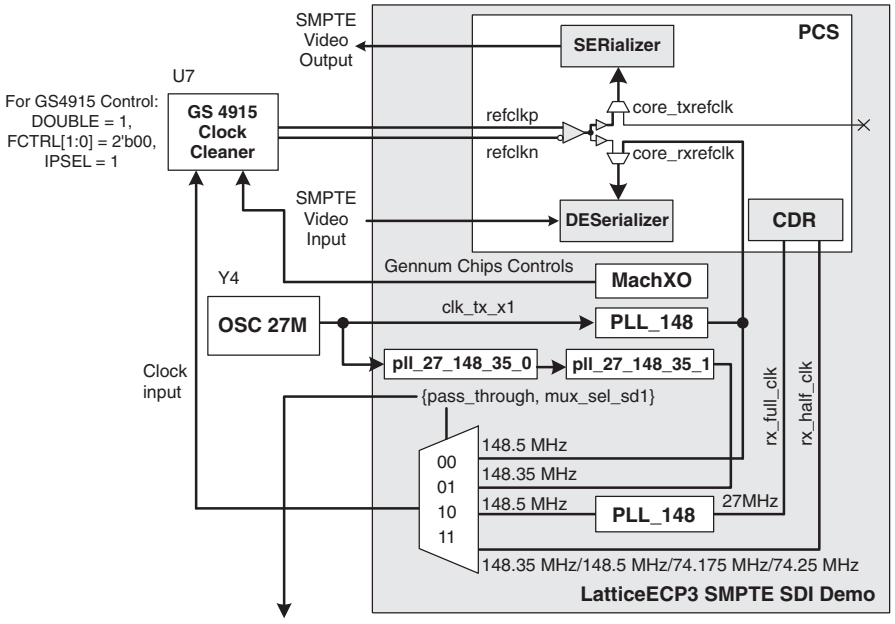
Each Tx Serializer and Rx Deserializer can be split into a full data rate and div2 rate or div11 rate depending on the rate configure pins of the PCS. This allows for different data rates in each direction and in each channel. The frequency division is done by the PLL inside the PCS. So, the Tx or Rx reference clock can be fixed at 148.5MHz.

For Pass-Through mode, the Rx reference clock is used by the DESerializer for reference only and its frequency is okay to be slightly different from the DESerializer's recovered clock by a few PPM. This is because the DESerializer's recovered clock is actually the clock used to recover the serial data. On the Tx side, however, the reference clock used by the SERializer must be able to create a transmit clock that is exactly (0 PPM difference) the same frequency as the DESerializer's recovered clock. Otherwise, a video frame buffer must be used for dropping or duplicating a frame when it is needed so that the Tx frame rate can still be slightly different from the Rx frame rate.

In order to provide a Tx reference clock that is GENLOCKed to the input video stream, the LatticeECP3 SMPTE SDI board uses GS4915 to clean the recovery clock. After the CDR is locked to the input video stream, the recovery clock rx_half_clk (HD or 3G mode) or the multiplier of the rx_full_clk (SD mode) will then be fed into Gennum's GS4915 clock cleaner to reduce the jitter. If not controlled, the jitter will migrate from the reference clock to the serial data output. A low jitter reference clock ensures the jitter on the SERializer output to be controlled within the SDI's specification.

Figure 6 shows a block diagram of the reference design clocking scheme. Only a 27 MHz oscillator and a Gennum GS4915 clock cleaner device are used for all the video formats supported in this demo. The 27 MHz oscillator is used to generate the Rx reference clock and the Pattern-Gen mode Tx reference clock. When in Pattern-Gen mode, if the video formats with fractional frame rates are selected by turning on SW1_2, a 148.35MHz clock will be generated by the 27MHz and two cascaded PLLs. The Pass-Through mode Tx reference clock is coming from the recovered clock of the SERDES. Using GS4915 ensures that a clean clock with very low jitter will be generated for the SERDES Tx reference clock and the SDI video output stream will have low timing jitter and alignment jitter. Depending on the demo mode and the video format being run, the reference clock may come from four different sources. There is a 4:1 MUX in the demo used for clock selection. The output of the MUX is sent to the GS4915 for jitter cleaning. The frequency of this MUX output may be either 148.35 MHz, 148.5 MHz, 74.175 MHz, or 74.25 MHz. The GS4915 is configured to run in Auto Frequency mode by setting its FCTRL[1:0] controls to low. The GS4915's DOUBLE control is set to high so that when the MUX output is either 74.175 MHz or 74.25 MHz, it will be doubled to 148.35 MHz or 148.5 MHz. Table 4 shows the MUX selection when the demo is running in different modes and video formats.

Figure 6. Reference Clock Connection



When pass_through is '1', rx_hd_sdn is used to select SD or HD/3G (mux_sel_sd1 = rx_hd_sdn).
When pass_through is '0', sw1_2 (M select switch) is used if fractional frame rate is defined (mux_sel_sd1 = sw1_2 and frac_valid).

Table 4. MUX Selection Control

Mode	MUX Select	Video Format	MUX Output	GS4915 Output	Units
Pattern-Gen	00	SD (525i and 625i) and HD/3G with integer frame rates	148.5	148.5	MHz
	01	HD/3G with fractional frame rates	148.35	148.35	MHz
Pass-Through	10	SD (525i and 625i)	148.5	148.5	MHz
	11	HD with integer frame rates	74.25	148.5	MHz
		HD with fractional frame rates	74.175	148.35	MHz
		3G with integer frame rates	148.5	148.5	MHz
		3G with fractional frame rates	148.35	148.35	MHz

Figure 8 shows how the Rx reference clock is generated by CORE_RXRFECLK (from FPGA fabric) and the Tx reference clock is generated by the REFCLK (from external pins).

Figure 7. Clocking Setup for PCS

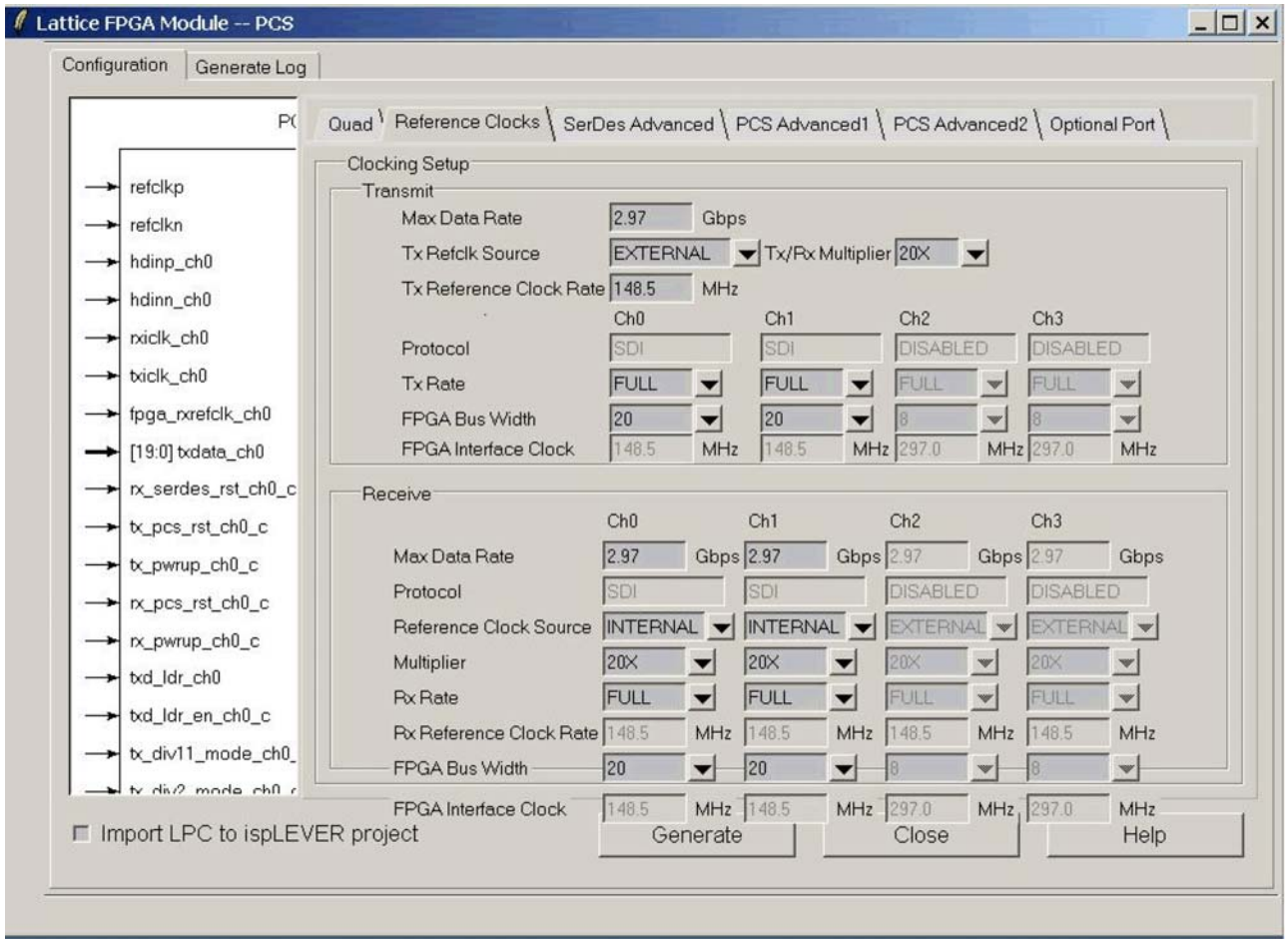
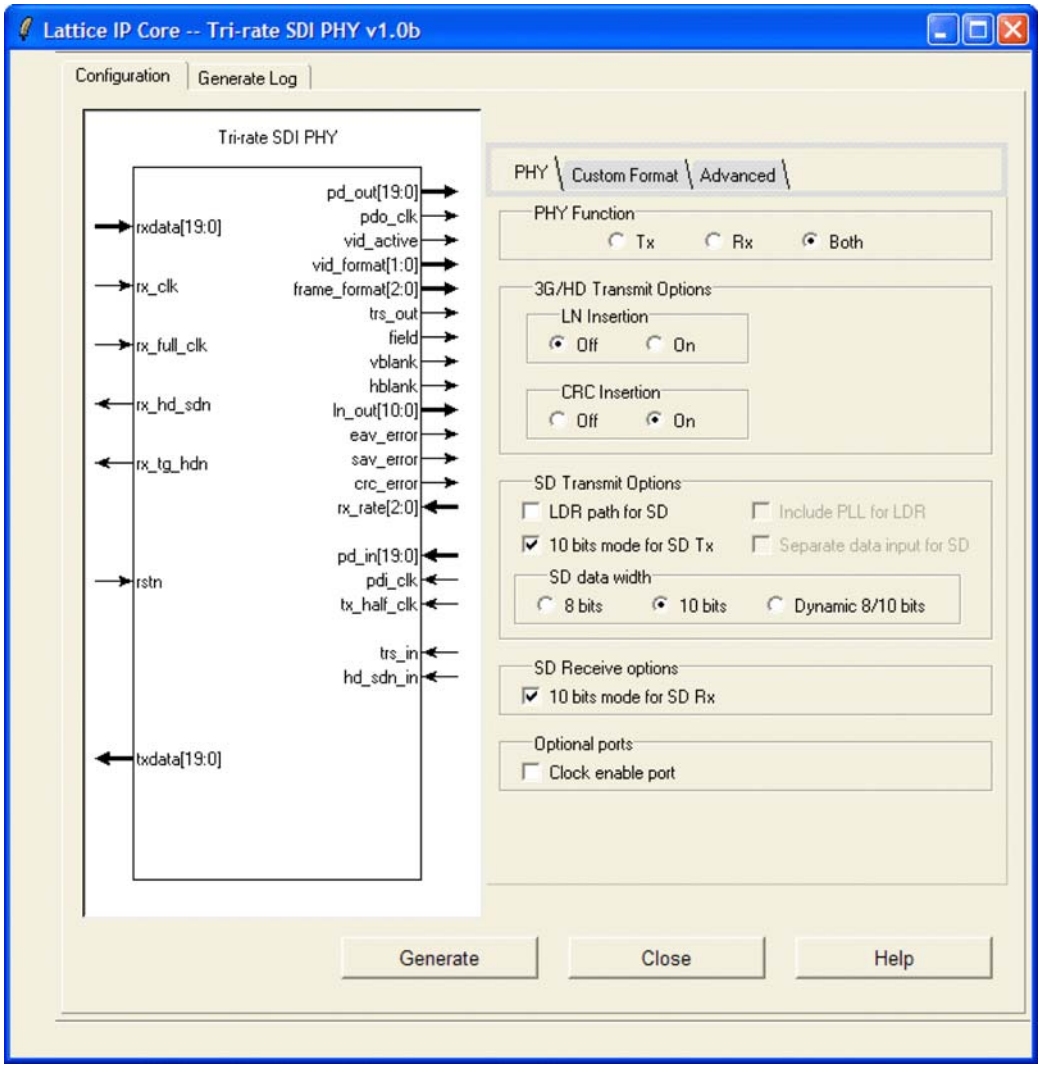


Figure 8. Tri-Rate SDI PHY IP Core Generation

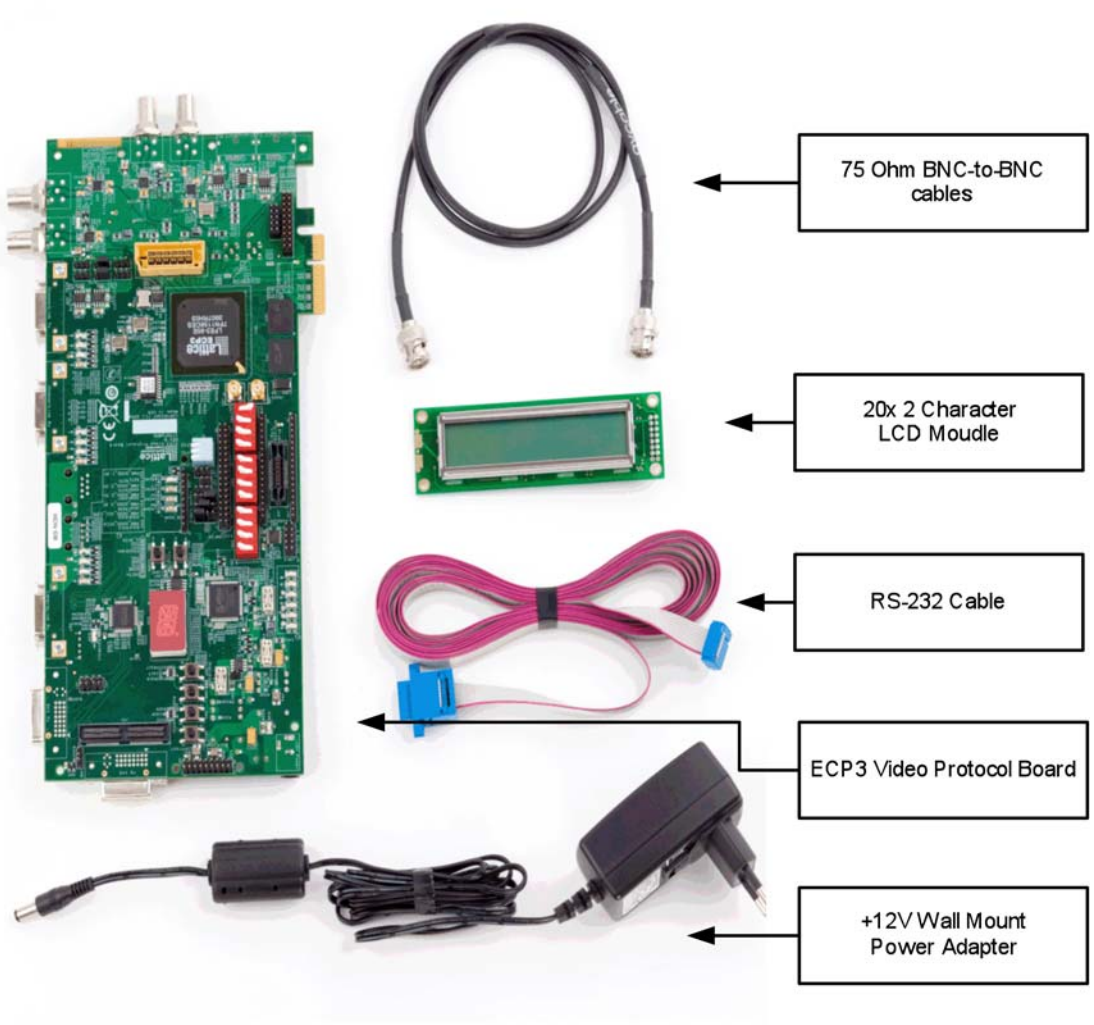


Demo Kit

This design uses LatticeECP3 Video Protocol Board, which includes the following items:

- LatticeECP3 Video Protocol Board
- RS-232 cable
- 75 Ohm BNC-to-BNC cables
- +12V wall mount power adapter
- 20x2 character LCD module

Figure 9. Items Included in the Demo Kit

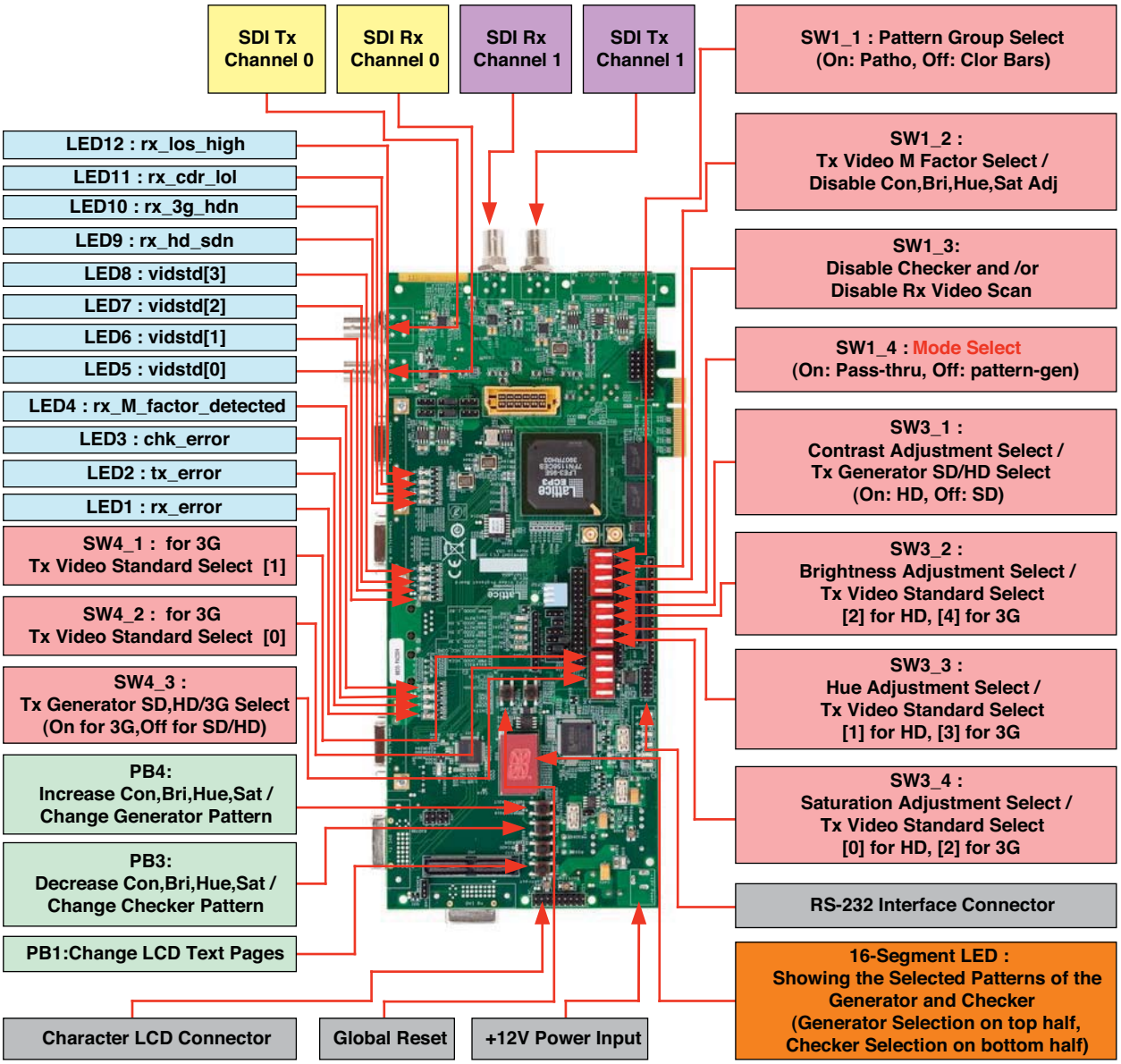


Demo Settings

To run this demo, you will need to connect cables, adjust switches, press push-buttons and monitor the LEDs. Figure 10 lists the functions of the connectors, switches, push-buttons and LEDs that are used in the demo. Since the demo design is controlled by the limited number of switches and push-buttons, many of these switches and push-buttons have dual functions depending on the mode of operation.

There are three 4-position SPST switches, SW1, SW3 and SW4, on this board that are used for the demo controls. The most important one is in position #4 of SW1, which is designed as SW1_4 in this document. SW1_4 is used to select the mode of operation of this demo. The setting of SW1_4 determines the functions of the other switch positions and the push-buttons. The demo settings are controlled by push-buttons PB1, PB2, PB3 and PB4 and switches SW1, SW3 and SW4. The following sections include detailed descriptions of these switches, push-buttons and LEDs in the two operational modes.

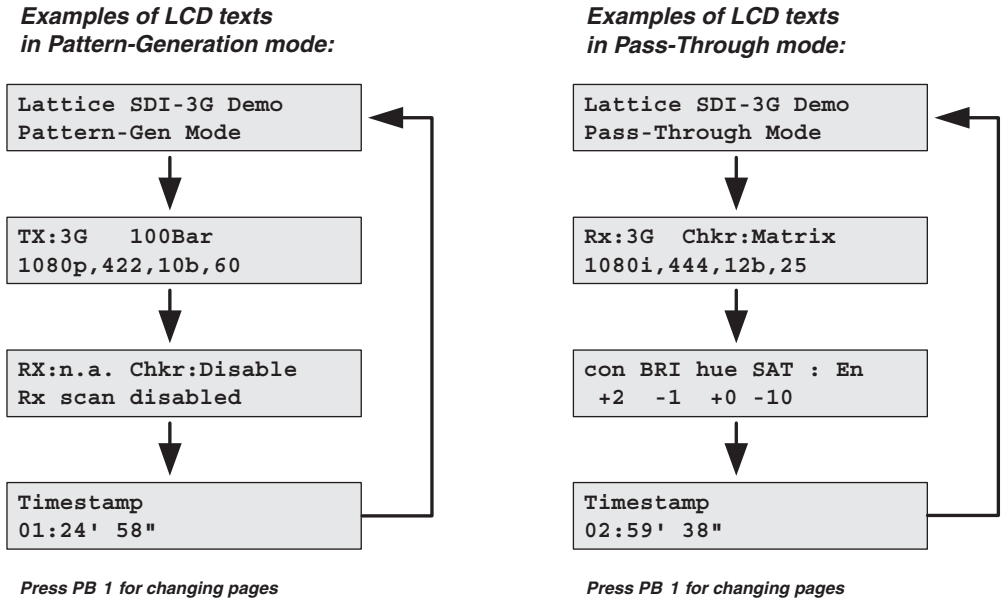
Figure 10. Functions of the Connectors, Push-buttons, Switches and LEDs



There is a 20x2 character LCD module provided with this demo kit. It needs to be installed on J43. If it is not installed, please refer to the photos in this document for the installation. The LCD can display four different pages of contents. The texts of these pages are different for Pass-Through Mode and Pattern-Generation Mode. Whenever the SW1, SW3 and SW4 switches or the push-buttons are adjusted, the LatticeMico8 processor will sense the adjustment and then turn the page to the related page.

When in Pattern-Generation Mode, these pages are (1) Current Mode, (2) Tx Status (3) Rx Status and (4) Time-stamp After Power On. When in Pass-Through Mode, these pages are (1) Current Mode, (2) Rx Status (3) Contrast/Brightness/Hue/Saturation Values and (4) Timestamp After Power On. Figure 11 shows the examples of these pages. You can also change the displayed pages by pressing the push-button PB1.

Figure 11. Examples of LCD Texts in Different Operational Mode



Running the Demo in Pattern-Generation Mode

When in Pattern-Generation mode, the design can create data patterns for color bars as well as the pathological signal tests. The generated video stream is out through SDI Tx Channel 0. It can be looped back through an SDI cable back to SDI Rx Channel 1 to the pattern checker. SDI Tx Channel 1 and SDI Rx Channel 0 are not used in this demo.

The patterns generated by the pattern generator are divided into two groups. The color bars group supports three different color bars types - SMPTE, 75% and 100% color bars. The pathological test group supports Matrix check-field, EQU check-field and the PLL check-field. As seen in Table 2, push-buttons PB3, PB4 and SW1_1 are used to select the color bars types or the pathological test patterns.

For video mode selection, SW3_1 and SW4_3 are used to select either SD, HD or 3G standards; SW3_2, SW3_3, SW3_4, SW4_1, SW4_2 are used to selected the specific format of the SD/HD/3G standard. The settings and the corresponding video formats are shown in Table 1 through Table 3.

The HD and 3G formats with 24 fps, 30 fps, and 60 fps frame rates can be adjusted to formats with fractional frame rates running at 23.98 fps, 29.97 fps, and 59.94 fps. These are the video formats for the US/Japan standards that have the 1.001 value of factor M shown in Table 1 through Table 3. The frame rates are actually 24/1.001, 30/1.001, and 60/1.001 frames per second. SW1_2 is used to select the value of factor M (either 1 or 1.001). When SW1_2 is turned ON, M is equal to 1.001 and the video patterns with fractional frame rates will be generated. This SW1_2 switch is used to select a fractional rate reference clock (148.35MHz as opposed to 148.5MHz). Note that the SD 525i video format has a fractional field rate of 59.94 (60/1.001) and a fractional frame rate of 29.97 (30/1.001). The SD 525i does not include a format with integer frame rate. However, the reference clock for this format is still 148.5MHz. The fractional frame rate of the SD 525i format is achieved by the frame structure, i.e. total words per line and total lines per frame, not by adjusting the pixel clock frequency.

When the video patterns with fractional frame rates are transmitted or received, "24/M", "30/M", or "60/M" will be displayed on the character LCD module.

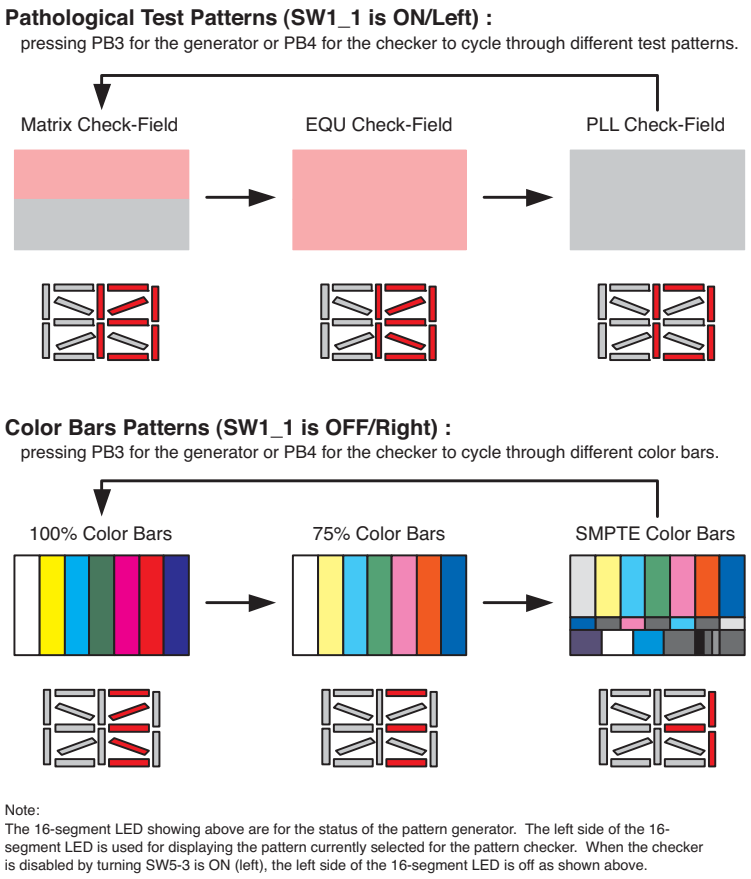
When in the Pattern-Generation Mode, both the pattern generator and the pattern checker are available. The pattern checker is used for checking the received video pattern in the loopback test. It can be disabled by SW1_3. When in Pattern-Generation mode, the checker pattern can be set to either color bars or the pathological test pat-

terns. Figure 12 shows the how the screen will look like when these patterns are selected. The 16-segment LED is used to display what pattern is currently selected. The corresponding 16-segment LED patterns are also shown in Figure 12. If the board is rotated to the orientation shown in this document, the bottom half of the 16-segment LED is used for displaying the pattern currently selected for the pattern checker, while the top half is for displaying the pattern currently selected for the pattern generator. If the checker is disabled by SW1_3, the left side of the 16-segment LED will be off.

Table 5. Switches for Color Bars Generation

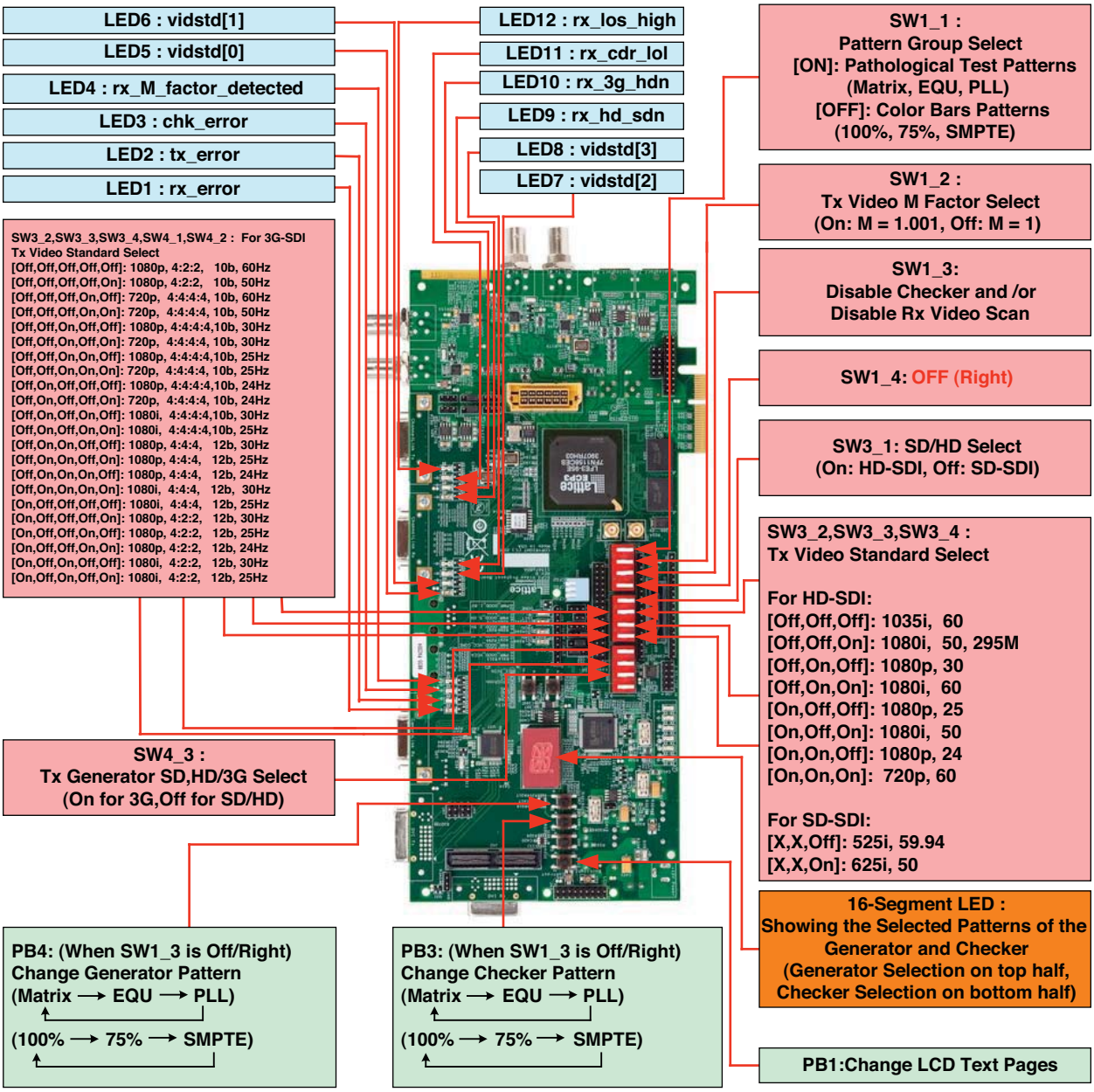
SW1_1	Selected Pattern Group	Changing Pattern by Pushing PB4 (for Generator) or PB3 (for Checker)
OFF (right)	Pathological Test	Matrix --> EQU --> PLL
ON (left)	Color Bars	100% --> 75% --> SMPTE

Figure 12. Pathological Signal Test Patterns on Screen



The push-button and switch controls as well as the LEDs function in Pattern-Generation Mode are shown in Figure 13. The pattern generator and the pattern checker can be enabled simultaneously in the Pattern-Generation mode. SW1_3 is used to turn the pattern checker off. When it is turned off, Rx scanning is also disabled. When Rx scanning is disabled, no video stream will be received by the receiver.

Figure 13. Pattern-Generation Mode Settings (SW1_4: OFF (Right))



Running the Demo in Pass-Through Mode

When in Pass-Through mode, the incoming video stream is received by SDI Rx Channel 1 and passed through SDI Tx Channel 0. SDI Tx Channel 1 and SDI Rx Channel 0 are not used in this demo.

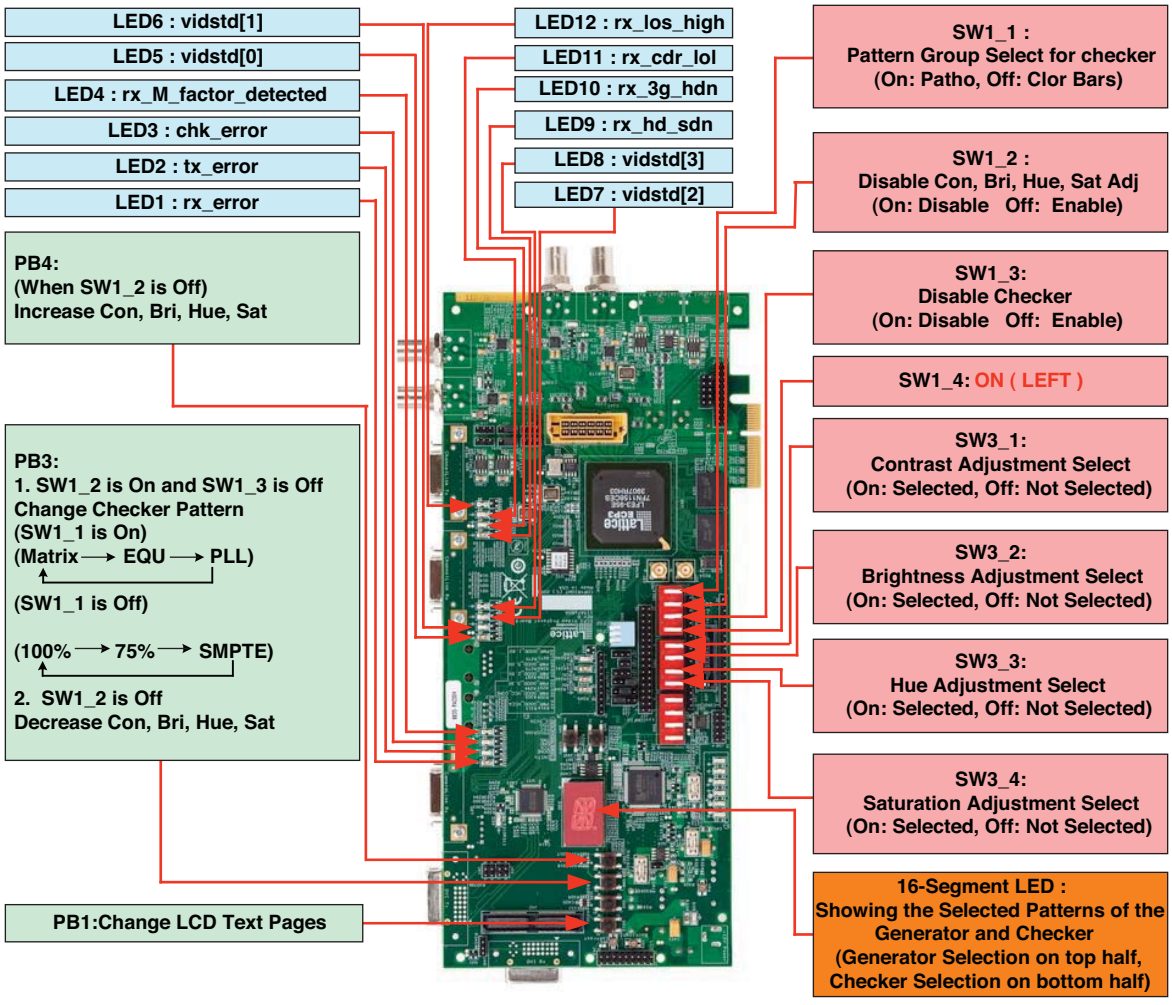
For running the demo in Pass-Through Mode, SW1_4 needs to be turn on (left). When in this mode, the Contrast/Brightness/Hue/Saturation adjustment video processing module can be used to adjust the received video before passing it through the Tx. The SW1_2 control the MUX that provides the parallel video data stream to the IP core transmitter. When SW1_2 is ON, the C/B/H/S adjustment module is bypassed and the original parallel video data stream received by the Rx is selected. When SW1_2 is OFF, the video data stream after the C/B/H/S adjustment is selected. The C/B/H/S adjustment is not supported for SD-SDI formats in this demo, so SW1_2 should be ON for SD-SDI formats in Pass-Through mode. This Contrast/Brightness/Hue/Saturation adjustment module, which includes 20 steps of adjustment from -10 to 0 to +10, is modified from the one used in RD1030, LatticeXP2

and LatticeECP2/M 7:1 LVDS Video Interface. The modification is required to address the sampling format difference between the SMPTE's YCbCr 4:2:2 and the YCbCr 4:4:4 in the 7:1 LVDS ChannelLink design. For more information about the design of this module, refer to the RD1030 document.

When running in Pass-Through Mode, the pattern generator will be forced to disable by the design. However, the pattern checker is still available for checking the incoming pattern and report errors if it finds any differences. The SW1_3 is used to disable the pattern checker if it is not required. In Pass-Through Mode, the pattern checker can check the incoming pattern with pathological test patterns only. They can only be either Matrix check-field, EQU check-field or PLL check-field, but cannot be the color bars as in Pattern-Generation mode. Push-button PB4 is used to select these test patterns. When using PB4 to select these test patterns, the SW1_2 must be turned ON to disable the C/B/H/S adjustment. Otherwise, pushing PB4 will increase the C/B/H/S selected by the SW3_1, SW3_2, SW3_3 and SW3_4 instead.

The push-button and switch controls as well as the LEDs in Pass-Through Mode are shown in Figure 14.

Figure 14. Pass-Through Mode Settings (SW1_4: ON (Left))

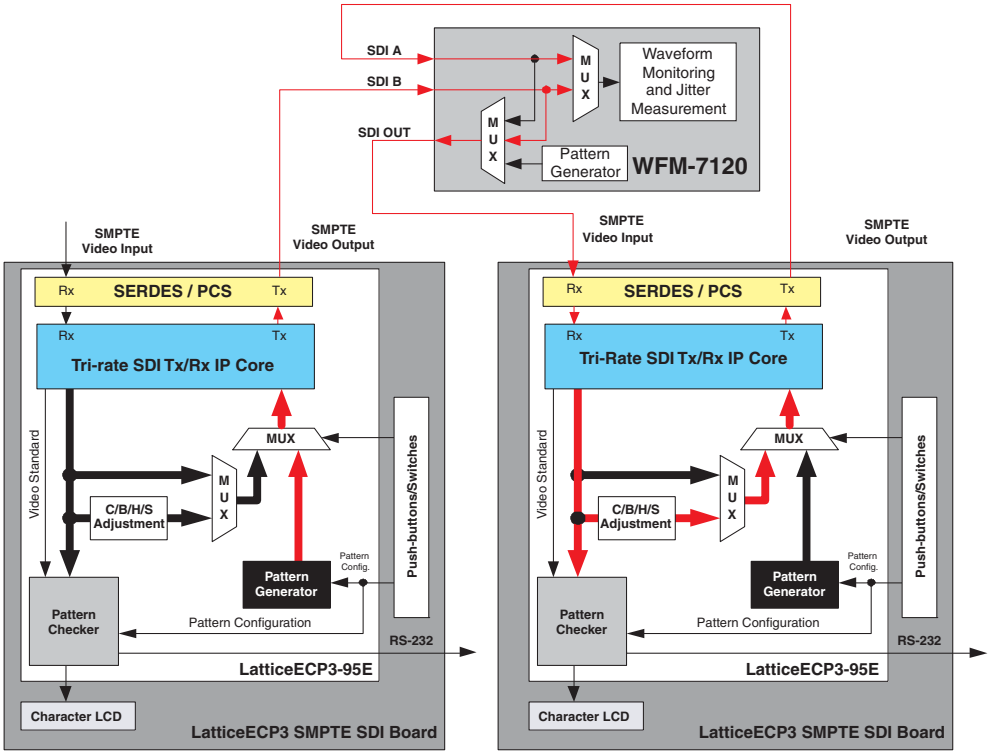


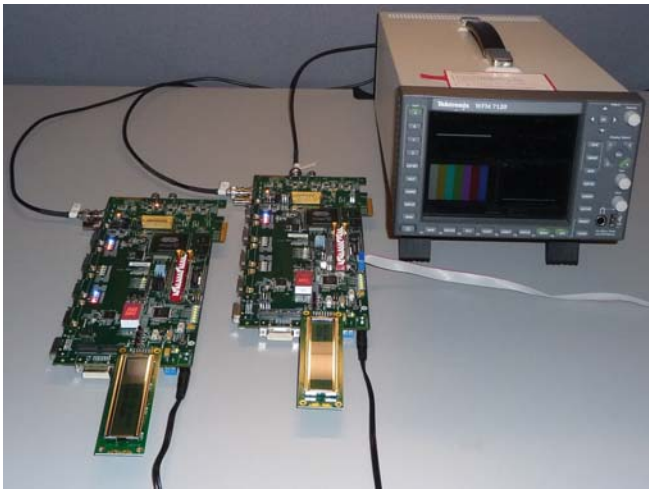
Cable Connections

The demo kit includes the 75 Ohm BNC-to-BNC cable.The SDI standard uses the 75 Ohm single-ended cable and you should use this cable for connecting to other SDI devices.

Figure 15 shows an example of using two SDI demo boards and a waveform monitor. The first board is set to Pattern-Generation mode and the second board is set to Pass-Through mode. The video output of the first board is connected to the SDI B input of the waveform monitor which can be displayed on the monitor. The waveform monitor is configured to loop the SDI B video input out of its SDI OUT port. The output of the second board is also connected to the waveform monitor through the SDI A input for monitoring and jitter measurement. The video process can be enabled, and the received video data can be adjusted with the Contrast, Brightness, Hue and Saturation.

Figure 15. Connecting Two Boards for pattern_gen and pass_through Mode Test





The pattern checker in the second board can be turned on. Since the Pattern Generator and the Pattern Checker can be set to different pathological check-field test patterns, please make sure they are set to the same test patterns, otherwise you will see the orange pattern-checking error LED flashing and the detailed error reported through the UART/RS-232 port. To monitor the detailed test results, set the RS-232 port to 115200 bps, 8 data bits, 1 stop bit, no parity bit and no flow control. Figure 16 shows an example of the test results captured by the HyperTerminal application. When the test is running without errors, the DP (Decimal Point) of the 16-segment LED will be flashing.This DP-segment is connected to one of the bit of the FCNT frame counter.The FCNT is used to count how many frames are compared without errors.The flashing of DP-segment indicates the testing is running good.In the Pattern-Generation Mode, the color bars patterns can also be used as test patterns.When the color bars patterns are selected for the loopback test, the 16 strip shape segments of the 16-segment LED will all be turned off.Since the YCbCr data of the color bars may be slightly different from test equipment to test equipment, you may see errors if you use an external waveform generator to generate the color bars and use the Pattern Checker to compare with whatever was received by the IP core receiver.

Figure 16. Example of the Test Results Captured by HyperTerminal

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Lattice SMPTE 3G-SDI Demo (V1.0) - designed by Joseph H. & Guolin W. 04/06/2009

Matrix   720p,60 00:00'01"03->08:07'19"29 Fram=01754242  ErrPLL Elaps =08:07'18"26
Matrix   720p,60 08:07'20"10->08:07'20"14 Fram=00000000  ErrTRS Elaps =00:00'00"00
Matrix   720p,60 08:07'20"94->15:10'09"94 Fram=01522092  Passed Elaps =07:02'49"00
Pattern Checker Disabled   !!!
Matrix   720p,60 15:10'13"61->
Received Video Format or Pattern Changed    !!!
Matrix  1080i,50 15:10'16"15->
Received Video Format or Pattern Changed    !!!
EQUtst  1080i,50 15:10'22"69->
```

Technical Support Assistance

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2009	01.0	Initial release.
April 2009	01.1	Added fractional frame rate support.
April 2009	01.2	Corrected minor errors in Video Clocking Scheme and Running the Demo in Pass-Through Mode text sections.
July 2009	01.3	Updated the following figures to include revision B of the evaluation board: - Items Included in the Demo Kit - Functions of the Connectors, Push-buttons, Switches and LEDs - Pattern-Generation Mode Settings (SW1_4: OFF (Right)) - Pass-Through Mode Settings (SW1_4: ON (Left))
October 2010	01.4	References to "LatticeECP3 SMPTE Video Evaluation Board" corrected to read as "LatticeECP3 Video Protocol Board".
December 2011	01.5	Updated the Running the Demo in Pass-Through Mode text section.