WISHBONE-Compatible LCD Controller

Reference Design

FPGA-RD-02102-1.3

December 2019

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1. Introduction

Liquid Crystal Display (LCD) is a flat display device used in many electronic products. These slim and thin packages, known for their low power characteristics, are an excellent choice for consumer applications. LCD devices are also found in demo boards and evaluation tools to provide debugging capabilities. Use of these devices has been simplified with on-board controllers, on-board drivers, and generic interfaces available on most LCD modules.

This reference design provides a processor interface to the common dot-matrix LCD module. The on-chip oscillator available on some Lattice CPLD or FPGA families can further simplify the implementation by eliminating the need for an external clock source. This design is also suitable for low-power applications together with Lattice zeropower CPLDs.

2. Features

- WISHBONE bus interface
- Read/write cycle access time optimized according to the LCD module

3. Functional Description

This design is used to control dot matrix LCD modules that have an on-board controller and driver. The controller and driver are able to display a wide variety of symbols through the interpretation of a simple 4-wire interface. The 4-wire interface includes the following signals:

- Read/write enable (E)
- Register select (RS)
- Read/write (R/W)
- Data bus (DB7-DB0)

This reference design sits between a dot-matrix LCD module and a WISHBONE bus compatible host. It translates the WISHBONE commands into the necessary timing signals for the LCD module. The timing relationship among the above signals is detailed in the LCD module data sheet. Figure 3.1. shows the system interface of this reference design.

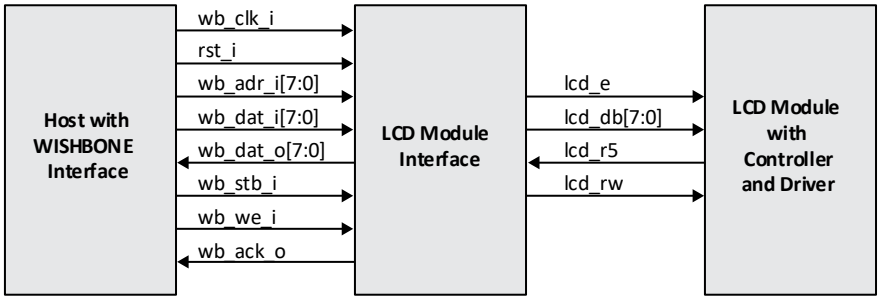

Figure 3.1. System Diagram

4. Signal Descriptions

Table 4.1. Signal Descriptions

Signal Name	Signal Direction	Signal Type	Active State	Definition
wb_clk_i	Input	WISHBONE Interface	N/A	Clock input.
rst_i	Input	WISHBONE Interface	High	Active high reset signal.
wb_adr_i[7:0]	Input	WISHBONE Interface	N/A	Address input.
wb_dat_i[7:0]	Input	WISHBONE Interface	N/A	Data input during read cycles.
wb_dat_o[7:0]	Output	WISHBONE Interface	N/A	Data output during write cycles.
wb_stb_i	Input	WISHBONE Interface	High	Strobe input signal indicates a valid data transfer cycle.
wb_we_i	Input	WISHBONE Interface	1 = Write 0 = Read	This signal is negated during read cycles and is asserted during write cycles.
wb_ack_o	Output	WISHBONE Interface	High	When asserted, indicates the normal termination of a bus cycle.
lcd_e	Input	LCD Interface	High	Read/write enable signal.
lcd_rs	Input	LCD Interface	0 = IR 1 = DR	Register select signal.
lcd_rw	Input	LCD Interface	0 = Write 1 = Read	Used as a read/write selection input. When high, read operation; when low, write operation.
lcd_db[7:0]	Input/Output	LCD Interface	N/A	

5. Register Transfer Level (RTL) Implementation

The RTL block diagram of the LCD module interface is shown in Figure 5.1. It consists of three modules, the top-level module, the WISHBONE slave module and the LCD interface module.

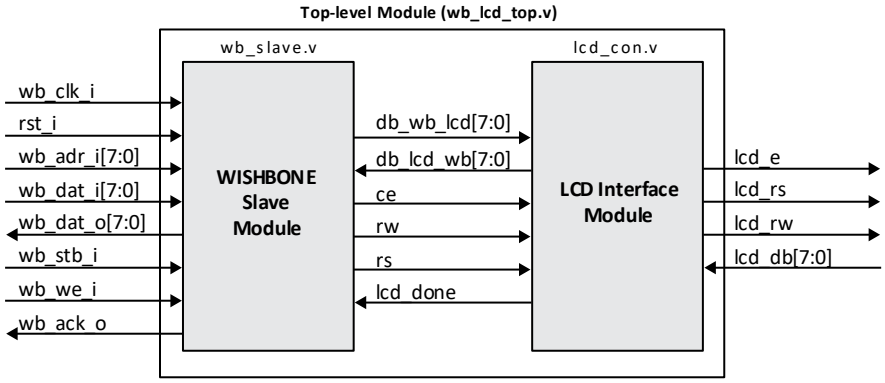

Figure 5.1. Block Diagram

5.1. Top-Level Module

This module is created to instantiate the other lower-level modules of the design.

5.2. WISHBONE Slave Module

The WISHBONE slave module interprets write/read commands from the WISHBONE master, passing relevant control to the LCD interface module. The active input signal wb_stb_i indicates a master-initiated bus transfer. The module then sends the signal ce to the LCD interface module to enable the LCD state machine. Meanwhile, the module generates the signal rw depending on the input signal wb_we_i, and the signal rs depending on the input signal wb_adr_i[0]. If the master initiates a read transfer, the module receives data from the LCD interface module. Otherwise, the module sends data to the LCD interface module. The module generates the signal wb_ack_o when the input signal lcd_done is active, indicating that the LCD interface module has finished the write or read command.

5.3. LCD Interface Module

This module generates the appropriate control signals together with data signals to access the dot-matrix LCD module. The timing of the signals meets the access time requirements for read and write of the LCD. It responds to the WISHBONE slave module by generating the signal lcd_done. This reference design is targeted at a dot-matrix LCD controller and driver S6A0069. The timing requirements are based on the S6A0069 data sheet. Figure 5.2. shows the write mode timing diagram and Figure 5.3. shows the read mode timing diagram.

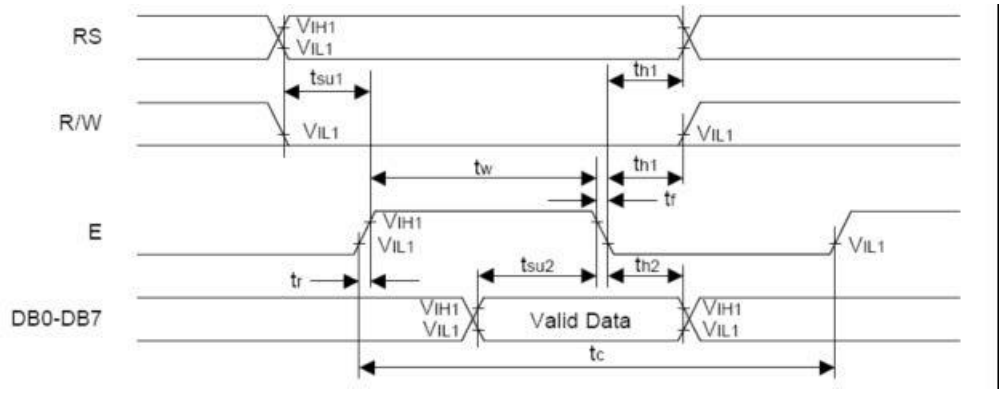

Figure 5.2. Write Mode Timing Diagram

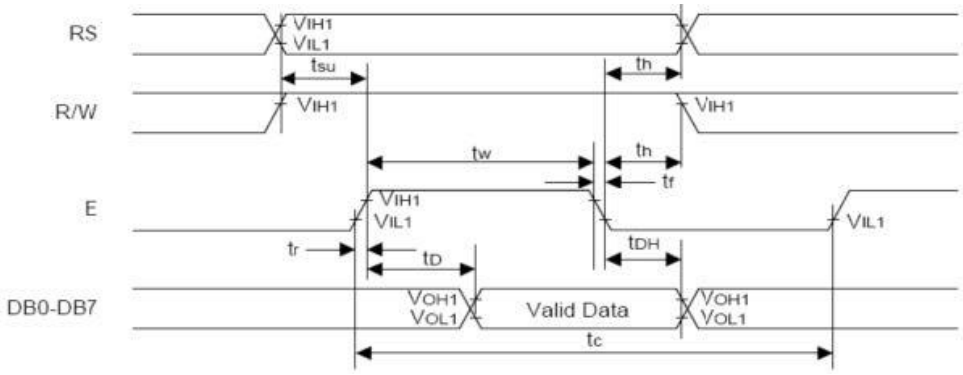

Figure 5.3. Read Mode Timing Diagram

When the WISHBONE slave module sends the signal ce to the LCD interface module, the LCD state machine in this module begins to work. Figure 5.4. shows the state diagram of the state machine in this module.

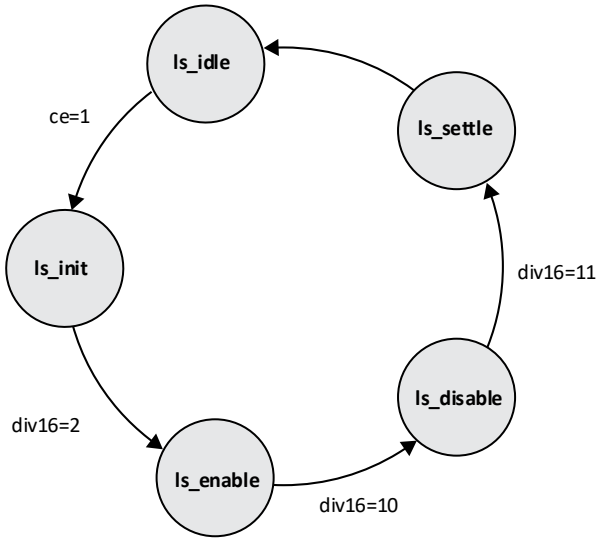

Figure 5.4. LCD State Machine

During reset, the state machine is forced to the ls_idle state. When reset is inactivated, the state moves from ls_idle to ls_init if the input signal ce is activated. In this state, the module enables the signal lcd_rw and lcd_rs. After 16 clock periods, the state moves from ls_init to ls_enable. In this state, the module enables the signal lcd_e. After 64 clock periods, the state moves from ls_enable to ls_disable. In this state, the module disables the signal lcd_e. After eight clock periods, the state moves from ls_disable to ls_settle. In this state, the module generates the signal lcd_done which is used in the WISHBONE slave module and then switches to the ls_idle state.

6. Clock Frequency Considerations

Two counters in the LCD interface module calculate the timing parameters required by the data transfer. When the state machine in the LCD interface module is enabled, the counters begin to work. 16 clock periods are used to generate the timing parameter tsu, 64 clock periods are used to generate the timing parameter tw and 8 clock periods are used to generate the timing parameter th. Faster clock frequencies need more clock cycles between the states because more clock periods are needed to achieve the required Tsu, Tw and Th timing of the LCD devices. Designers can modify the value of the counters if the high clock frequency (>200 MHz) is used.

7. Test Bench Description

The test bench for this design includes read and write tasks to and from the LCD module. These two tasks create the read or write cycles as a WISHBONE master and check the data from the LCD module.

8. Timing Specifications

The following timing diagrams show the major timing milestones in the simulation. The Tsu, Th, and Tw for read/write operations meet or exceed the LCD module data sheet requirements.

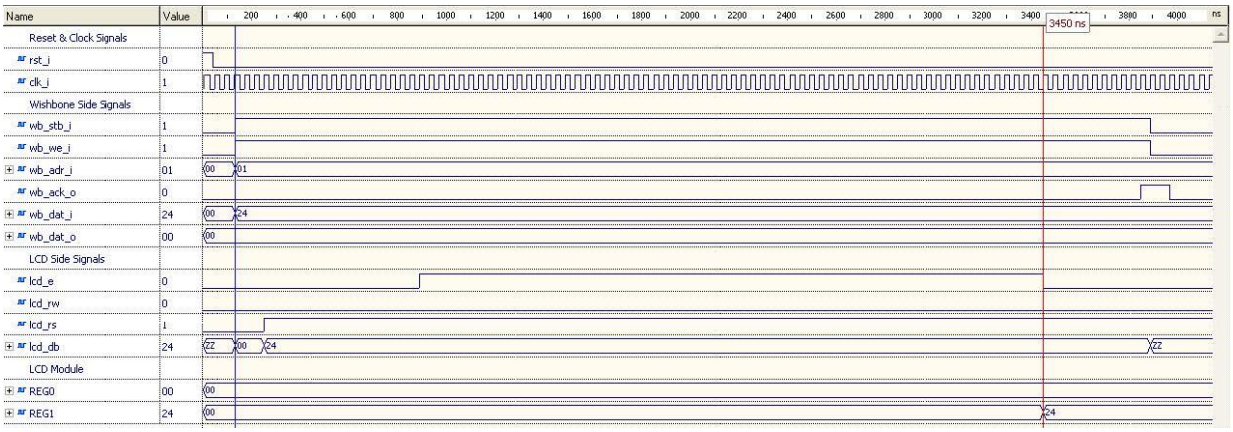

Figure 8.1. Write Operation Cycle

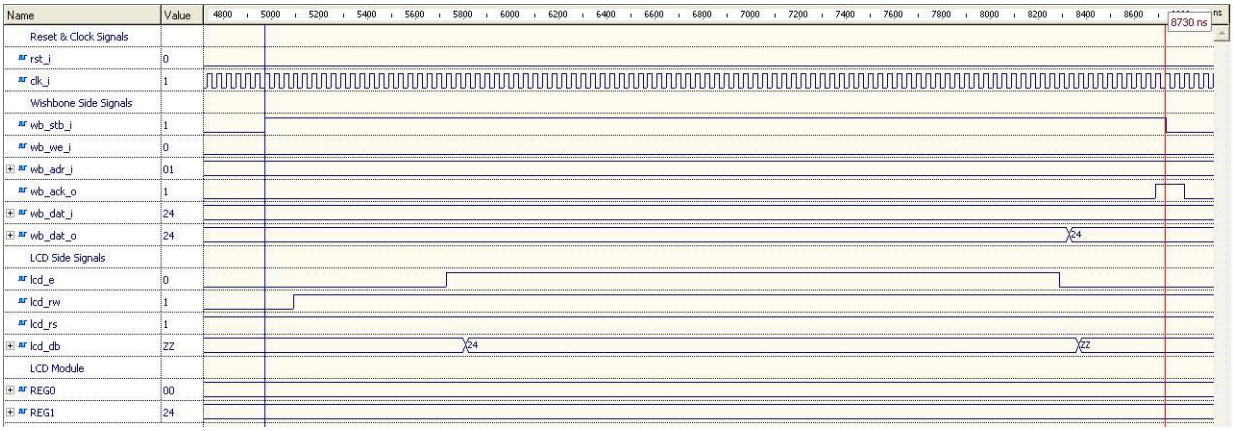

Figure 8.2. Read Operation Cycle

9. Implementation

Table 9.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
MachXO2™ [1]	Verilog	-4	25	> 50	33	NA
	VHDL	-4	25	> 50	33	NA
MachXO™ [2]	Verilog	-3	23	> 50	33	NA
	VHDL	-3	23	> 50	33	NA
LatticeXP2™ [3]	Verilog	-5	25	> 50	33	NA
	VHDL	-5	25	> 50	33	NA

Notes:

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-4TG100C, with Lattice Diamond™ 1.1 and ispLEVER® 8.1 SP1 software. When using this design in a different device, density, speed or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LCMXO2280C-3T100C, with Lattice Diamond 1.1 and ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LFXP2-5E-5TN144C, with Lattice Diamond 1.1 and ispLEVER 8.1 SP1 software. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Technical Support Assistance

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Revision History

Revision 1.3, December 2019

Section	Change Summary
All	• Changed document number from RD1053 to FPGA-RD-02102. • Updated document template.
Disclaimers	Added this section.

Revision 1.2, November 2010

Section	Change Summary
Implementation	Added support for MachXO2 device family.

Revision 1.1, April 2010

Section	Change Summary
Implementation	• Added support for LatticeXP2 device family. • Added VHDL support.

Revision 1.0, May 2009

Section	Change Summary
All	Initial release.

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