Platform Management Using Low-Cost Non-Volatile PLDs

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Introduction

Power-up control, general purpose I/O expansion, voltage level translation and interface bridging are common functions in telecom infrastructure, server and industrial applications. System designers are turning to the use of programmable logic devices (PLDs) to implement these functions in their designs due to the inherent time-to-market and design flexibility advantages they offer over ASICs and ASSPs. By using PLDs in their designs, designers can respond to changing market standards and requirements within a compressed window of opportunity. In addition, PLDs enable designers to reduce the total system cost by integrating discrete logic components combined with a small footprint, minimizing PCB space.

Figure 1 shows a typical platform management application in a server.

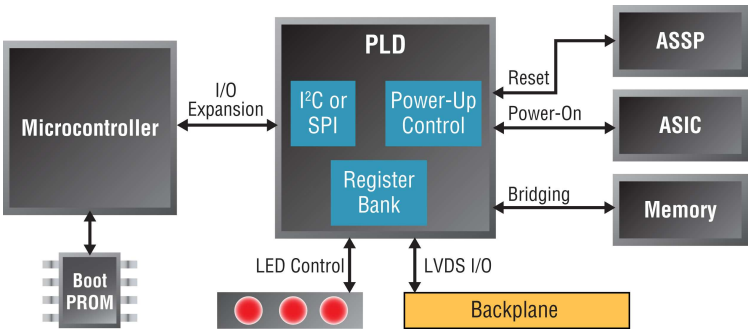

Figure 1 - Typical PLD usage in a server application

The platform manager device, in this case a PLD, communicates with a microcontroller, ASSPs, ASICs, LEDs and the backplane. The microcontroller monitors the status of the system through the register bank of the PLD via I2C or SPI interface. The PLD provides status indication via the LEDs and interfaces or bridges to the memory for logging in data or storing the configuration data. The PLD also communicates to the control path signals in the backplane via LVDS I/O and also provides a number of system reset and power-on signals to the ASSP and ASIC devices.

The following are the general requirements for this application and show how PLDs are able to meet these requirements.

Instant-on

Bus bridging and control logic functions have to operate before other devices power-up within a system. This includes the ability to control the power sequencing of other devices in a particular sequence to ensure that they operate correctly. Embedded non-volatile Flash memory enables a PLD to power up in less than 1ms and to implement these types of 'instant-on' functions.

3.3V Power Supply

Typically the platform management PLD operates from the auxiliary power supply as this is the first to be powered-on and the last to be powered off. For many systems the auxiliary rail is 3.3-volts. The ability to operate directly from this rail avoids the expense and increased component count of an additional regulator.

High I/O Count

As the number of devices increase on a board to provide different levels of system functionality, the number of I/Os needed to interface between these devices also increases. PLDs can be used to monitor and control many signals to multiple devices. In addition, they can be used in conjunction with a microcontroller or ASSP to increase the number of available user I/O.

Robust 3.3V I/O and Voltage Level Translation

Designers need to connect to multiple devices that operate at different voltages within a system. For example, the microcontroller needs to interface with peripheral devices such as ASSP, ASIC, memory and LEDs that operate at

different voltage levels. Voltage level translators can be used to implement this function. However, a PLD, which is less expensive than discrete voltage level translators, can be used to interface with different voltage levels ranging from 3.3-V to 1.2-V. Given that 3.3V interfaces still continue to be popular in platform management functions, a PLD must not only be able to drive and receive 3.3V signals, it must also be robust enough to operate in a noisy system environment.

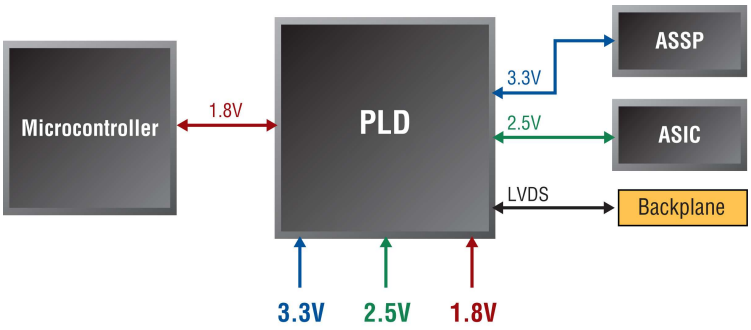

Figure 2 - Voltage level translation using a PLD

Interface Bridging and I/O Versatility

Within a system, devices with different I/O interfaces need to be connected. For example, interfacing between two different bus interfaces such as I2C and SPI requires a PLD to act a bridging interface. PLDs can be used to implement popular interfaces such as I2C-bus controller, I2C-bus master controller, SPI-bus controller, UART, SRAM controller and compact Flash controller for communication between a host processor and peripheral devices, including serial EEPROMS and compact Flash cards. PLDs have single ended I/O standards such as LVTTL, LVCMOS and PCI that operate at 3.3/2.5/1.8/1.2V and differential I/O standards such as LVDS that are required to interface with high speed interfaces such as a backplane. Additional emulated differential I/O standards, such as LVPECL, RSDS and BLVDS are also supported in some PLDs.

System Integration

In order to satisfy customer demand for changing features and standards, designers are often faced with the challenge of supporting a high level of functionality while trying to reduce the total system cost. Discrete devices can increase the bill of materials (BOM), lower board reliability and increase the total power budget of a system. PLDs offer the benefit of system integration by providing the ability to integrate discrete logic such as I/O expanders, voltage level and bus bridging translators, voltage regulator, clock sources and configuration devices, all in a single device. The availability of PLDs in space saving packages such as TQFP and csBGA reduces total PCB space and total system cost.

Remote Field Upgrade

Updating logic while devices are deployed in the field continues to increase in importance as it provides designers the flexibility to respond to changing standards, fix bugs, upgrade existing equipment and minimize system downtime. Some PLDs support this capability through the use of Flash and SRAM technologies on a single chip. The device's SRAM controls device configuration while the Flash is updated in the background mode. The I/O states are usually maintained during device programming to allow seamless transitions while updating the logic from SRAM to Flash.

Figure 3 - Remote field upgrade using PLDs

PLDs are an Ideal Fit For Platform Management

Compared to ASICs and ASSPS, PLDs offer significant time-to-market and design flexibility advantages that make them a compelling fit in platform management applications. ASICs have high non-recurring engineering (NRE) costs and long development times and, if they do not function correctly, or if the product requirements change due to changes in industry standards or market demand, a new design must be developed. This redesign results in significant NRE costs, which include engineering resources, new mask sets and software. ASSPs have lower NRE costs because they are used by multiple customers; however, they restrict the designers' capability to differentiate their products in the market.

PLDs enable designers to develop, test and make design changes without incurring any mask costs or design penalty. Because PLDs are reprogrammable, designers can make last minute changes and product upgrades using software design tools, even when the devices have already been deployed in the field.

Accelerating Time Between Design Development and Prototype Phases

In order to accelerate the development time required to implement control and interface bridging functions in a design, development kits and reference designs provide designers a path to prototype and to implement their designs in hardware. Development kits typically include an evaluation board populated with a PLD and peripheral devices such as memory, clock source, programming cables and a demo designs. Reference designs provide a good starting point for a design. Most reference designs are coded in HDL and include downloadable information such as documentation, project files and source code. Reference designs can typically be downloaded for free from the PLD vendor's website.

Example of an Instant-on Non-Volatile PLD – the MachXO PLD Family

Lattice's MachXO PLD family is an ideal fit for the platform management functions described above. Combining an optimized look-up table (LUT) architecture with low-cost embedded Flash process technology, the instant-on, easy-to-use MachXO devices are the most versatile, non-volatile PLDs for low-density applications. The combination of Flash and SRAM within the same device provides significant advantages for remote field upgrades as well as instant-on non-volatile operation. Upon power-up the SRAM configuration bits are loaded into the non-volatile memory of the device, enabling instant-on operation in less than 1ms after power-up.

Table 1 shows the key features and benefits of the MachXO PLD family.

Key Feature	Benefit
Instant-on, non-volatile	Powers up in less than 1ms enabling precise control during system boot-up
Single 3.3V core supply	Can be run off typical 3.3V auxiliary power rail without the need for a voltage regulator
Single chip	No external configuration memory required reducing total system cost
Small footprint	Space saving csBGA packaging
Embedded & distributed memory	Efficient cost effective data buffering
Built-in PLLs and oscillator	Integrated clock management reducing total system cost
Flexible high performance I/Os	Interface with multiple voltages and speed critical functions
Sleep mode	Reduces standby power to <100uA
TransFR technology	Allows remote field upgrades while the equipment operates

Table 1- MachXO PLD key features and benefits

MachXO PLDs have two power supply options. The upper voltage or "C" version supports 1.8, 2.5 and 3.3-V V_{cc}. A lower voltage or "E" version supports a 1.2V V_{cc}. For both versions of the device, Vcc_{aux} is a 3.3V auxiliary power supply that provides a higher internal reference voltage to optimize device performance.

Vcc_{io}, used for the general-purpose I/O banks, is a user-selectable voltage that corresponds to different I/O standards.

The MachXO "C" PLD can run off a single 3.3V power supply. MachXO PLDs have a core power supply voltage (V_{cc}) that is independent of the I/O voltage (V_{ccio}). Each I/O bank of the MachXO PLD can be configured to operate at the unique voltage that is required to interface with the logic device. In addition, the I/O banks can interface with a wide variety of standards including LVCMOS, LVTTL, LVDS, BLVDS, LVPECL and PCI.

Available in commercial, industrial and automotive grades, the MachXO PLDs offer 256 to 2280 look-up tables (LUTs), up to 271 user I/O and are supported in thin quad flatpack (TQFP), thin fine-pitch BGA (fpBGA) and space saving chip-scale BGA (csBGA) packages from 100 to 324 leads.

Using Lattice's TransFR™ technology, the Flash memory in MachXO PLDs can be programmed in the background while the device continues to operate. The new configuration file can be loaded into the SRAM logic, enabling remote field upgrades and minimizing system downtime. Alternatively, toggling the sleep pin (SLEEPN) in MachXO PLDs can be used to load a new configuration file into the SRAM logic without having to cycle the power. The sleep pin is also useful in power sensitive applications and controls the power down or sleep mode of the device. Using the sleep pin, the static power of the MachXO PLD is less than 100 microamps.

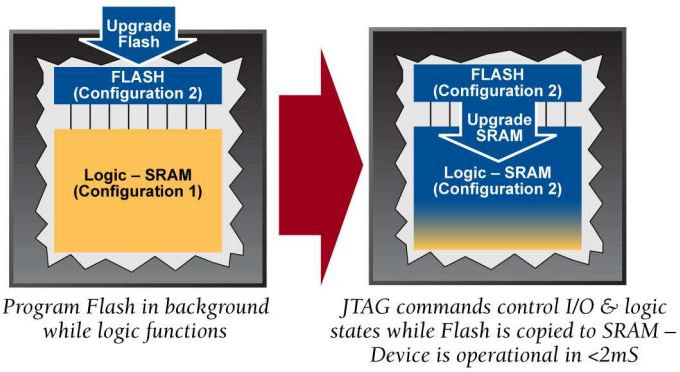

Figure 3 - TransFR operation using MachXO PLDs

MachXO Mini Development Kit and Reference Designs

The MachXO Mini Development Kit provides an easy-to-use and low-cost platform for evaluating and designing with MachXO PLDs. The board comes with the MachXO PLD pre-programmed with a system-on-chip (Mini SoC) demo design that integrates multiple Lattice reference designs, including the LatticeMico8 (LM8) microcontroller, Wishbone interconnect, and peripheral controllers for on-board SPI, SRAM and I2C. . The board features on board peripheral devices like an I2C connected temperature sensor, a programmable SPI Flash memory and SRAM memory. The board can be controlled with switches and a menu driven interface via a Windows or Linux terminal program over an RS-232/USB link.

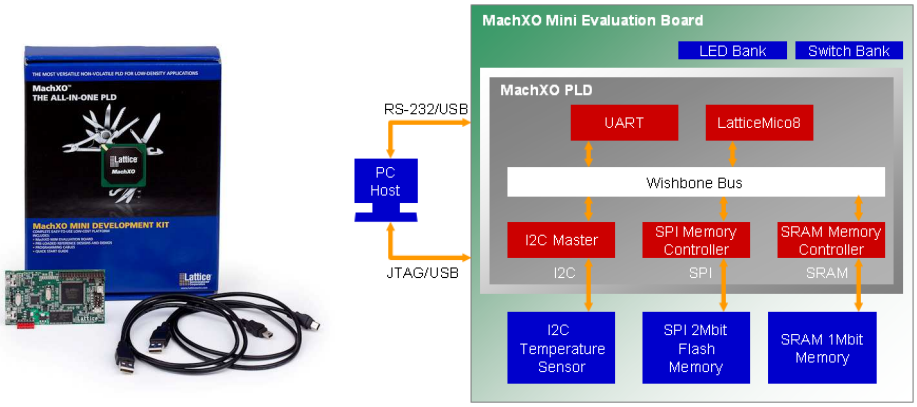

Figure 4 - MachXO Mini Development Kit & evaluation board block diagram

A comprehensive suite of popular reference designs optimized for control and interface bridging applications can be downloaded for free from the Lattice website. The available reference designs include support for popular protocol and connectivity standards such as I2C, SPI, UART and PCI. Table 2 shows the list of available reference designs for the MachXO PLD family.

Control Application	Connect Application
HDLC Controller	PCI Target 32bit-33MHz
LatticeMico8 Microcontroller	I2C Bus Controller for Serial EEPROM
SDRAM Controller	I2C Bus Master with WISHBONE Bus Interface
BSCAN1 (Multiple Scan Port Adressable Buffer)	I2C Master
BSCAN2 (Multiple Scan Port Linker)	LatticeMico8 to WISHBONE Interface Adaptor
Compact Flash Memory Controller	UART
Fast Page Mode DRAM Controller	WISHBONE UART
LPC Bus Controller	Read and Write Usercode
SPI Bus Controller	PCI to NOR Flash
SRAM Controller	

Table 2 - Reference designs optimized for the MachXO PLD family

The reference design source, including HDL, firmware and design tools, can be modified depending on the application requirement. For more information about the reference designs, visit www.latticesemi.com/ip

Summary

Instant-on, non-volatile PLDs are a good choice for implementing platform management functions because they overcome the limitations of ASICs and ASSPs by providing a cost-effective, flexible and single chip solution. MachXO PLDs fit perfectly for implementing functions such as power-up control, general purpose I/O expansion, voltage level translation and interface bridging in telecom infrastructure, server and industrial applications. They provide several key system integration benefits that ultimately reduce total system cost. The MachXO Mini Development Kit and free downloadable reference designs provide

designers a complete and easy-to-use low-cost solution to jump start their designs quickly and effectively.

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