High-Speed SERDES Interfaces In High Value FPGAs

A Lattice Semiconductor White Paper

February 2009

Lattice Semiconductor

5555 Northeast Moore Ct.

Hillsboro, Oregon 97124 USA

Telephone: (503) 268-8000

www.latticesemi.com

Introduction

Serial interfaces are commonly used for chip-to-chip and board-to-board data transfers. As system bandwidths continue to increase into the multi-gigabit range, parallel interfaces have been replaced by high-speed serial links, or SERDES (Serializer/ Deserializer). Initially, SERDES were available as standalone ASSPs or ASICs. The last few years have seen the introduction of FPGA families with built-in SERDES. These devices offer an attractive alternative to standalone SERDES devices. However, these SERDES-based FPGAs have often been expensive, since they were offered as part of high-end (and hence more expensive) FPGA families. Lattice Semiconductor has been a pioneer in this area, and has introduced two low cost FPGA families with SERDES, the LatticeECP2M, introduced in 2007, and the most recent family, the LatticeECP3. The ECP2M and ECP3 FPGAs provide designers with the best of both worlds: a high performance, low-cost FPGA fabric with built-in high performance SERDES. These devices offer designers a low-cost integrated platform to meet their next generation design requirements. Lattice also offers customers a high performance SERDES-based FPGA family, the LatticeSC/M, which offers additional on-chip ASIC IP integration.

The Lattice SERDES have been designed to exceed the stringent jitter and drive requirements of various commonly used protocols. The LatticeECP2M and LatticeECP3 low-cost, high performance SERDES-capable FPGA families provide an excellent platform for customers designing next generation systems. Some of the highlights of the devices are:

- Low Power: 90mW per channel, nominal, at 3.2Gbps.
- Reliable transmission and recovery of serial signals for chip-to-chip and small form factor backplanes (up to 40 inches of FR-4).
- Embedded Physical Coding Sublayer block that supports popular serial protocols such as 1 Gigabit Ethernet, 10 Gigabit Ethernet (XAUI), PCI Express, Serial RapidIO SMPTE.
- Support for Wireless protocols such as CPRI, OBSAI and others, including a low latency variation option for multi-hop implementations.
- Flexible quad-based SERDES: multiple standards/protocols can be mixed in a single quad.
- High-performance, low-cost, low power FPGA that provides industry-leading fabric and IO performance for a low-cost family.
- Complemented by Industry-leading software, Intellectual Property cores and evaluation platforms to enable complete solution designs.

SERDES Architecture

The SERDES is primarily comprised of the Physical Medium Dependent (PMD) sublayer, the Physical Media Attachment (PMA) sublayer and the Physical Coding Sublayer (PCS). The PMD is the electrical block responsible for the serial signal transmission. The PMA is responsible for the serialization/deserialization, and the PCS is responsible for the encoding/decoding of the data streams. Beyond the PCS is the upper layer functionality. For FPGA SERDES, the PCS provides the interface boundary between the ASIC block and the FPGA.

Functionality	Lattice Implementation
Upper Layer Functionality (MACs, etc.)	FPGA logic
Physical Coding Sublayer (8b/10b, alignment, etc.)	Embedded ASIC core/ FPGA logic
PMA/PMD (Serializer/Deserializer, Pre-emphasis, Equalizer, etc.)	Embedded ASIC core

Figure - 1 – Serial Protocol Stack Functional Partitioning

Popular Serial Protocols

Ethernet (1 Gigabit Ethernet and 10 Gigabit Ethernet or XAUI) and PCI Express are among the most popular communications protocols. These protocols have each evolved from parallel bus interfaces to serial interfaces to keep up with ever increasing data rates. These popular protocols share common blocks in the Physical Coding Sublayer. For example, they all use 8b/10b coding. 8b/10b coding provides very good DC balance with a maximum run-length of five and a good transition density. These help improve transmission reliability. As shown in Figure 2, the embedded ASIC blocks on the Lattice ECP2M and ECP3 devices include the PMA & PMD blocks as well as the common blocks of the PCS, e.g., the link synchronization block and the 8b/10b encoder/decoder.

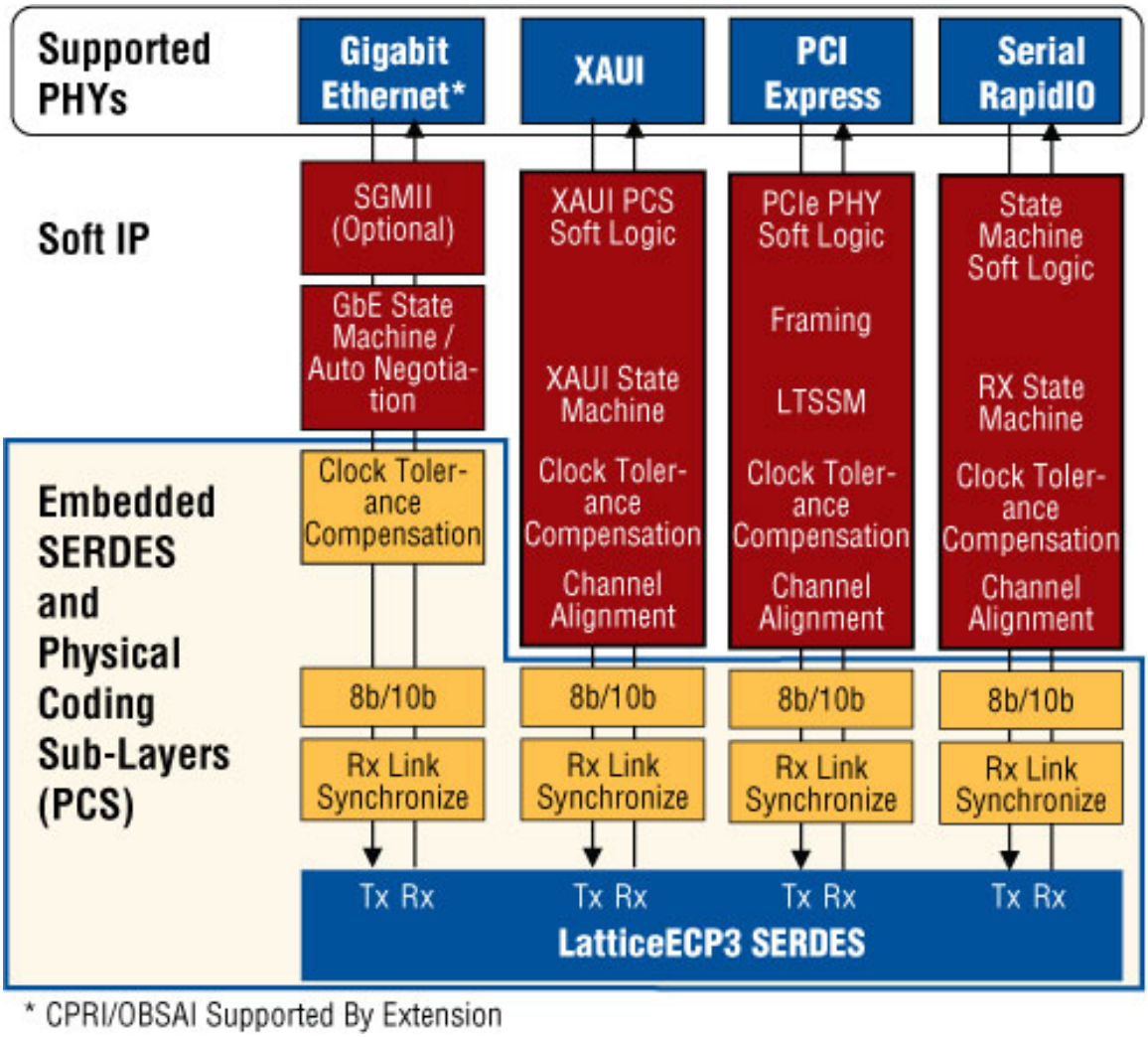

Figure 2 - Popular Serial Protocols Supported by the LatticeECP3

Ethernet

Ethernet is the most widely used communications protocol. Ethernet data rates have evolved from 10 Mbps to 100 Mbps to 1 Gbps (1000 Mbps) to the multi-gigabit ranges: 10 Gbps, 40 Gbps and 100 Gbps. As the data rates have evolved, the links have evolved from parallel interfaces (MII, GMII) to serial links (GE, SGMII, XAUI, etc.).

The LatticeECP3 family is fully compliant with both the Gigabit Ethernet and 10 Gigabit Ethernet protocols. The SERDES is compliant to the IEEE 802.3z specification for 1000 BASE-X Gigabit Ethernet and the IEEE 802.3-2005 specification for 10 Gigabit Ethernet XAUI. As shown in Figure 2, the LatticeECP3 devices support the Ethernet Physical Layer by embedding the SERDES and other blocks such as the Link synchronization, 8b/10b encoding/decoding and clock tolerance compensation as ASIC blocks on the

device. When combined with the Lattice GE/SGMII PCS and MAC IP, the LatticeECP3 provides the user a fully integrated, fully compliant Gigabit Ethernet solution.

The LatticeECP3 SERDES exceed the jitter specifications defined by the IEEE 802.3-2005 specification for XAUI. The Lattice XAUI IP and 10 Gigabit Ethernet MAC IP cores provide a fully integrated, fully complaint 10 Gigabit Ethernet platform. The LatticeECP3 is the industry's lowest cost FPGA platform with fully compliant 1 Gigabit and 10 Gigabit Ethernet support.

PCI Express

PCI Express is the next generation Peripheral Component Interconnect (PCI) standard. The PCI Express protocol was conceived to address ever increasing bandwidth requirements by providing a scalable, point-to-point serial connection between chips, over cable or via connector slots for expansion cards, while maintaining compatibility with conventional PCI at the software layer.

A single PCI Express serial link is a dual-simplex connection, specified to speeds of 2.5Gbps (or 5Gbps or beyond for v2.0 and later specs) per link that can be scaled in x1, x2, x4, x8, x12, x16 and x32 lane widths to achieve greater bandwidth. A serial implementation is cheaper, can be driven further distances and alleviates common mode noise and skew concerns inherent in existing source synchronous parallel interfaces (such as conventional PCI), as well as reducing the overall number of connections required. The LatticeECP3 SERDES are fully compliant to the PCI Express v1.1 jitter specifications. Combined with the Lattice PCI Express Endpoint Controller IP, this provides designers with a low-cost platform for PCI Express.

Lattice also provides a complete PCI Express development kit for designers. As shown in Figure 3, the Lattice PCI Express Development Kit is a fully integrated development platform that offers a complete hardware/software development environment to accelerate the evaluation of PCI Express technology. The kit includes the various components required for PCI Express system design, including the Lattice PCI Express Endpoint IP core, RTL source, project directories and documentation for several demos ranging from control plane through data plane applications, drivers, GUI and an evaluation board.

Figure 3 - Lattice PCI Express Development Kit

Wireless Protocols: CPRI & OBSAI

Common Public Radio Interface (CPRI) and the Open Base Station Architecture Initiative (OBSAI) are two popular packet-based protocol standards for the wireless infrastructure. These standards are also supported by the LatticeECP3 SERDES. As shown in Figure 4, the CPRI/OBSAI Physical Layer support is included in the LatticeECP3 SERDES/PCS ASIC blocks. Lattice also provides CPRI (v3.0 specification) and OBSAI (OBSAI-RP3-01) IP cores that provide full support for the respective protocol stacks.

Additionally, the LatticeECP3 SERDES also supports the low-latency variation requirements for multi-hop implementations. In the new Remote Radio Head (RRH) topologies there is a system requirement to be able to measure and offset delay variations incurred in multi-hop scenarios. To support this, the ECP3 PCS blocks were very carefully designed to make the link delay variations deterministic and consistent. Additionally, the Word Aligner delay variation is measurable and once this value is known, it is reported in offset registers so that an offset can be applied at the system level.

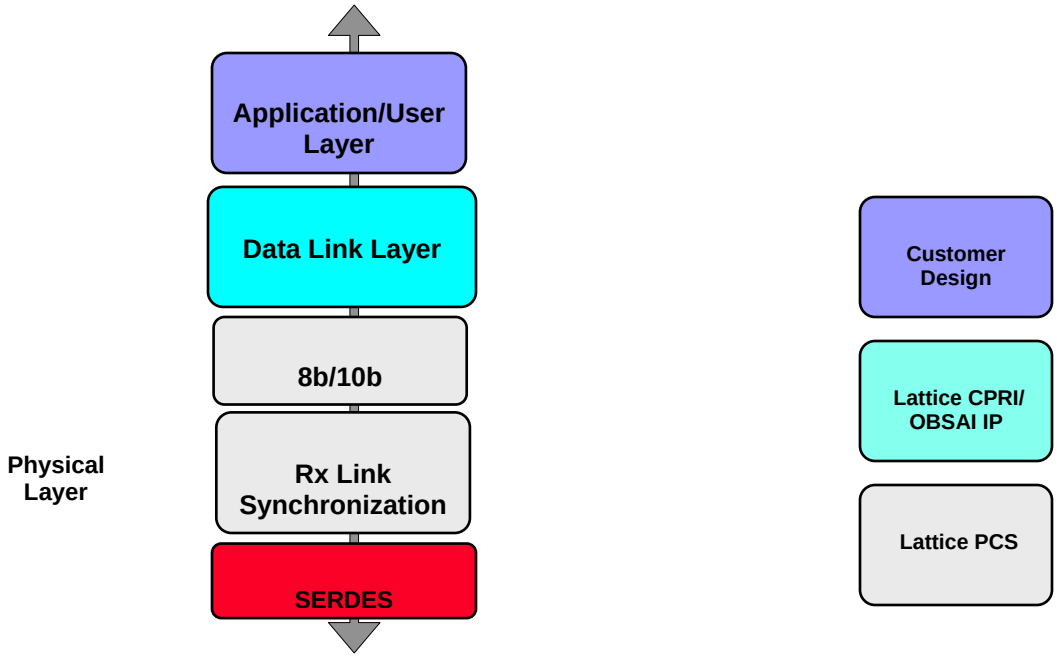

Figure 4 - CPRI/OBSAI Protocol Stack Supported by the LatticeECP3

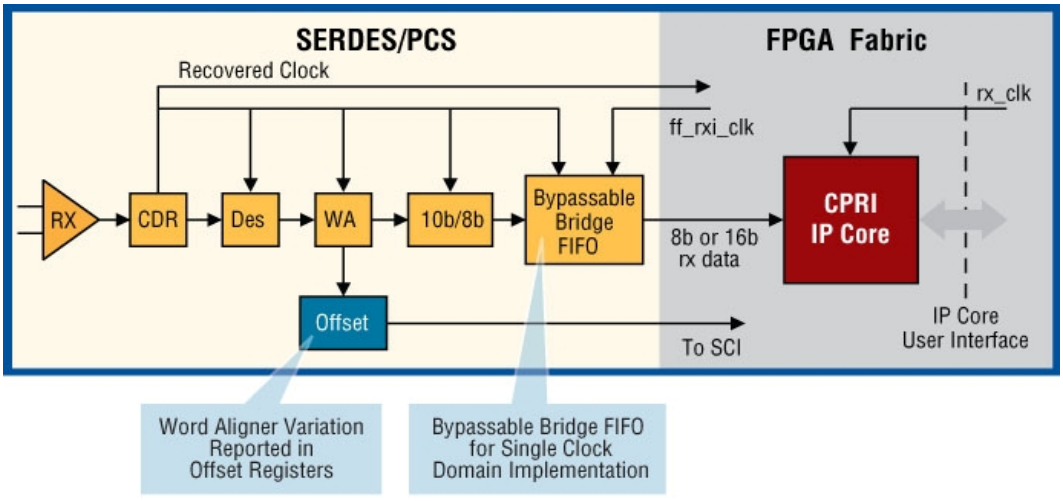

Figure 5 - Low Latency Option Implemented in ECP3 SERDES/PCS

SMPTE

The Society of Motion Picture and Television Engineers (SMPTE) has developed a set of standards built around SDI, or Serial Digital Interface. These consist of: SMPTE 259M – Standard Definition Serial Digital Interface (SD-SDI), the SMPTE 292M – High Definition Serial Digital Interface (HD-SDI), and the SMPTE 424M – 3Gbps Serial Digital Interface (3G-SDI).

SMPTE 259 transmits data over a serial link at a rate of 270 Mbps, the SMPTE 292 increases that to 1.485 Gbps, and the SMPTE 424 increases that to 2.97 Gbps. The LatticeECP3 devices simultaneously and dynamically support all those rates without oversampling. The LatticeECP3 SERDES are fully compliant to the SMPTE jitter specifications. The SERDES IOs can also be DC-coupled (with external capacitors) to supporting SMPTE pathological signals. Additionally, the ECP3 SERDES have been architected for channel independence. As shown in Figure 6, the device includes the appropriate clock dividers (DIV1, DIV2 and DIV11) to allow one to implement truly Independent Transmit Multi-Rate Support for SD/HD/3G. The receive clocking is independent per channel and can be sourced externally or from the FPGA, allowing independent multi-rate Receive support for SD/HD/3G.

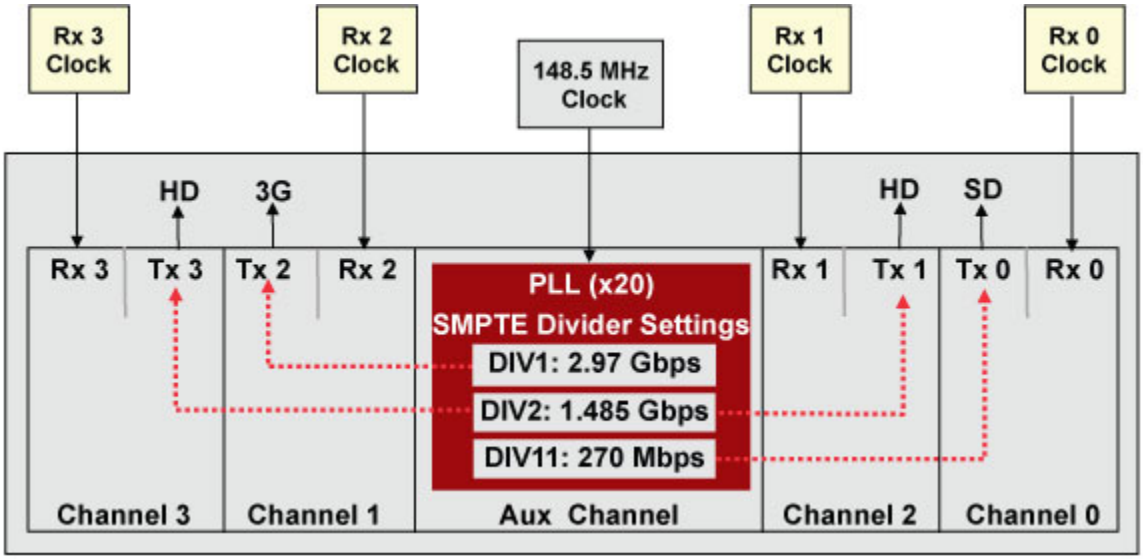

Figure 6 - Enhanced SMPTE Multi-rate Support in the LatticeECP3 SERDES

As shown in Figure 7, the SMPTE protocol stack can be fully implemented in the LatticeECP3 FPGAs. Lattice provides a Multi-Rate Serial Digital Interface (SDI) PHY Layer IP core that implements NRZ/NRZI encoding, word alignment and framing. The LatticeECP3 is the industry's lowest cost, lowest power and most flexible programmable development platform for SMPTE.

Lattice has also developed a complete system to demonstrate compliance to SMPTE standards. This system consists of the LatticeECP3 Video Protocol board, along with the IP and demo designs.

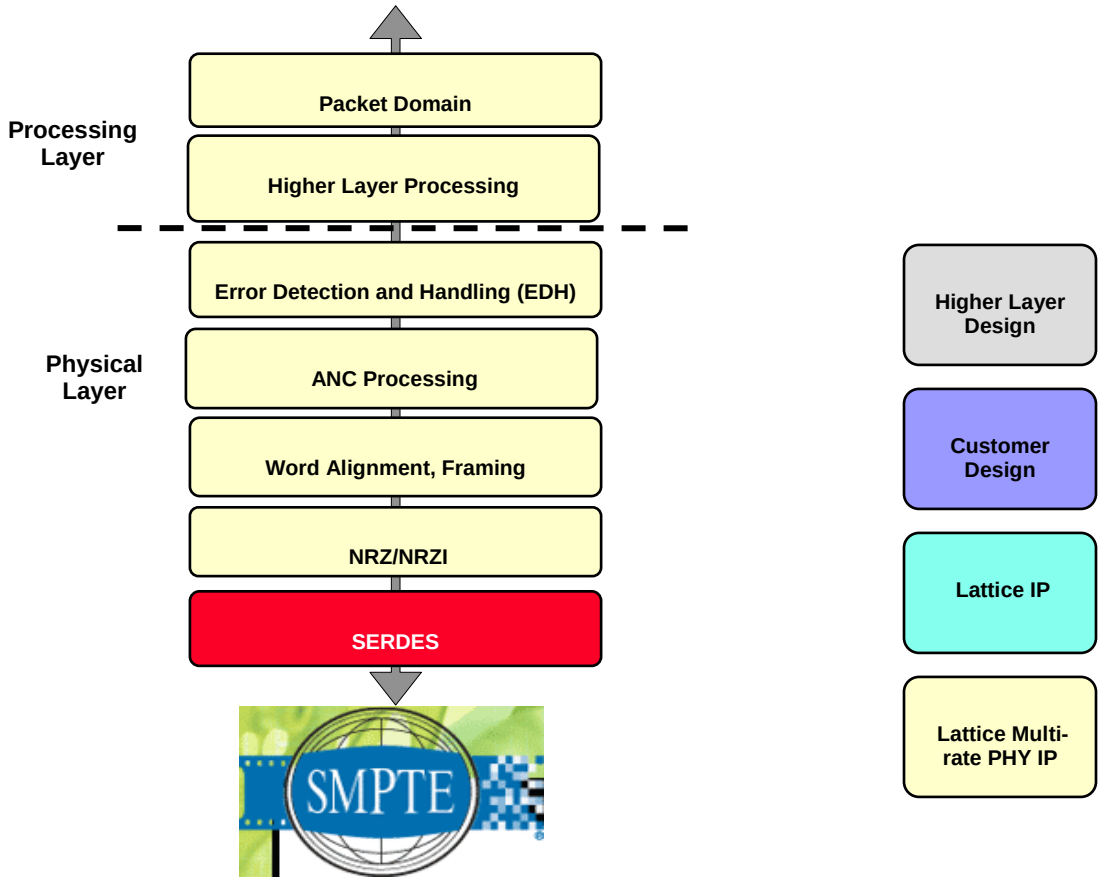

Figure 7: SMPTE Protocol Stack Supported by the LatticeECP3

Conclusion

SERDES are becoming increasingly popular interfaces and are experiencing wider adoption in networking applications. The LatticeECP3 SERDES-capable FPGAs provide designers with a robust yet low-cost platform for developing various SERDES-based

applications. Common serial protocols for Ethernet, PCI Express, SMPTE and wireless applications are supported in a powerful yet low cost FPGA platform.

###