POWER CONSIDERATIONS IN FPGA DESIGN

A Lattice Semiconductor White Paper

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Power as a Design Component

Power has always been a design consideration. Traditionally, though, a lower priority has been assigned to power than to most other variables (speed/performance, cost, time-to-market, risk, etc.). In today's marketplace, however, power has become a very important component in the designer's decision making process. There is good reason for this. Power translates to significant system cost. Here are two examples:

> The United States Federal Government spends an estimated $479M per year to power its datacenters[1]. Of the $479M annually, 25% of the money is directly attributed to powering the datacenter servers, while 50% of the money is associated with powering cooling system, fans, etc. to remove the heat generated by running the servers.

> On average each fully loaded 3G cell site, using traditional PAs (Power Amplifiers), costs approximately $1600/yr US or $3200/yr in Europe[2]. This suggests a typical European operator running 20000 cell sites would consume 58MW, which translates to about $62M USD per year. In addition to these costs, the level of consumption per cell site leads to an estimated 11 tons of carbon dioxide emissions per cell site per year.

It is clear that systems operators regard power as a significant operating expense. These constraints trickle down to system designs and the boards that comprise those systems. In addition to operational costs, design complexity increases when dealing with thermal issues caused by excessive power. Port density and bandwidth requirements go up from marketing, yet form factors go down, pressuring engineers to accommodate both schedule and budget for their projects.

FPGAs are a popular choice in numerous system designs. A wise selection of FPGAs can significantly aid the designer in reducing the challenges associated with power consumption.

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[1] For more information click on DataCenter Power Example
[2] For more information click on: 3G Cell Site Power Consumption

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The New LatticeECP3 Family is the Lowest Power, Highest Value FPGA Solution Available Today

Claims of "lowest power" are common, and designers may be understandably, skeptical. However, the comparisons described below are transparent to the user (you can duplicate these results on your own using each vendor's power calculator software), and although there are numerous variables of density, device, temperature, Activity Factor, etc., a reasonable compromise on a typical application has been made. Your situation will certainly be different, and so Lattice encourages you to experiment on your own. Lattice has posted the design example source code on-line, http://www.latticesemi.com/products/fpga/ecp3/lowpower.cfm, to enable customers to experiment with their own design constraints more easily.

Power Components in FPGA Devices

There are traditionally four power components that are important when considering a design using FPGA products. These components are:

1. Pre-Programmed Static (Quiescent) Device Power Consumption
2. Inrush Programming Current: (the surge current/power required when programming a device until programming in complete)
3. Post-Programmed Static Power Consumption: Power being consumed by the device with a 'zero MHz' frequency
4. Dynamic Power Consumption: Incremental power consumed by a non-zero frequency component. (i.e. $P=kcV^2f$)

Pre-Programmed Static Quiescent Device Power Consumption is the amount of power consumed by the FPGA prior to the device being programmed. For quiescent device power consumption the FPGA is in a non-programmed state, yet has been powered. It is important that the device not consume significant power during this time, as conceptually the FPGA device could draw excessive

power and potentially crow-bar (shut down) power supplies, preventing the board from successfully initializing itself and the system.

Inrush Programming Current has in the past been an issue for FPGA vendors. Inrush programming current had actually been larger than a typical application's power consumption, effectively sizing the power supplies/regulators. This was of course a non-desired effect, and all vendors put considerable energy into designing their products so that programming current (inrush) was well under any typical application's power consumption. This white paper will not discuss inrush as a component, as it would be unusual to see this as a dominant design consideration in today's FPGA devices. Lattice does, however, continue to spec and track inrush needs in its datasheets and Software (PowerCalc).

Post-Programmed Static Power Consumption is a very significant component of FPGA power consumption. This is due to the large number of transistors on FPGAs (typically 8x to 10x for an equivalent ASIC logic implementation, config and muxing not included) that all have a small amount of leakage current. The leakage on these transistors (pass muxes for switches, RAM cells, etc.) typically is 'always on' and drawing power whether the transistor is used or not. Typically, post-programmed static power is equal to or greater than the previously described Quiescent Device Power. There are some recent innovations addressing power grids and removing power to the transistor, etc., which will impact static power. This paper will not address these techniques in the interest of brevity. Regardless of the technology, however, in the end the user wants to see low power, independent of the techniques, on a realistic design. This will be shown shortly.

Dynamic Power Consumption is the last power component on the list above. Dynamic power tracks kcV^2f, and typically is under the designer's control. Dynamic power is a significant component in power analysis and, depending on the type of design being implemented (always on, always processing, datapath-

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type of design vs. a wake up, process and go back to sleep type of design),, ranks either #1 or #2, with static power being the other component.

Power is Impacted by Your Environment

As with any silicon, power consumption is closely linked to temperature. As the device heats up, power increases due to increased leakage of the transistors. In extreme cases a device can get so hot that it exceeds manufacturer thermals and the transistors can not turn off, a situation referred to as thermal runaway. It is strongly recommended that power analysis be completed as part of the design process for any FPGA. By doing so, one can have an extremely high confidence the design will work within the design environment.

Temperature can be controlled using various techniques such as fans, heat sinks, modification of the design, I/O standards, etc. Later in this paper temperature effects will be analyzed as part of comparison graph data.
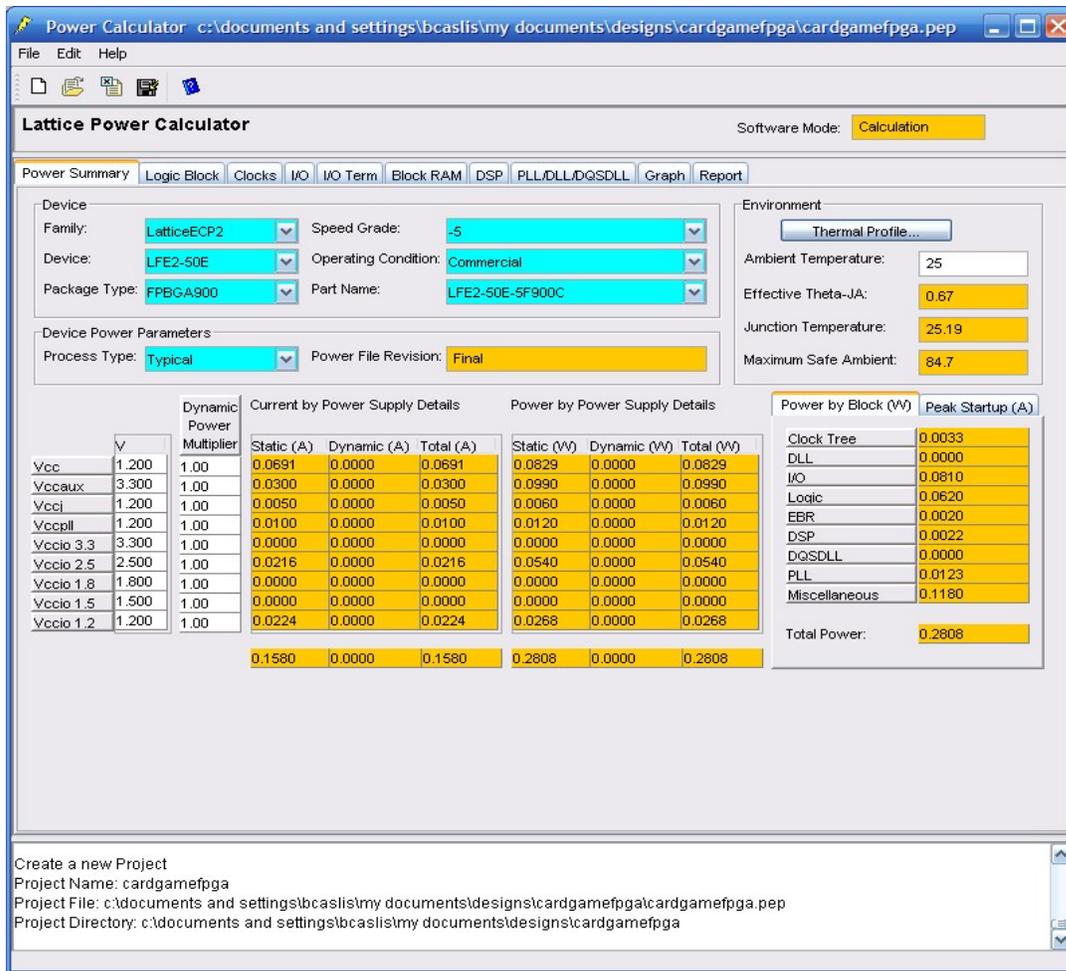
The Methodology

Each FPGA vendor offers different (sometimes significantly different) FPGA architectures. The components can be different enough that a direct comparison is not practical, as there would be significant changes to the source implementation. Examples would be DSP blocks, EBR block sizes, SERDES, number of global clock routes and even basic LUTs. The approach chosen for the below comparison was to simplify the variables and focus on what is common for a majority of users. These areas of focus are LUTs, registers, I/Os, routing and total EBR memory. Parameterizable source code was used to scale easily in order to address multiple devices in the families. DSP and SERDES analysis is more closely tied to the end application and is not addressed in the following graphs.

Using a self-generating pattern, power could then be measured across all devices and chosen vendors on evaluation boards; however, there are numerous

issues with different evaluation boards. For example, power rails may not be totally isolated from other board components. For these reasons, an approach that can eliminate these complications is needed.

Power Calculators

Additionally, the engineer wants to know what the power is <u>prior</u> to board build, as the designer's management is not interested in surprises after the board/system is built and the design exceeds a power budget and/or has thermal issues. This design challenge has driven the need for software-based power calculators. Software-based power calculators can be used up front in the pre and post FPGA design process to analyze the power expected when the PCB returns from assembly. *Assuming the calculators are accurate*, one can use these tools to make meaningful comparisons.

Power Calculator c:\documents and settings\bcaslis\my documents\designs\cardgamefpga\cardgamefpga.pep

File   Edit   Help

Lattice Power Calculator   Software Mode: Calculation

Power Summary | Logic Block | Clocks | I/O | I/O Term | Block RAM | DSP | PLL/DLL/DQSDLL | Graph | Report

Device
Family: LatticeECP2   Speed Grade: -5
Device: LFE2-50E   Operating Condition: Commercial
Package Type: FPBGA900   Part Name: LFE2-50E-5F900C

Device Power Parameters
Process Type: Typical   Power File Revision: Final

Environment
Thermal Profile...
Ambient Temperature: 25
Effective Theta-JA: 0.67
Junction Temperature: 25.19
Maximum Safe Ambient: 84.7

	V	Dynamic Power Multiplier	Current by Power Supply Details			Power by Power Supply Details		
			Static (A)	Dynamic (A)	Total (A)	Static (W)	Dynamic (W)	Total (W)
Vcc	1.200	1.00	0.0691	0.0000	0.0691	0.0829	0.0000	0.0829
Vccaux	3.300	1.00	0.0300	0.0000	0.0300	0.0990	0.0000	0.0990
Vccj	1.200	1.00	0.0050	0.0000	0.0050	0.0060	0.0000	0.0060
Vccpll	1.200	1.00	0.0100	0.0000	0.0100	0.0120	0.0000	0.0120
Vccio 3.3	3.300	1.00	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
Vccio 2.5	2.500	1.00	0.0216	0.0000	0.0216	0.0540	0.0000	0.0540
Vccio 1.8	1.800	1.00	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
Vccio 1.5	1.500	1.00	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
Vccio 1.2	1.200	1.00	0.0224	0.0000	0.0224	0.0268	0.0000	0.0268
			0.1580	0.0000	0.1580	0.2808	0.0000	0.2808

Power by Block (W) | Peak Startup (A)

Clock Tree	0.0033
DLL	0.0000
I/O	0.0810
Logic	0.0620
EBR	0.0020
DSP	0.0022
DQSDLL	0.0000
PLL	0.0123
Miscellaneous	0.1180
Total Power:	0.2808

Create a new Project
Project Name: cardgamefpga
Project File: c:\documents and settings\bcaslis\my documents\designs\cardgamefpga\cardgamefpga.pep
Project Directory: c:\documents and settings\bcaslis\my documents\designs\cardgamefpga

Perhaps an alarm has been triggered with the previous statement, '*Assuming the calculators are accurate*'. Some of you may even have had some unpleasant experiences in the past with the accuracy of some vendor's power calculators. Lattice has been refining the accuracy of its software power calculation tool (screenshot above) for several years. We believe it is the best and most accurate tool in the market. This will be discussed further when power calculator terminology[3] is discussed.

The methodology used for most of the data in this white paper is to use each vendor's power estimation/calculation tools. At the end of the exercise, a comparison was made between the power calculated mode and silicon

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[3] To learn more about the Lattice Power Calculator software click on the following website link:
Lattice Power Calculator software

measured mode to validate the accuracy. Total Power was measured from 25°C to 85°C.

Assumptions

As part of creating an objective example used for comparison, design and software assumptions are:

Design Assumptions:
- Quiescent Devices are un-programmed (blank) devices
- A patterned device is used for Static, Dynamic and Total Power analysis
- The pattern used is parameterizable counters, targeted to achieve a 12.5% Activity Factor (AF). This maps to a 6 bit counter. Groups of 6 bit counters are routed out to I/Os for similar Activity Factors
- A 70% LUT utilization is targeted at each vendor's devices
- A 70% I/O usage is used on each vendor's largest package in their given family
- A 70% utilization of available EBR bits, configured as a Dual-Port RAM
- Fabric clock frequency is 100 MHz
- DSP blocks were not used in the analysis. Although we believe such an analysis is favorable for Lattice, there are numerous differences across the vendors' architectures and perhaps a FIR or other DSP function might be better suited for future comparisons
- SERDES blocks were not included in this analysis
- 5pF of additional load placed on the I/Os being used
- Junction Temperature used to eliminate Package permutations
- LVCMOS2.5 being used for I/O analysis

Software Assumptions

The latest available production software was used for Lattice, Altera and Xilinx. These versions are:

Synthesis, Place and Route:

- Lattice: ispLever 7.2

- Xilinx: ISE Design Suite 10.1

- Altera: Quartus II 8.1

Power Calculation Tools:

- Lattice: Power Calculator (included in ispLever 7.2)

- Xilinx: Xpower (included in Xilinx ISE Design Suite 10.1)

- Altera:

  o Power Play (included in Altera Quartus II 8.1)

  o ArriaIIGX beta power spreadsheet

Power Calculation Terminology

Most power calculators have several different modes of operation. These modes have different accuracies. There is no standard industry-defined terminology for the different power modes. A definition of what is referred to in this white paper as 'Estimation', 'Calculation' and 'VCD' is provided below. These modes are consistently applied to each vendor:

The Lattice Power Calculator tool supports three modes:

Estimation Mode:

- Example: 20 EBRs, 20K LUTs, 4 PLLs, 20% AF, etc.

- Used in Architectural Analysis, i.e. pre-netlist

- Estimates Routing

- Activity Factor (AF) needs to be provided

- Lattice Goal is accuracy to about +10%
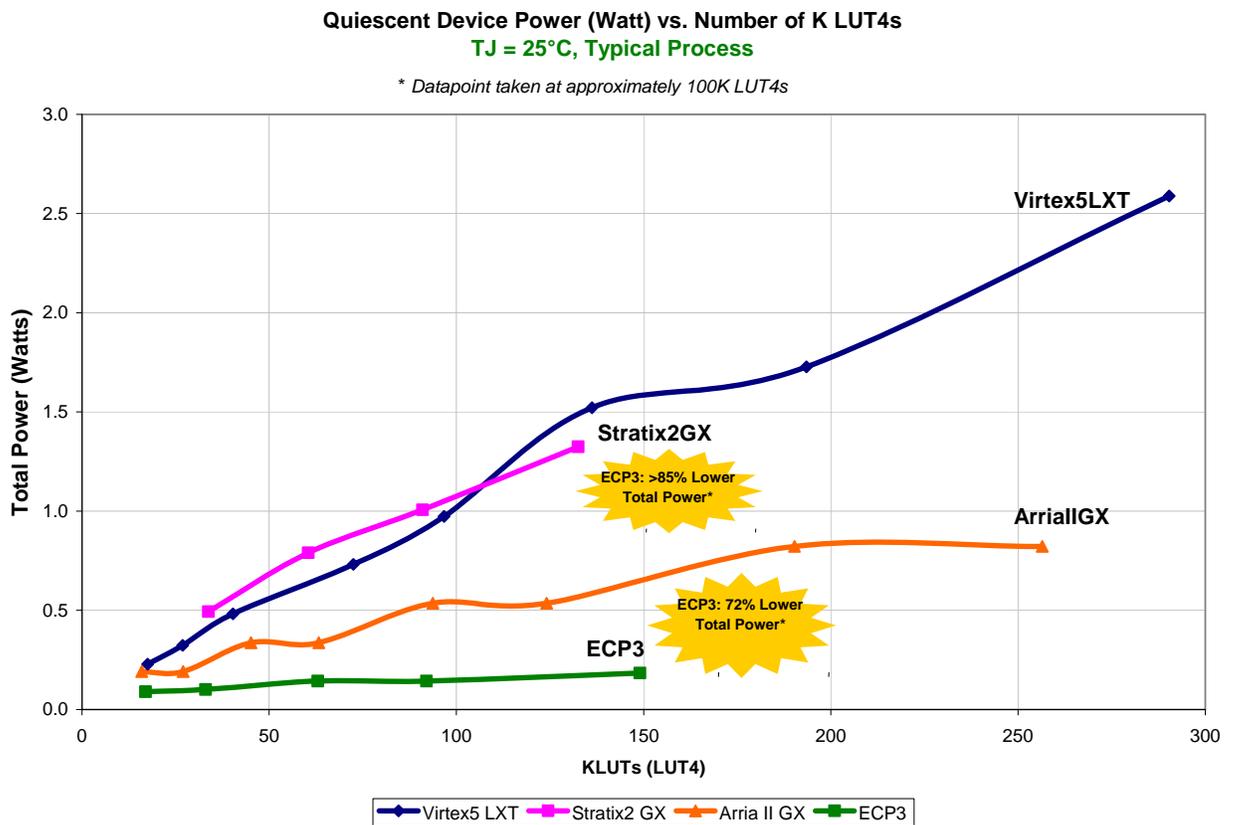
Calculation Mode:

- Design Needs to be complete and synthesized, placed and routed

- Netlist taken into the tool, uses real, routed data

- AF needs to be provided

- Lattice goal is accuracy to +-5% Typical, +10% Worst Case Process

VCD Mode:

- Same as Calculation Mode for netlist
- User provides pattern to simulate, and logs nodes to a file. Reads VCD file (Verilog Change Dump) to determine AF on a net by net basis
- Development is a high priority. Currently being enhanced
  - (AF supported on top level currently)
- Accuracy goal not yet targeted

Most of the following data assumes 'Estimation Mode' unless otherwise noted. The accuracy of the Xilinx and Altera power calculator tools and their targeted goals are not addressed in this paper.

Quiescent Device Power (Watt) vs. Number of K LUT4s
TJ = 25°C, Typical Process

* Datapoint taken at approximately 100K LUT4s

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The above chart illustrates the power benefits of the LatticeECP3 compared to the Altera StratixIIGX, ArriaIIGX and Xilinx Virtex5LXT families. The chart graphs the vendors' specific devices in equivalent LUT4s[4] to Power (in Watts) at 25°C, typical process, using an Estimated Mode for a pre-programmed static device.

Quiescent Device Power at approximately 100K LUT4s:

Device	Quiescent Power in mW	ECP3 % Lower than Comp	Comp X higher than ECP3
Lattice ECP3-95	147	NA	NA
Altera EP2AGX95D	533	72%	3.6X
Xilinx V5LXT110	975	85%	6.6X
Altera 2SGX90E	1007	86%	6.8X

Why show quiescent power? As mentioned previously, quiescent power is an important component of power analysis. Additionally, static and dynamic power (post-programmed) should be reviewed. Below is a chart of Static vs. Dynamic as a percentage of Total Power for the LatticeECP3 family using the reference design. (Please see 'Design Assumptions' listed above. They are applicable for the following table).

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[4] Both Lattice and Altera use a 4-input LUT structure in the above devices. Xilinx V5 has a LUT6-based architecture. There can be much debate about what is the appropriate equivalent conversion ratio to apply. They are heavily dependant on several factors. Lattice believes a LUT6 is on average worth about 1.1 to 1.33 LUT4s. For the purposes of eliminating a debate on this item, a more favorable Xilinx ratio (1.4X) was used. Using the 1.4X conversion ratio would plot the V5LXT110 at 97.8K LUT4s. An identical multiplier was used on the remaining Xilinx devices.

Static and Dynamic as % of Total
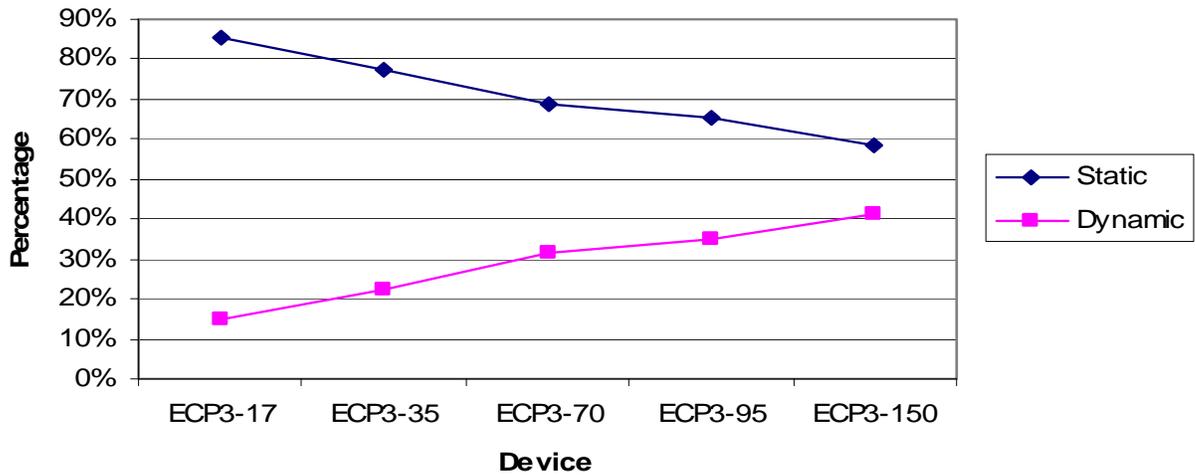
For the Lattice devices, static power is significant at the smaller device sizes and decreases as the device size increase. The static percentage goes down marginally, which is non-intuitive, but can be explained by fixed power consumption on items such as VccAux, (biasing circuits) reference circuits, analog circuitry for PLLs, etc. Changes in AF and frequency would obviously skew the charts and more heavily weigh the dynamic component over static for this particular example.

In the first slide we showed the tremendous savings of quiescent power over our competition. It would be prudent to ask the question "What about total power over temperature? This is a very important item also that should be evaluated in a system. How does this compare?"

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Total Power vs. KLUTs
70% Utilization Pattern (No SERDES)
Typical Process, TJ = 85°C

* *Datapoint taken at approximately 100K LUT4s*
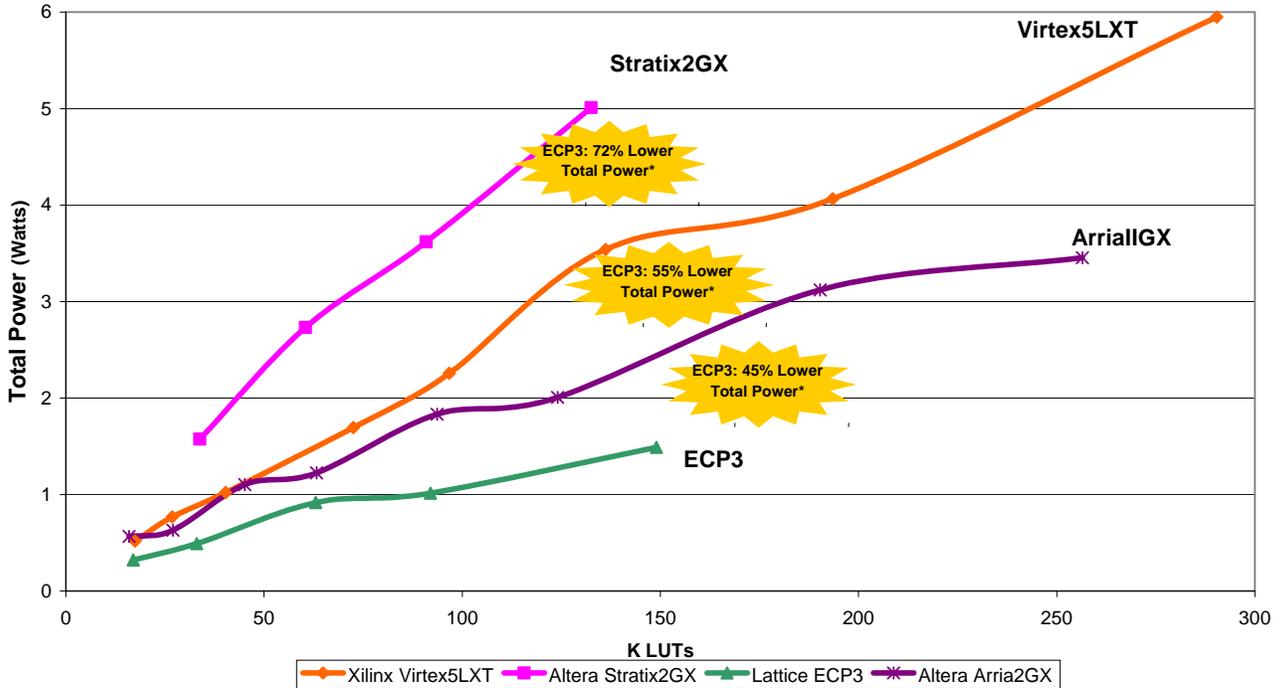
The above graph uses Estimated Mode and summarizes the total power consumed based on the 70% utilization pattern (assumptions highlighted above) at 100Mhz. Junction temperature is picked at 85°C. The LatticeECP3 continues to have a huge savings in power compared to the competition.

Device	Total Power (W)	ECP3 % Lower than Comp	Comp X higher than ECP3
Lattice ECP3-95	1.013	NA	NA
Altera EP2AGX95D	1.833	45%	1.8X
Xilinx V5LXT110	2.256	55%	2.2X
Altera 2SGX90E	3.619	72%	3.6X

Accuracy

As discussed earlier, much of this data has been charted from power estimation software. Currently the ECP3-70 and ECP3-95 are available in silicon. All other

Lattice data points are estimated based on process technology and design information. In order to confirm that using an estimated methodology is a valid, accurate approach, Lattice took some hardware measured data points on the ECP3-95 in the 1152 package (replaced in production with an 1156) in a controlled environment and overlaid this with the Lattice Power Calculator software.

'Calculation Mode' Typical Process Total Power (mA) vs. TJ (°C)
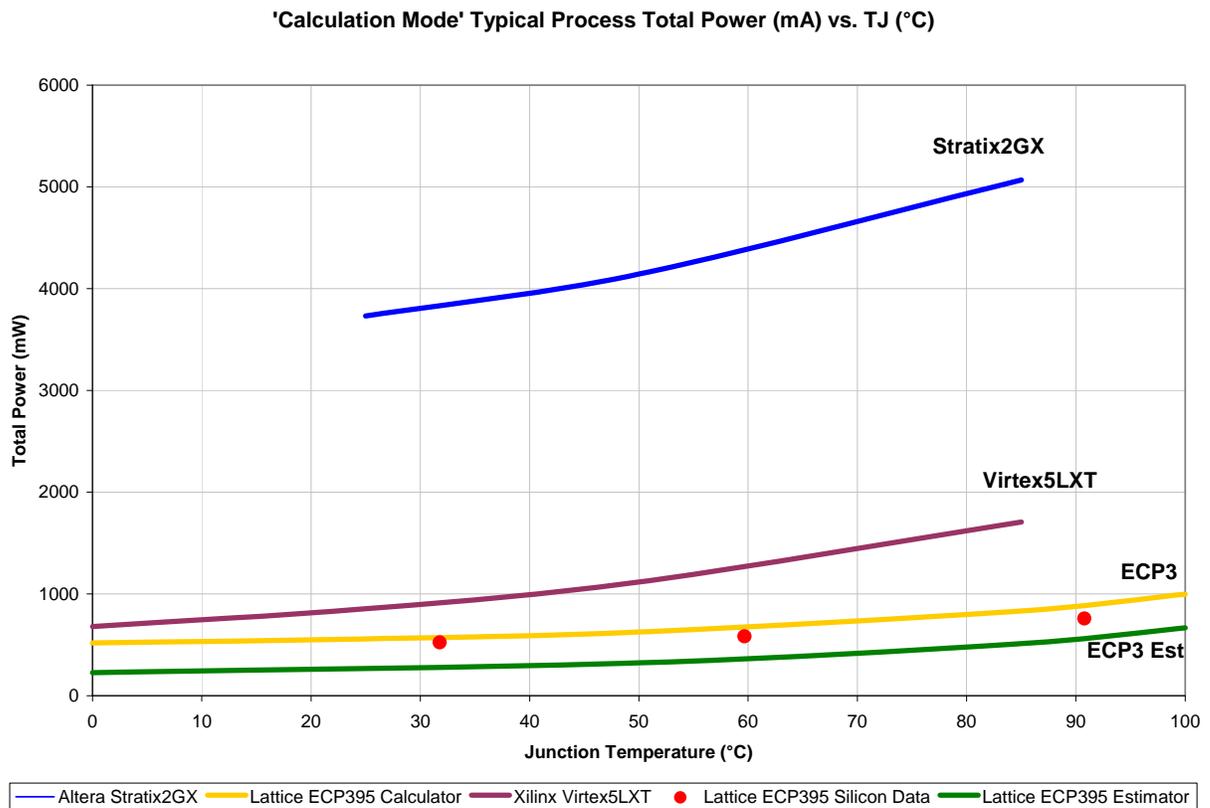
A thermal diode was used to calibrate junction temperature with stream temperature. Target junction temperatures were 25°C, 55°C and 85°C. Any errors in targeted junction temperature vs. measured junction temperature were interpolated.

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One part was measured where this part is within the typical process parameters. The chart above has Xilinx, Altera and Lattice Power Calculation Mode (post-route) curves for the above design[5] Estimation Mode was also overlaid for the purposes of calculating Estimation vs. Calculation accuracy.

The three data points (highlighted in Red) are the measured power on the load board. The Yellow and Green curves (Lattice Calculated and Estimated, respectively) straddle the measured power data points.

In terms of accuracy, at 85°C the Lattice 'Calculate Mode' is approximately <10% error. The 'Calculation Mode' for this data point was overestimated, i.e. true power was less than the predicted consumption. For Lattice 'Estimation Mode' (the green curve) is under the measured values, at approximately <15% error. This is acceptable, considering that no routing has been done to the design and routing is estimated.

ArriaIIGX was not charted, as the purpose was to overlay post-route power numbers and, additionally, add Lattice measured numbers and compare for accuracy. Currently the ArriaIIGX power calculator is in beta mode and does not support a post-route capability.

Considering that only one Lattice part was measured (soldered into the board) and potential slight errors in measuring, one can conclude the methodology established (using Power Calculator) is a very viable, accurate approximation of the expected results of LatticeECP3 devices. The results are within desired Lattice accuracy goals. Customer feedback on the Lattice Power Calculator and targeted accuracy has been that it is the best in the industry.

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[5] The design used on all of the previous charts could not be used on our available ECP3-95 AC load board due to a limited number of I/Os available on this board. The design used for the above graph is as close as possible to being identical to the estimated examples; however, due to the limited number of I/Os on this load board, a subset of I/Os (35) was brought out to test points.

Summary

In summary, power is an important consideration in today's marketplace. The important components of power in FPGA systems, Static and Dynamic, have been charted against other FPGA products. The charted results were:

- **ECP3 is 72% to 85% Lower Quiescent Power than the competition** (15%-28% of the Static Power of the competition)
- **ECP3 is 45% to 75% Lower Total Power than the competition** (25% to 55% of the total power of the competition)

It has been proven that Lattice Power Calculator software is a very accurate approach to estimating designs early in the design process. Accuracy in pre- and post-route was confirmed with real data measurements

We believe Lattice has the best low power, high value FPGAs. But see for yourself. The Lattice Power Calculator software is available free (available stand-alone as well) for download. Additionally, the example used has also been made available.

For more information on LatticeECP3 go to the Lattice website at
http://www.latticesemi.com/products/fpga/ecp3 or contact Sales at
http://www.latticesemi.com/sales