Using a Low-Cost CMOS Oscillator as a Reference Clock for SERDES Applications

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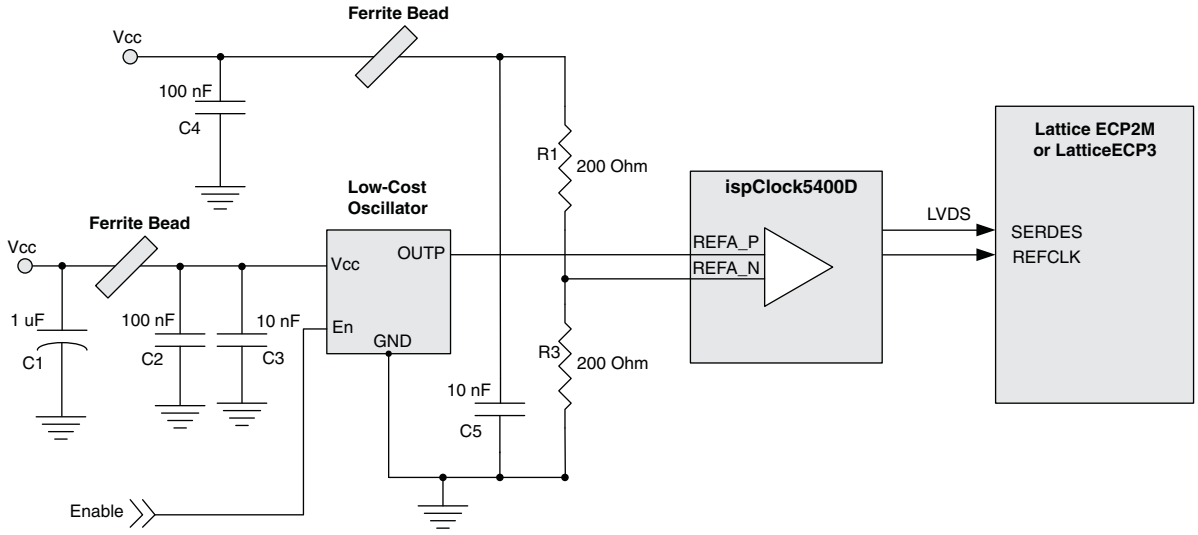
The Lattice ispClock™5400D family integrates a CleanClock™ PLL and a FlexiClock™ Output block. The CleanClock PLL provides an ultra-low-jitter clock source to a set of four V-dividers. The FlexiClock output block receives the clock output from these V-dividers through an output switch matrix and distributes them to the output pin using a programmable logic interface. There are two members in the ispClock5400D family, the ispClock54010D (10-output FlexiClock block) and the ispClock5406D (6-output FlexiClock block). Each of the outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, SSTL, HSTL, MLVDS, HCSL) and output frequency.

Typically, expensive oscillators with LVDS or LVPECL interface are used as a reference clock for FPGA SERDES interface applications. The ispClock5400D device provides ultra-low-jitter differential clock outputs that can be used to drive both the general purpose clocks and the SERDES reference clocks for FPGAs. The inputs of the ispClock can also be connected to a low cost CMOS oscillator. This application note will show how to interface a low-cost CMOS interface oscillator to the ispClock5400D and present some of its design considerations.

The FPGA SERDES reference clocks usually require lower jitter than many low-cost oscillator sources can provide. In order to keep the jitter output of the ispClock5400D device low, it is important to use good design practices when interfacing with a low cost oscillator with CMOS interface. Figure 4-1 shows an example circuit for interfacing a low cost CMOS interface oscillator to the ispClock5400D device.

Figure 4-1. Interfacing a Low-Cost CMOS Interface Oscillator to the FPGA SERDES Reference Clock



When designing the board for this system there are some important considerations to take into account.

1. The oscillator and ispClock5400D devices should be mounted close to each other to reduce the possibility of picking up noise on the system which will show up as jitter on the input to the ispClock5400D device.
2. The ground signal on the voltage divider circuit should be connected to the ground of the oscillator and located physically close to both devices. This circuit is used to insure that any noise that is picked up will show up as common mode noise and hence not add to the signal amplitude which would appear as jitter to the ispClock5400D.

3. Bypass capacitors should be used on the voltage divider circuit to provide additional noise rejection capability.

4. The use of a ferrite bead inductor is recommended on the power supply to the oscillator and also the voltage divider circuit as shown in Figure 4-1.

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Revision History

Date	Version	Change Summary
February 2009	01.0	Initial release.
February 2012	01.1	Updated document with new corporate logo.