LatticeMico8 to WISHBONE Interface Adapter

February 2010 **Reference Design RD1043**

Introduction

The LatticeMico8™ 8-bit microcontroller is an open IP licensed core that is easily configured for FPGA devices. This versatile microcontroller provides a wide range of capabilities with minimal device resources.

The WISHBONE interface is a flexible, multipurpose general interface bus. With the increasing number of WISHBONE-capable open-source designs and intellectual property (IP), system design can be greatly simplified.

To bridge the power and interoperability of both the LatticeMico8 and the WISHBONE interface, this reference design provides logic to adapt the LatticeMico8 external I/O to a WISHBONE master interface.

Functional Description

The LatticeMico8 to WISHBONE adapter uses the upper address lines to decode each individual slave device. The number of address lines used for this is configurable, with the number of decoded slaves equaling 2^N address lines used.

Based on this address decoding, the desired device is enabled. The logic used for the adapter is shown in Figure 1.

Figure 1. LatticeMico8 to WISHBONE Logic

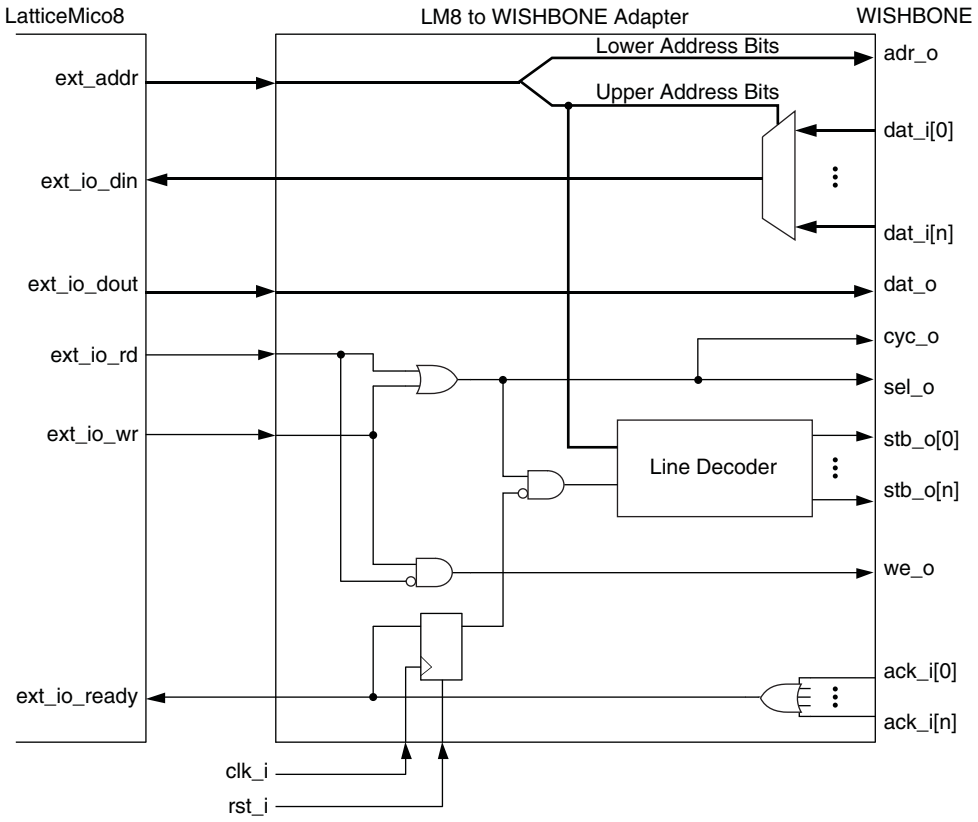


Table 1. Pin List

Pin	I/O	Description
WISHBONE Interface		
clk_i	I	Clock input - Common signal to LatticeMico8, WISHBONE Adapter, and WISHBONE slave devices.
rst_i	I	Reset input - Synchronous, active-high. Common signal to LatticeMico8, WISHBONE Adapter, and WISHBONE slave devices.
wb_ack_i[N]	I	WISHBONE acknowledge - Each WISHBONE slave asserts its ack_o when a cycle has terminated normally.
wb_dat_i[N*8]	I	WISHBONE data in - Combined (concatenated) data from each WISHBONE slave data_o[7:0] output.
wb_stb_o[N]	O	WISHBONE strobe - A signal generated by the master unique to the slave device selected.
wb_we_o	O	WISHBONE write enable - A signal generated by the master to indicate write cycles.
wb_sel_o	O	WISHBONE select - Indicates which byte(s) will be used for the current cycle. For the 8-bit only LatticeMico8, this signal is one bit wide.
wb_cyc_o	O	WISHBONE cycle - Indicates that a cycle is in progress.
wb_dat_o[7:0]	O	WISHBONE data output - 8-bit data from master.
wb_adr_o[]	O	WISHBONE address - Address generated by the master after decoding the address from LatticeMico8.
LatticeMico8 Interface		
lm8_addr[]	I	LatticeMico8 address - Generated during read and write cycles.
lm8_ext_io_rd	I	LatticeMico8 I/O read - Indicates the current cycle is an external I/O read.
lm8_ext_io_wr	I	LatticeMico8 I/O write - Indicates the current cycle is an external I/O write.
lm8_ext_io_din[7:0]	O	LatticeMico8 data input - Data sent back to LatticeMico8 from the external I/O reads.
lm8_ext_io_dout[7:0]	I	LatticeMico8 data output - Data from LatticeMico8 on external I/O writes.
lm8_io_ready	I	LatticeMico8 ready - Held low by the external device until it has read or written the data.

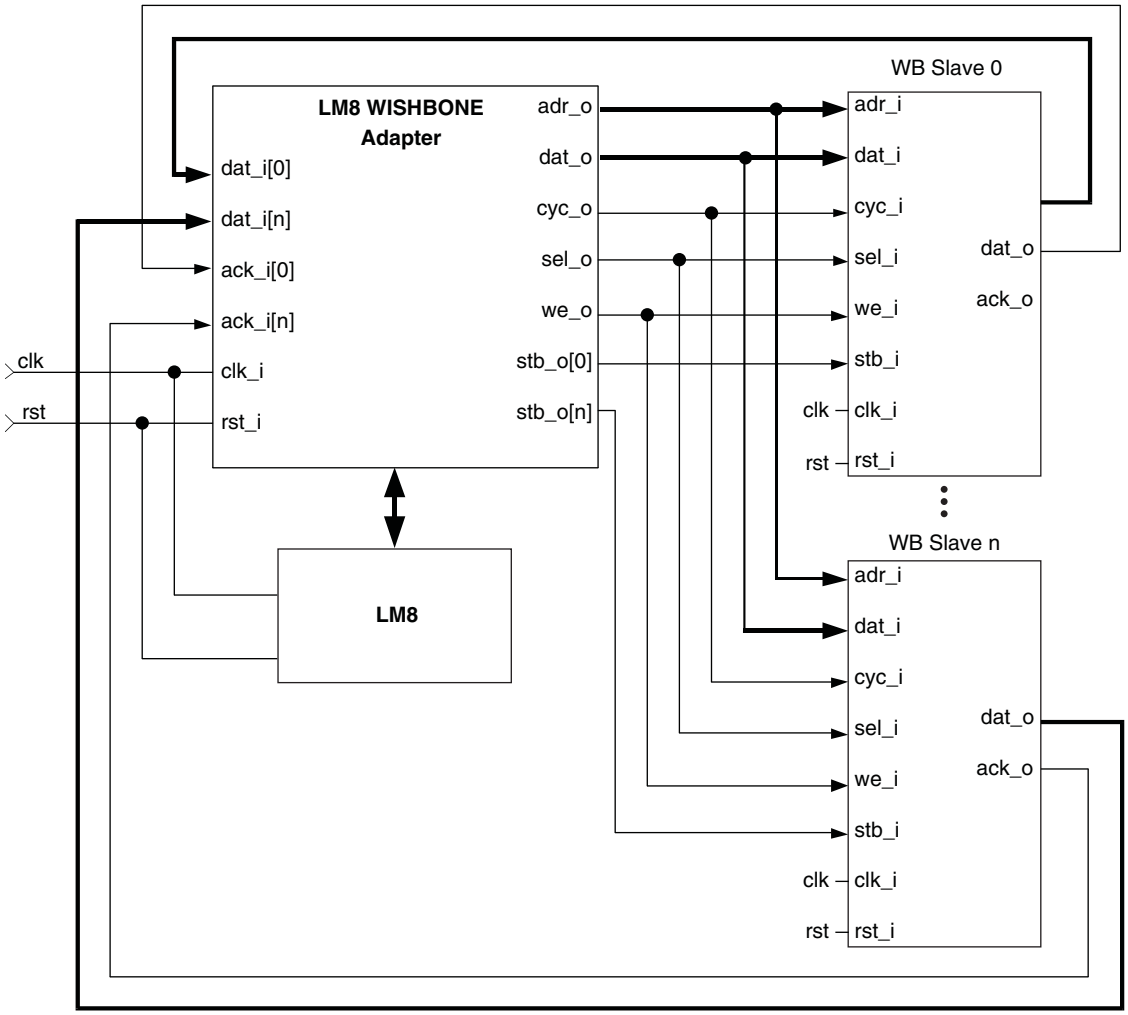
Since the LatticeMico8 supports only single transfers and is 8 bits wide, cyc_o and sel_o are logically identical. A cycle is in progress when the LatticeMico8 is reading or writing, and the active data lines are limited to [7:0].

The outputs to each slave device are all common, with the exception of stb_o. This output is unique to the device and is generated from the address decoding. A WISHBONE slave responds only when its stb_i input signal is asserted.

Each slave indicates normal termination of a cycle by asserting its ack_o output. This is driven back to the LatticeMico8 ext_io_ready input, inserting LatticeMico8 wait states and holding its I/O outputs constant until the slave device no longer requires their presence. The stb_o output from the LatticeMico8 WISHBONE Interface Adapter is de-asserted on the next clock cycle, as required by the WISHBONE specification.

Connections from the LatticeMico8 WISHBONE Interface Adapter to the slave devices are shown in Figure 2.

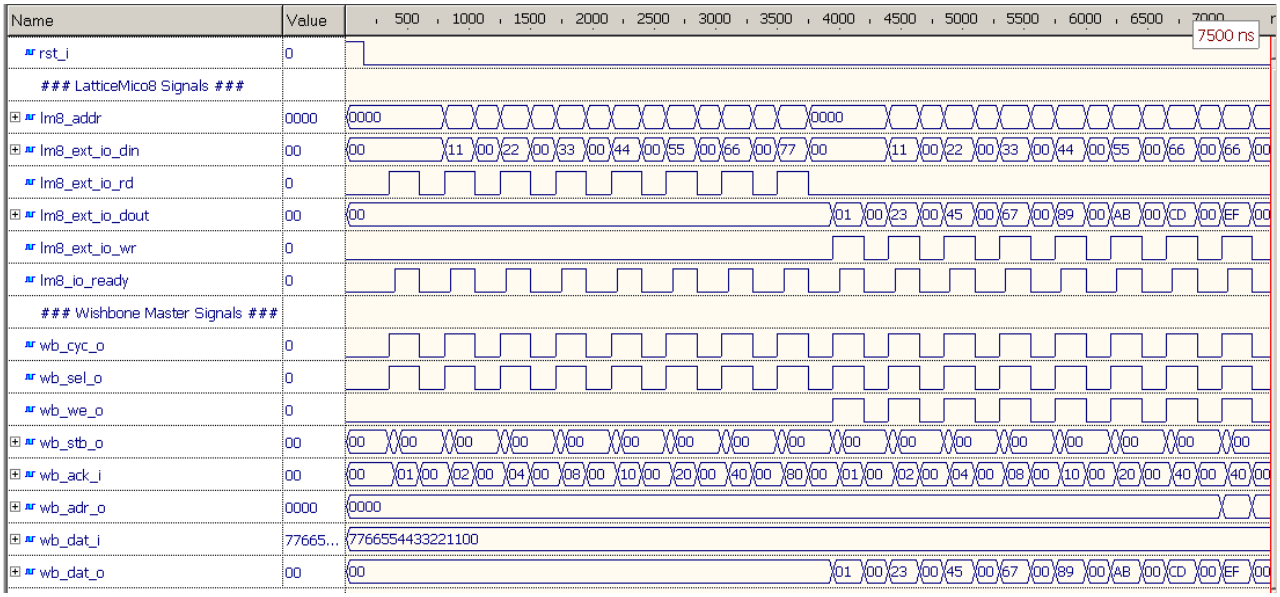
Figure 2. WISHBONE Interconnect



Note: clk and rst signals are common to LM8 and the WISHBONE adapter and slave devices.

Timing Specifications

Figure 3. LatticeMico8 Read and Write



Implementation

Table 2. Performance and Resource Utilization

Device Family	Language	Speed Grade	I/O[3]	f_{MAX} (MHz)	Utilization (LUTs)[4]	Architecture Resources
MachXO™ [1]	Verilog	-5	141	>300	58	N/A
	VHDL	-5	141	>300	58	N/A
LatticeXP2™ [2]	Verilog	-5	141	>300	58	N/A
	VHDL	-5	141	>300	58	N/A

1. Performance and utilization characteristics are generated using LCMXO1200C-5FT256C with Lattice ispLEVER 8.0 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
2. Performance and utilization characteristics are generated using LFXP2-5E-5QN208C with Lattice ispLEVER 8.0 software. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
3. Signals for this design typically interconnect other internal logic and do not impact external device I/O utilization.
4. Varies with configuration. Utilization shown uses three address bits to decode eight devices.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
February 2009	01.0	Initial release.
February 2010	01.1	Added support for the LatticeXP2 device family.
		Added VHDL support for all device families.