ispClock5400D

Integrates Zero-Delay and Fan-out Buffers with Dynamic Skew Adjustment through I²C

The ispClock™5406D and ispClock5410D are in-system-programmable differential clock distribution ICs designed for use in high-performance communications and computing applications such as PCI Express, ATCA, MicroTCA, and AMC. The ispClock5400D family features the CleanClock™ ultra-low phase noise, third-generation PLL. The FlexiClock™ output section supports multiple logic standards and dual skew control features.

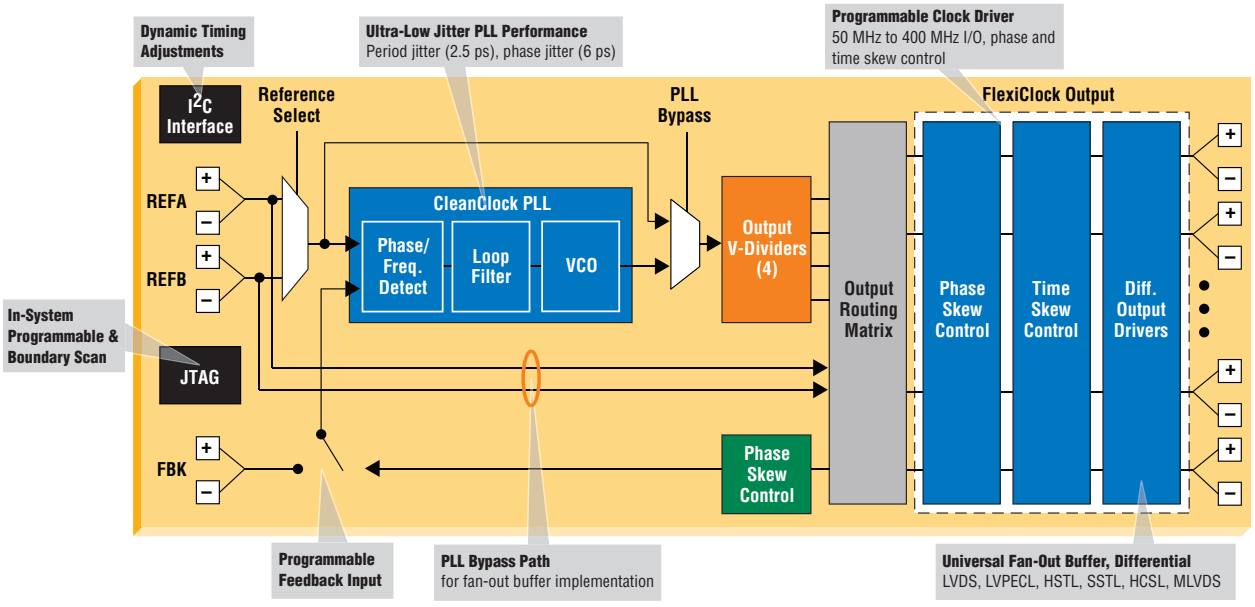
The configuration of each device is held in on-chip non-volatile memory that is reprogrammable through a JTAG interface. Certain aspects of the device can be modified on-the-fly via an I²C interface.

The ispClock5400D architecture is built around a high-performance ultra-low jitter PLL with programmable input, feedback, and output interface standards. Each output's time and phase skew can be individually and precisely controlled to compensate for differences in board trace lengths or timing requirements of the receiving devices. Additionally, each output can be individually configured for fan-out buffer (FOB) or zero-delay buffer (ZDB) operation.

Key Features and Benefits

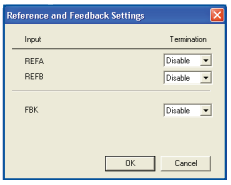
- **CleanClock PLL for High-Speed Protocol Support**
  - Period jitter 2.5 ps
  - Cycle-cycle jitter 29 ps (p-p)
  - Compatible with spread-spectrum clocks
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable termination
  - Clock A/B selection multiplexer
- **FlexiClock Output**
  - 50MHz to 400MHz
  - Programmable phase skew control per output
    - 16 settings; minimum step size 156 ps
    - Up to +/- 12 ns skew range
  - Programmable time skew control per output (in addition to phased skew)
    - 16 settings; step size 18 ps
  - Dynamic phase and time skew adjustment through I2C
  - Low output-to-output skew (<100 ps)
  - 6 or 10 programmable fan-out buffers
    - Programmable differential output standards and individual enable controls (LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS)
    - Up to 10 banks with individual VCCO and GND (1.5V, 1.8V, 2.5V, 3.3V)
- **All Inputs and Outputs are Hot-Socket Compliant**
- **Programmable as Fan-Out Buffer (FOB) or Zero-Delay Buffer (ZDB) from a Reference Clock**
  - Single chip replaces a variety of ZDB and FOB ICs
  - Single chip for high-performance differential clock distribution needs
  - Ultra-low jitter
- **Full JTAG Boundary Scan Test In-System Programming Support**
  - Increases test coverage and reduces manufacturing time
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges**
- **48-Pin and 64-Pin QFNS Packages**

ispClock5400D Block Diagram

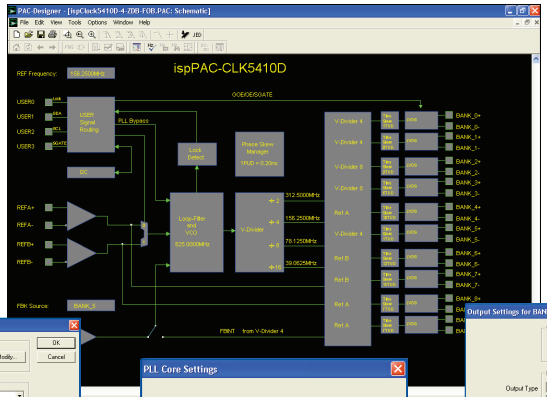


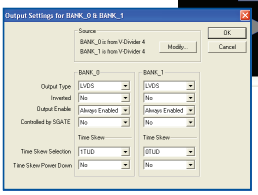
Design Made Simple with PAC-Designer Software

Lattice's PAC-Designer® software, a PC-based software tool, provides simple and intuitive pull-down menus for configuring all programmable features of the device. In addition, design utilities like the Skew Editor, Frequency Calculator and Frequency Synthesizer enable easy configuration of various counters and other options. Configurations can be downloaded into ispClock devices from a PC parallel port.

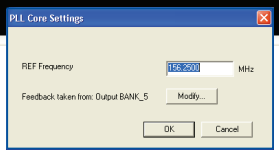


1. Set Reference and Feedback Clock Interface.

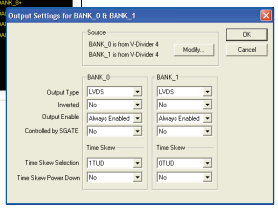




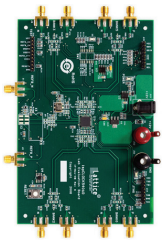
2. Set Output Clock Properties.



3. Set Input and Output Clock Frequencies.



4. Set Individual Clock Output Skews.



5. Download and Verify Design with Evaluation Board.

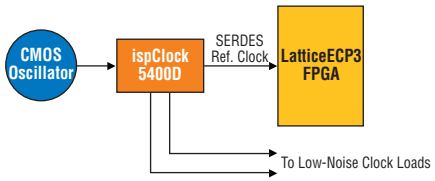
ispClock5400D Attributes

Feature	ispClock5400D Device	
	5406D	5410D
Outputs	6	10
I/O Frequency Range	50 to 400 MHz	
VCO Operation	400 to 800 MHz	
Spread Spectrum Compatibility	Yes	
Programmable I/O and Feedback Interface Types	LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS	
PLL Feedback	External/Internal	
Number of V-Dividers	4	
V-Divider Count Range	2 to 16 (power of 2)	
Maximum Cycle-Cycle Jitter	29 ps (p-p)	
Maximum Period Jitter (RMS)	2.5 ps	
Typical Phase Jitter (RMS)	6 ps	
Maximum Static Phase Offset	0 ps to 100 ps	
Programmable Phase Skew	156 ps to 12 ns	
Packaging	48 QFNS	64 QFNS

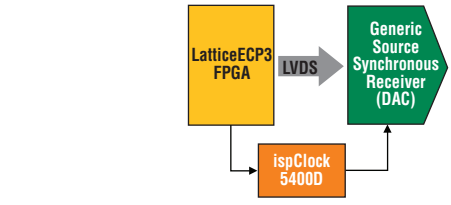
Application Diagrams

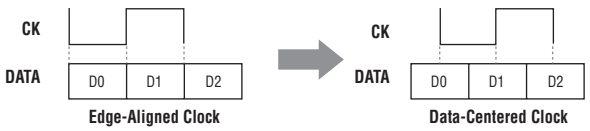
The ispClock5400D PLD can be used as a standard differential clock distribution IC across all designs.

- **High-Performance SERDES Reference Clock for LatticeECP3™ FPGA Using Low-Cost CMOS Oscillator**
  - Eliminates expensive differential crystal oscillators



- **Clock Management for High-Speed Source Synchronous Interfaces**
  - Converts edge-aligned clock output from FPGA to data-centered clock (90° phase skew) for receiver
  - Use Time Skew feature to dynamically adapt to PVT variation of setup and hold times





Applications Support
1-800-LATTICE (528-8423)
503-268-8001
techsupport@latticesemi.com

November 2012
Order #: I0200A