Lattice ECP3 Hardware Checklist

Technical Note

FPGA-TN-02183-2.4

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
BGA	Ball Grid Array
CML	Current Mode Logic
CSN	Chip Select Negative
CSSPI	Chip Select SPI
CSSPIN	Chip Select SPI Negative
DC	Direct Current
DDR	Double Data Rate
DI	Data In
DLL	Delay-Locked Loop
DM	Data Mask
DNI	Do Not Install
DOUT	Data Out
DQ	Data Queue
DQS	Data Strobe
ESR	Equivalent Series Resistance
FPGA	Field Programmable Gate Array
GPLL	General Purpose PLL
HCSL	High-Speed Current Steering Logic
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
IOLOGIC	I/O Logic Block
JTAG	Joint Test Action Group
LDQS	Lower Data Strobe
LUT	Look-Up Table
LVDS	Low-Voltage Differential Signaling
MCLK	Master Clock
MPCM	Multiplexed Parallel Configuration Mode
ODT	On-Die Termination
OEN	Output Enable Negative
PCKLTx_y	Clock Input Pin
PCLK	Phase Clock
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
SCM	Serial Configuration Mode
SERDES	Serializer/Deserializer
SSTL	Stub Series Terminated Logic
TAP	Test Access Port
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
XRES	External Reset

1. Introduction

When designing complex hardware using the LatticeECP3™ FPGA, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the LatticeECP3 device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that the reader is familiar with the LatticeECP3 device features as described in the LatticeECP3 Family Data Sheet (FPGA-DS-02074). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Please refer to the LatticeECP3 Family Data Sheet for the device-specific details.

- LatticeECP3 Family Data Sheet (FPGA-DS-02074)

The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the LatticeECP3 power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Users should refer to the following documents for detailed recommendations.

- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- LatticeECP3 sysIO Usage Guide (FPGA-TN-02194)
- LatticeECP3 sysCONFIG™ Usage Guide (FPGA-TN-02192)
- LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC SERDES Jitter (TN1084)
- LatticeECP3 SERDES Characterization Report (TN1195)(available under NDA, contact your local Lattice sales representative)
- HSPICE SERDES CML simulation package and die models in RLGC format (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- LatticeECP3-related pinout information can be found on the Lattice web site.

2. Power Supplies

All supplies including V_{CC}, V_{CCAUX} and V_{CCIO8} power supplies determine the LatticeECP3 internal *Power Good* condition. These supplies need to be at a valid and stable level before the device can become operational. Several other supplies including V_{CCPLL}, V_{CCIB}, and V_{CCOB} are used in conjunction with on-board SERDES and phase-locked loops. Table 2.1. shows the power supplies and the appropriate voltage levels for each supply.

Table 2.1. LatticeECP3 FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.2 V	FPGA core power supply.
V_{CCA}	1.2 V	Power supply analog SERDES blocks. It should be isolated and *clean* from excessive noise.
$V_{CCPLL[L:R]}$	3.3 V	Power supply for PLL. It should be isolated and *clean* from excessive noise.
V_{CCAUX}	3.3 V	Auxiliary power supply.
$V_{CCIO[0-3]}$* & $V_{CCIO[6-8]}$*	1.2 V to 3.3 V	I/O power supply. Seven general-purpose I/O banks and each bank has its own supply V_{CCIO0} to V_{CCIO3} and V_{CCIO6} to V_{CCIO8}.
		V_{CCIO8} is used in conjunction with the pins dedicated and shared with device configuration.
		V_{CCIO0} to V_{CCIO3} and V_{CCIO6} to V_{CCIO8} are optionally used based on, per bank usage of I/O.
V_{CCJ}	1.2 V to 3.3 V	JTAG power supply for the TAP controller port.
V_{CCIB}	1.2 V to 1.5 V	CML input termination voltage.
V_{CCOB}	1.2 V to 1.5 V	CML output termination voltage.

Note: *Banks 4 and 5 do not exist on the LatticeECP3. Therefore, V_{CCIO4} and V_{CCIO5} are not available.

The LatticeECP3 FPGA device has a power-up reset state machine that depends on various power supplies.

These supplies should come up monotonically. A power-up reset counter will begin to count after all of the approximate conditions are met:

- V_{CC} reaches 0.8 V or above
- V_{CCAUX} reaches 2.7 V or above
- $V_{CCIO[8]}$ reaches 0.8 V or above

Initialization of the device will not proceed until the last power supply has reached its minimum operating voltage.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage
- Expected voltage drops due to power filtering the ferrite bead's ESR x expected current draw
- Expected voltage drops due to the current measuring resistor's ESR x expected current draw

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.2 V rail is especially sensitive to noise, as every 12 mV is 1% of the rail voltage. For SERDES differential power rails, it is recommended to target a maximum 1% peak noise. For PLLs, target less than 0.25% peak noise.

3. LatticeECP3 SERDES/PCS Power Supplies

There are supplies dedicated to the operation of the ECP3 device, SERDES Blocks. These supplies are also paired with dedicated ground pins. Providing a quiet supply is critical for these blocks. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with short traces to keep inductance low.

For the best jitter performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading cause of PCB-related crosstalk to sensitive blocks is related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	10 µF x 3 + 100 nF per pin	FPGA core power supply. 1.2 V
V_{CCA}	120 Ω FB + 10 µF + 100 nF per pin	Power supplies analog SERDES blocks. Should be isolated and *clean* from excessive noise. 1.2 V
$V_{CCPLL[L:R]}$	120 Ω FB + 10 µF + 100 nF per pin	Power supply for the PLL. Should be isolated and *clean* from excessive noise. 3.3 V
V_{CCAUX}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply 3.3 V
$V_{CCIO[0-3]}$ & $V_{CCIO[6-8]}$	10 µF + 100 nF per pin	Bank I/O. Unused banks can replace the 10 µF with a 1.0 µF. For banks with lots of outputs or large capacitive loading, replace the 10 µF with a 22 µF (or add one additional 10 µF).
V_{CCJ}	10 µF + 100 nF per pin	JTAG power supply for the TAP controller port. 1.2 V to 3.3 V
V_{CCIB}	120 Ω FB + 10 µF + 100 nF per pin	CML input termination voltage 1.2 V to 1.5 V
V_{CCOB}	120 Ω FB + 10 µF + 100 nF per pin	CML output termination voltage 1.2 V to 1.5 V

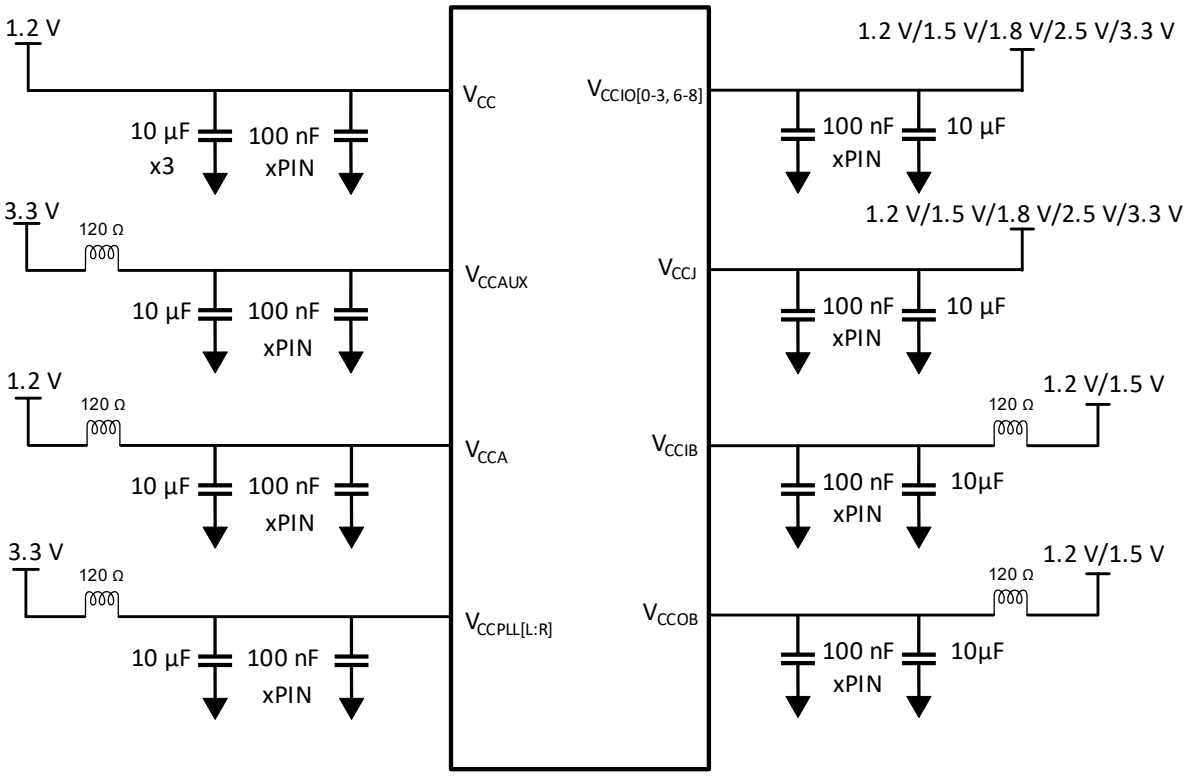

Figure 3.1 Recommended Power Filters

3.2. Ferrite Bead Selection Notes

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead-induced noise voltage from ESR × CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with an ESR between 0.025 Ω and 0.10 Ω depending on the current load.
- PLL rails are low-current which allows ferrite beads with an ESR ≤ 0.3 Ω.
- Small package-size ferrite beads have a higher ESR than large package-size ferrite beads of the same impedance.
- High-impedance ferrite beads have a higher ESR than low-impedance ferrite beads in the same package size.

3.3. Ground Pins

All ground pins need to be connected to the board's ground plane.

3.4. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, a single-ended or differential clock oscillator (for example), proper power supply isolation and decoupling of the clock oscillator are recommended.

When specifying components, choose good-quality ceramic capacitors in small packages and place them as close to the clock oscillator supply pins as possible. Good-quality capacitors for bypassing generally meet the following requirements.

3.5. Capacitor Selection

When specifying components, choose good-quality ceramic capacitors in small packages and place them as close to the power supply pins as possible. Good-quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.5.1. Dielectric

Use dielectrics such as X5R, X7R, and similar that have good capacitance tolerance (≤ ±20%) over a temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

3.5.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with a higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the voltage rail (maximum). For example, 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.5.3. Size

Smaller-body capacitors have lower inductance, work at higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size-related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0603
4.7 µF	0603	0402
10 µF	0603	0805
22 µF	0805	1206

3.6. Unused Bank V_{CCIOx}

Connect unused V_{CCIO} pins to a power rail; do not leave them open.

3.7. Unused SERDES

- Connect V_{CCA} pins to a power rail.
- Connect the REFCLK differential pair and Rx differential pair inputs to the system ground.
- Leave V_{CCIB}, V_{CCOB}, and Tx differential pair outputs open.

4. Power Sequencing

V_{CCIO} supplies should be powered up before or together with the V_{CC} and V_{CCAUX} supplies.

5. Power Estimation

Once the LatticeECP3 device density, package, and logic implementation are decided, power estimation for the system environment should be determined based on the software Power Calculator provided as part of the ispLEVER®design tool. When estimating power, the designer should keep two goals in mind:

1. Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current, or maximum DC and AC current for the given system's environmental conditions.
2. The ability for the system environment and LatticeECP3 device packaging to be able to support the specified maximum operating junction temperature. By determining these two criteria, LatticeECP3 power requirements are taken into consideration early in the design phase.

6. Configuration Considerations

The LatticeECP3 includes provisions to program the FPGA via a JTAG interface or through several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations:

Table 6.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI	4.7 kΩ Pull-up to V_{CCJ}
TMS	4.7 kΩ Pull-up to V_{CCJ}
TDO	4.7 kΩ Pull-up to V_{CCJ}
TCK	4.7 kΩ Pull-down

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO8} and ground.

Using JTAG for configuration, the MODE pins are not used. Using other programming modes requires the use of the CFG[2:0] input pins. The CFG [2:0] pins include internal weak internal pull-ups. It is recommended that 1–10 kΩ external resistors be used when using these sysCONFIG modes. Pull-up resistors should be connected to V_{CCIO8}.

External resistors are always needed if the configuration signals are being used to handshake with other devices. Recommended 4.7 kΩ pull-up resistors to V_{CCIO8} and pull-down to board ground should be used on the following pins:

Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO8}
INITN	4.7 kΩ pull-up to V_{CCIO8}
MCLK/CCLK	1 kΩ pull-up to V_{CCIO8}
CSSPIN	4.7 kΩ to 10 kΩ pull-up to V_{CCIO8}
CFG[2:0]	1 kΩ to 10 kΩ pull-up to V_{CCIO8}, 0 = GND. See Table 6.3
XRES	10 kΩ pull-down

Table 6.3. Configuration Pins Needed per Programming Mode[1]

Configuration Mode	Bus Size	Dedicated CFG[0:2]	sysCONFIG Pin Mapping + Dedicated Pins			Dedicated Pins
			Clock Pin	I/O	Shared Pins	
SPI Controller (Fast/Slow)	1 bit	000	MCLK	O	SPID0, CSSPIN, SPISI, DOUT, D0, CONT1N, CONT2N	PROGRAMN, INITN, DONE
		010	MCLK	O	SPID[0,1], CSSPI[0,1]N, SPISI, D0, CONT1N, CONT2N	
Burst Flash	16 bits	001	MCLK	O	D[0:7], XD[8:15], AVDN, OEN, RDY	PROGRAMN, INITN, DONE
MPCM	8 bits	011	MCLK	O	D[0:7], CSN, CS1N, WRITEN, BUSY	PROGRAMN, INITN, DONE
Target SPI	1 bit	100	CCLK	I	SO, SN, SI, DOUT,HOLDN	PROGRAMN, INITN, DONE
SCM	1 bit	101	CCLK	I	DI and DOUT	PROGRAMN, INITN, DONE
Parallel	8 bits	111	CCLK	I	D[0:7], CSN, CS1N, WRITEN, BUSY	PROGRAMN, INITN, DONE
JTAG	1 bit	XXX	TCK	I	NA	TCK, TMS, TDI, TDO

Note:

1. Leave the unused configuration ports open.

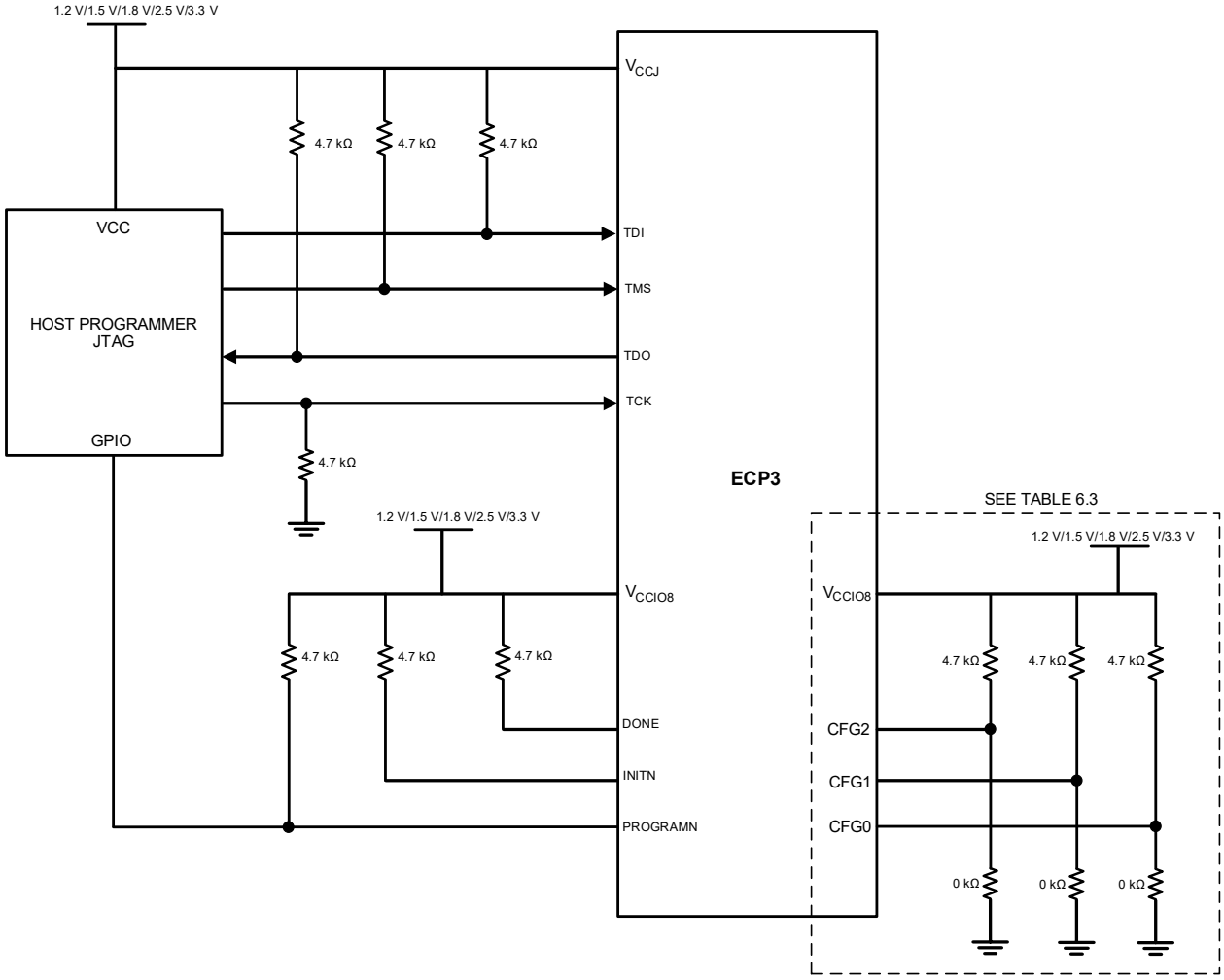

Figure 6.1. Typical Connections for Programming SRAM via JTAG

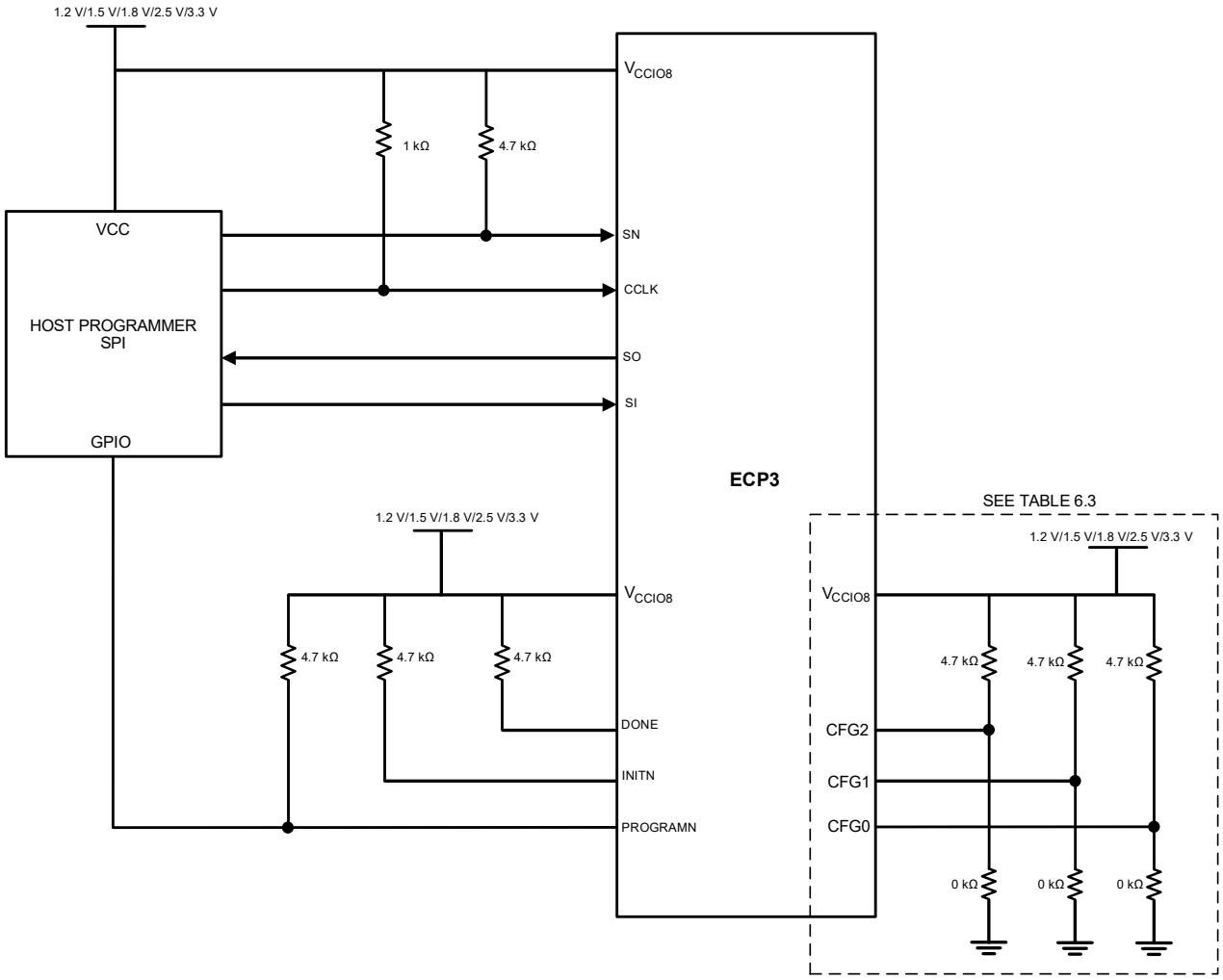

Figure 6.2. Typical Connections for Programming SRAM via SSPI

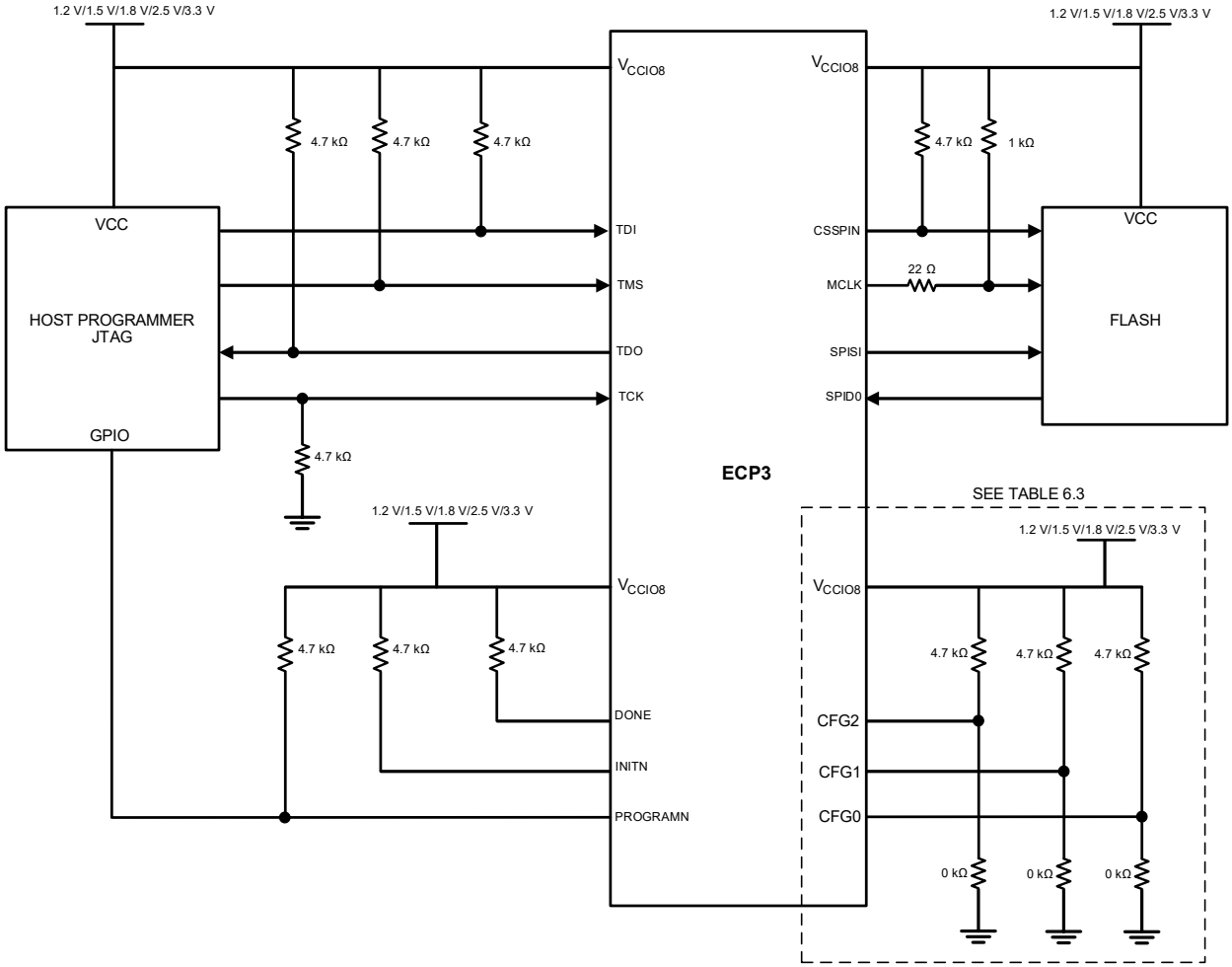

Figure 6.3. Typical Connections for Programming external Flash via JTAG

7. External SPI FLASH

The flash voltage should match the V_{CCIO8} voltage.

It is recommended to use an SPI flash device that is supported in Diamond Programmer. To see the supported list of devices, go to Diamond Programmer, under the *Help* menu, choose **Help**, then search for **SPI Flash Support**.

For SPI Flash devices that are not listed in the **SPI Flash Support**, using the custom flash option may allow a non-supported device to work.

8. I/O Pin Assignments

The V_{CCA} provides a *quiet* supply for the internal PLLs and critical SERDES blocks. For the best jitter performance, careful pin assignment will keep *noisy* I/O pins away from *sensitive* pins. The leading causes of PCB-related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the V_{CCA}; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

Although coupling has been reduced in the device packages of the LatticeECP3 devices where little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins, as well as other critical I/O pins such as clock signals. Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they will cause problems.

It is common practice for designers to select pinouts for their system early in the design cycle. For the FPGA designer, this requires detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/Os. Lattice provides detailed pinout information that can be downloaded from the Lattice website in **.csv** format for designers to use as a resource to create pinout information. For example, by navigating to the ECP3 web page, the user can gather the pinout details for all the different package offerings of the ECP3-17 device family, including I/O banking, differential pairing, and input and output details.

9. sysI/O

The LatticeECP3 provides the flexibility to configure each I/O according to user requirements. These pins can be configured as input, output, and tri-state. Additionally, attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can also be set up.

For the PULLMODE, Pull-up and Pull-down resistors can be set. The implementation of this resistor is by using a constant current that has the following values:

Table 9.1. Weak pull up/down current specifications

	Parameter	Condition	Min	Max	Unit
Pull-up	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	–30	–210	µA
Pull-down	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	210	µA

10. Clock Inputs

The LatticeECP3 devices provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for general purpose I/O.

However, when these pins are used for clocking purposes, noise needs to be minimized on these pins. Refer to the LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184).

These shared clock input pins, typically labeled as GPLL and PCLK, can be found under the Dual Function column of the pinout csv file located on the Lattice website and in the pin assignment tab of Diamond software's Spreadsheet View. High-speed differential interfaces (such as MIPI) being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

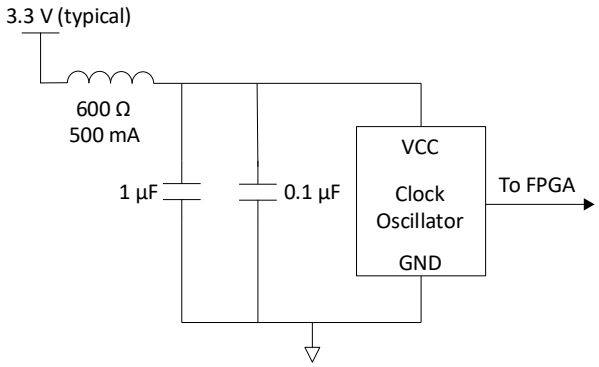

Figure 10.1. Clock Oscillator Bypassing

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS is shown below in Figure 10.2.

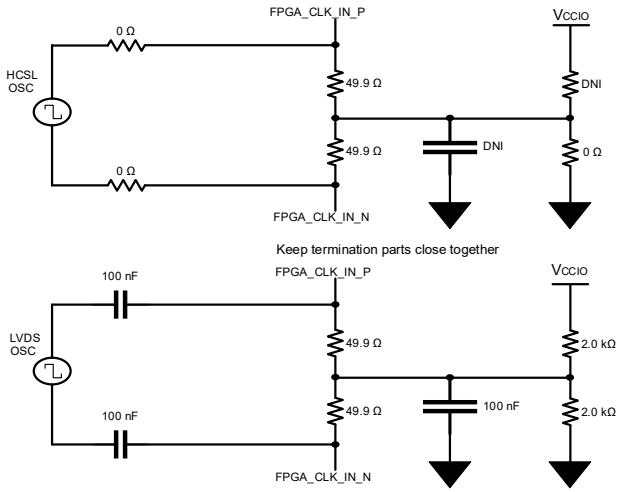

Figure 10.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

11. Dedicated FPGA Inputs (Non-Configuration)

Pins annotated E_A/B/C/D (example: PR43E_A, PR43E_B, etc.) are dedicated input pins. The primary purpose of these pins is to provide a dedicated input to the FPGA PLLs. They are also available for use as general inputs into the FPGA fabric when not used with a PLL. However, they are available as inputs only. These pins cannot be output or bidirectional.

12. Pinout Considerations

The LatticeECP3 supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to the implementation of the PCB design. The pinout selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to the LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184) for rules pertaining to these interface types.

13. LVDS Pin Assignments

True-LVDS outputs are available on I/O pins on the left and right sides of the device. LVDS output differential drivers are not supported in banks at the top and bottom. Emulated LVDS outputs are available on any A and B pair around the device, but this will require external termination resistors. This is described in the LatticeECP3 sysIO Usage Guide (FPGA-TN-02194).

LVDS inputs are available on any A and B pair of all I/O cells around the entire device. The LatticeECP3 device includes differential input terminations with a common mode connection to the bank V_{TT} pin, which must be left floating.

14. HSTL and SSTL Pin Assignments

These externally referenced I/O standards require an external reference voltage. The V_{REF} pin(s) should get high priority when assigning pins to the PCB. Each bank includes a separate V_{REF} voltage. V_{REF1} sets the threshold for the referenced input buffers. In the LatticeECP3 devices, any I/O pin in a bank can also be configured to be a dedicated reference voltage supply pin. However, the predefined V_{REF} pins provide the best case. Each I/O is individually configurable based on the bank's supply and reference voltages.

In addition, there are dedicated terminating supply (VTT) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are located in banks 2, 3, 7, and 6 and may not be available in some packages. Unused V_{TT} pins should be left disconnected.

A calibration resistor is used to compensate for output drivers. A 10Kohm ±1% resistor connected between the XRES pin and PCB ground is needed.

15. XRES Pin

The XRES pin provides a reference to the internal band gap circuit used by PLLs through a PCB-connected resistor (10 kΩ ±1%). This resistor is also essential for device configuration, which cannot be completed if it is missing. To ensure a stable current source, the XRES pin must be routed carefully. The PCB should maintain a short connection to the XRES resistor, which must be connected directly to the PCB ground plane.

This XRES pin can also be protected by careful pin selection of adjacent signals in the design. Any *switching or noisy* signals on adjacent pins can increase the PLL output jitter due to cross-coupling noise from the aggressor pin to the XRES pin.

It is strongly recommended to tie aggressor pins to the PCB ground. If the user has to assign a function due to pin constraints, it is recommended that the pin be a static or low-frequency control signal as opposed to a high-speed data signal. These aggressor pins are defined in Table 15.1.

Table 15.1. XRES Aggressor Pin Listing

Package	XRES Aggressor Pins
1156-ball BGA	AN29, AM31

16. SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly matched differential routing with very few discontinuities. Please refer to the High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance.

When operating at 2.5 Gbps or above, use of the following FPGA I/O pins can cause increased jitter. Extra care must be given to these pins when used in combination with the high-speed SERDES interface. High-speed switching output assignments should be minimized or avoided on these pins when the SERDES interface is in use. Only static output or input configurations are recommended.

If using the PCSC quad on the 1156 package (for either LatticeECP3-70, LatticeECP3-95, or LatticeECP3-150), the following pins are affected: AE26, AF26, AG26, AH26, AH27, AJ27, AK27, AL27, AM27, AN27, AP27, AH28, AJ28, AK28, AL28, AM28, AN28, AP28, AK29, AL29, AM29, AN29, AP29.

If using the PSCD quad on the 1156 package (for LatticeECP3-150), the following pins are affected: AE9, AF9, AG9, AH9, AJ8, AK8, AL8, AM8, AN8, AP8, AH7, AJ7, AK7, AL7, AM7, AN7, AP7, AJ6, AK6, AL6, AM6, AN6, AP6.

The above-mentioned aggressor pin list can only impact SERDES quads PCSC and PCSD. Quads PCSA and PCSB have no suggested aggressor pins due to the physical layout of the device.

There are no known aggressor I/O pins for any other LatticeECP3 device or package combinations other than the beforementioned devices.

17. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes; this is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

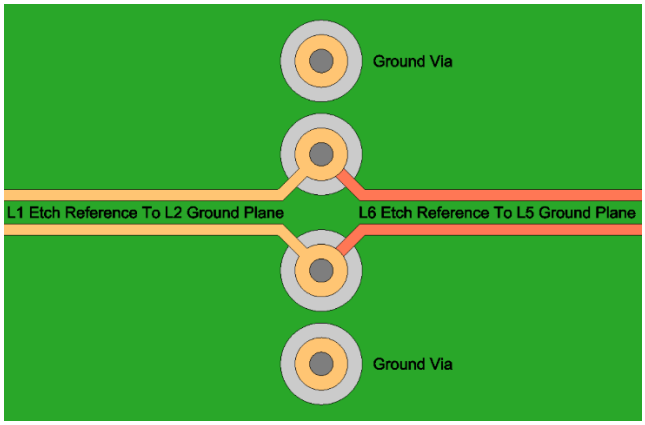

Figure 17.1. Ground Vias Implementation

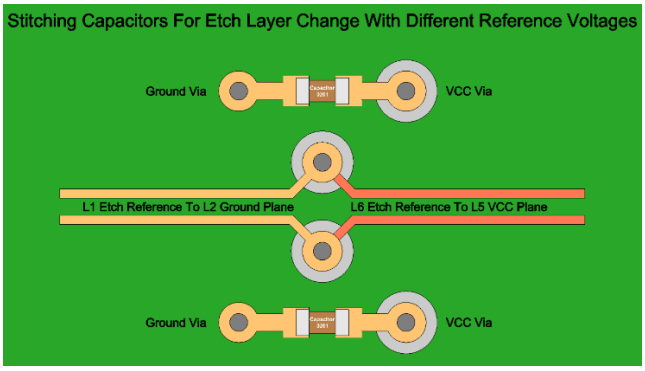

Figure 17.2. Stitching Vias Implementation

6. High-speed signals have a corresponding impedance requirement; calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

18. Simulation and Board Measurement of Critical Signals

To ensure a design is reliable and will have high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

18.1. Critical Signals

Signals sensitive to Signal Integrity (SI) degradation are considered critical signal which require extra design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, etc.)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

18.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often have reoccurring subscription pricing. The expensive tools can import board design files and can easily supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (ex. Micro-cap) can supply useful basic simulations, but take extra effort to set up SI effects for multiple signals with different transmission line lengths, lossy transmission lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

18.3. Board Measurements

Critical signals should be measured on the actual PCB assembly using an Oscilloscope. Verify proper signaling function and signal integrity (that is, eye diagram or SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (ex. output series termination resistor value).
- Adjust setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI)

19. Checklist

Table 19.1 Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	V_{CC} core at 1.2 V ±5%.		
1.1.1	Use a PCB plane for V_{CC} core with proper decoupling.		
1.1.2	V_{CC} core sized to meet power requirement calculation from software.		
1.2	V_{CCA} at 1.2 V ±5%.		
1.2.1	V_{CCA} *quiet* and *isolated.*		
1.2.2	V_{CCA} pins should be ganged together, and a solid PCB plane is recommended. This plane should not have adjacent non-SERDES signals passing above or below. It should also be isolated from the V_{CC} core power plane.		
1.3	All $V_{CCIO[1-8]}$ 1.2 V to 3.3 V.		
1.3.1	V_{CCIO8} is used with configuration interfaces (that is, memory devices). Need to match specifications.		
1.3.2	$V_{CCIO[1:7]}$ used based on user design.		
1.4	V_{CCAUX} at 3.3 V ±5%.		
1.4.1	V_{CCPLL} at 3.3 V ±5%.		
1.4.2	V_{CCPLL} *quiet* and *isolated* at 3.3 V ±5%.		
1.5	V_{CCJ} 1.2 V to 3.3 V.		
1.6	Power estimation		
1.7	10 kΩ ±1% pull-down on XRES pin.		
1.7.1	XRES pin uses short connection to resistor. Resistor connected directly to PCB ground plane.		
1.7.2	Follow XRES aggressor pin recommendation.		
2	**SERDES Power Supplies**		
2.3	V_{CCIB} and V_{CCOB} connected for USED SERDES channels.		
2.3.1	V_{CCIB} and V_{CCOB} 1.2 V-1.5 V nominal ±5%.		
3	**Configuration**		
3.1	Pull-ups and pull-downs on configuration specific pins.		
3.2	V_{CCIO8} bank voltage matches sysCONFIG peripheral devices such as SPI Flash.		
3.3	Pull-up or pull-down on SPIFASTN pin.		
4	**SERDES**		
4.1	Dedicated reference clock input from clock source meets the DC and AC requirements.		
4.1.1	External AC coupling caps may be required for compatibility to common-mode levels.		
4.1.2	Ref clock termination resistors may be needed for compatible signaling levels.		
4.2	Maintain good high-speed transmission line routing.		
4.2.1	Continuous ground reference plane to serial channels.		
4.2.2	Tightly length matched differential traces.		
4.2.3	Do not pass other signals on the PCB above or below the high-speed SERDES without isolation.		
4.2.4	Keep non-SERDES signal traces from passing above or below the 1.2 V V_{CCA} power plane without isolation.		
4.2.5	Avoid the aggressor pins mentioned previously in this document.		
5	**Special Pin Assignments**		
5.2	V_{REF} assignments followed for single-ended HSTL or SSTL inputs.		
5.2.1	Properly decouple the V_{REF} source.		
5.3	V_{TT} pins needed for on-die termination for HSTL or SSTL terminated I/O.		
5.3.1	All V_{TT} needs to be connected to termination power supply if used for V_{TT}. V_{TT} pins do not need to be connected if ODT (on-die termination) is not used in the design. V_{TT} pins can be left floating when not used for ODT.		

	Item	OK	NA
5.3.2	V_{TT} power connections (for SSTL or HSTL terminations) need to be a low-impedance PCB plane and properly decoupled.		
5.3.3	The bank V_{TT} pin must float when using differential input terminations.		
6	**Critical Pinout Selection**		
6.1	Pinout has been chosen to address FPGA resource connections to I/O logic and clock resources per LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184).		
6.2	Dedicated FPGA inputs are used only as inputs to the FPGA PLL or fabric. Not output or bidirectional.		
6.3	Use a PCLK pin for differential clock inputs to ensure clock signal is routed directly to the edge clock tree.		
6.4	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
7	**JTAG**		
7.1	Pulldown on TCK. See Table 6.1. JTAG Pin Recommendations.		
7.2	Pullups on TDI, TMS, TDO. See Table 6.1. JTAG Pin Recommendations.		
8	**External Flash**		
8.1	Flash voltage should match V_{CCIO8} voltage.		
9	**DDR3 Interface Requirements**		
9.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
9.2	Maintain a maximum of ±50 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
9.3	All data groups must reference a ground plane within the stack-up.		
9.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
9.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals.		
9.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
9.7	Differential pair of DQS to DQS_N trace lengths should be matched at ±10 mil.		
9.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
9.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
9.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
9.11	CK to CK_N trace lengths must be matched within 10 mil.		
9.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
9.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
9.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
9.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		
10	**Unused SERDES**		
10.1	See Unused SERDES section.		
11	**Layout Recommendations**		
11.1	Power should come from power planes to ensure good power delivery and thermal stability.		

	Item	OK	NA
11.2	Placement of analog circuits must be away from digital circuits or high switching components.		
11.3	High speed signals should target clearance of five times trace width from other signals.		
11.4	High speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are ground, else a stitching capacitor should be used.		
11.5	High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.		
12	**Simulation and Board Measurement of Critical Signals**		
12.1	Simulations: Use IBIS model to simulate critical signals for proper signal integrity.		
12.1.1	Simulate Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, etc.)		
12.1.2	Simulate Clock nets (Oscillator Inputs, Output Clocks).		
12.1.3	Simulate Data nets with embedded clocks.		
12.1.4	Simulate Interrupts (Edge Triggered).		
12.1.5	Simulate Logic signals travelling long distances requiring termination.		
12.1.6	Simulation results should be used to optimize each critical signal for best signal integrity: • Define output pin drive strength. • Define output pin slew rate. • Define output pin termination design (ex. output series termination resistor value). • Define setting of internal pin pull-up and pull-down resistors. • Improve PCB layout.		
12.2	Board Measurements: Use Oscilloscope to measure on PCB assembly critical signals for proper function and signal integrity.		
12.2.1	Measure Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, etc.)		
12.2.2	Measure Clock nets (Oscillator Inputs, Output Clocks).		
12.2.3	Measure Data nets with embedded clocks.		
12.2.4	Measure Interrupts (Edge Triggered).		
12.2.5	Measure Logic signals travelling long distances requiring termination.		
12.2.6	Measurement results should be used to optimize each critical signal for best signal integrity: • Adjust output pin drive strength. • Adjust output pin slew rate. • Adjust output pin termination design (ex. output series termination resistor value). • Adjust setting of internal pin pull-up and pull-down resistors.		
12.3	Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI)		

References

- LatticeECP3 Family Devices web page
- LatticeECP3 Family Data Sheet (FPGA-DS-02074)
- LatticeECP3 sysIO Usage Guide (FPGA-TN-02194)
- LatticeECP3 sysCONFIG™ Usage Guide (FPGA-TN-02192)
- LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC SERDES Jitter (TN1084)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Boards, Demos, IP Cores, and Reference Designs for LatticeECP3 Family Devices web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.4, October 2025

Section	Change Summary
All	Minor editorial fixes.
Abbreviations in This Document	Updated section contents.
Introduction	• Added, *Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists*, after the first paragraph of this section. • Removed the statement, *The device family consists of FPGA LUT densities ranging from 17K to150K.*
Configuration Considerations	Added XRES to Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins.
Clock Inputs	Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*.
XRES Pin	Rephrased the first paragraph to, *The XRES pin provides a reference to the internal band gap circuit used by PLLs through a PCB-connected resistor (10 kΩ ±1%). This resistor is also essential for device configuration, which cannot be completed if it is missing. To ensure a stable current source, the XRES pin must be routed carefully. The PCB should maintain a short connection to the XRES resistor, which must be connected directly to the PCB ground plane*.
Layout Recommendations	Replaced Figure 17.1. PCB Layout Recommendation with Figure 17.1. Ground Vias Implementation and Figure 17.2. Stitching Vias Implementation.
Checklist	• Added item 6.3, *Use a PCLK pin for differential clock inputs to ensure clock signal is routed directly to the edge clock tree.* • Added item 6.4, *For single-ended I/Os, use only PCLKT pins as primary CLK pads.*

Revision 2.3, August 2024

Section	Change Summary
All	• Minor editorial fixes • Replaced the word *Master* with *Controller*. • Replaced the word *Slave* with *Target*.
Inclusive Language	Added this section.
Abbreviations in This Document	Changed *Acronyms* to *Abbreviations* in This Document.
Power Supplies	Added Power Noise and Power Source subsection.
LatticeECP3 SERDES/PCS Power Supplies	Reworked section contents.
Power Sequencing	Added this section.
Configuration Considerations	Moved this section from Section 5 to Section 6 – Configuration Considerations and reworked section contents.
External SPI Flash	Added this section.
sysI/O	Added this section.
Clock Inputs	Added this section.
Layout Recommendations	Added this section.
Simulation and Board Measurement of Critical Signals	Added this section.
Checklist	Added this section.
References	Updated section contents.

Revision 2.2, March 2024

Section	Change Summary
All	• Changed document number from *TN1189* to *FPGA-TN-02183*. • Updated document template.
Disclaimers	Added this section.
Acronyms in This Document	Added this section.
References	Added this section.
Technical Support Assistance	Added the link to Lattice Answer Database.

Revision 2.1, February 2012

Section	Change Summary
Disclaimers	Updated document with new corporate logo.

Revision 2.0, July 2011

Section	Change Summary
XRES Pin	Added XRES pin information.

Revision 1.9, July 2011

Section	Change Summary
SERDES Pin Considerations	Added DDR3 Interface Requirements section to Hardware Checklist.

Revision 1.8, June 2011

Section	Change Summary
SERDES Pin Considerations	Added Pull-up or pull-down on SPIFASTN pin to Hardware Checklist.

Revision 1.7, December 2010

Section	Change Summary
SERDES Pin Considerations	Updated Hardware Checklist.

Revision 1.6, March 2010

Section	Change Summary
All	Updated reference documents list.

Revision 1.5, November 2009

Section	Change Summary
Introduction	Updated FPGA LUT densities in this section.
SERDES Pin Considerations	Updated this text section.

Revision 1.4, August 2009

Section	Change Summary
SERDES Pin Considerations	Updated this text section with information regarding pins that can cause increased jitter when operating at 2.5 Gpbs and above.

Revision 1.3, July 2009

Section	Change Summary
Power Supplies	LatticeECP3 FPGA Power Supplies table - Updated voltage values for VCCIB and VCCOB supplies.

Revision 1.2, July 2009

Section	Change Summary
SERDES Pin Considerations	• Added Dedicated FPGA Inputs (Non-configuration) and Pinout Considerations text sections. • Added Critical Pinout Selection section to Hardware Checklist table.

Revision 1.1, March 2009

Section	Change Summary
SERDES Pin Considerations	Updated Hardware Checklist table.

Revision 1.0, February 2009

Section	Change Summary
All	Initial release.

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