LatticeSC™ SFI-5 Evaluation Board

User's Guide

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Introduction

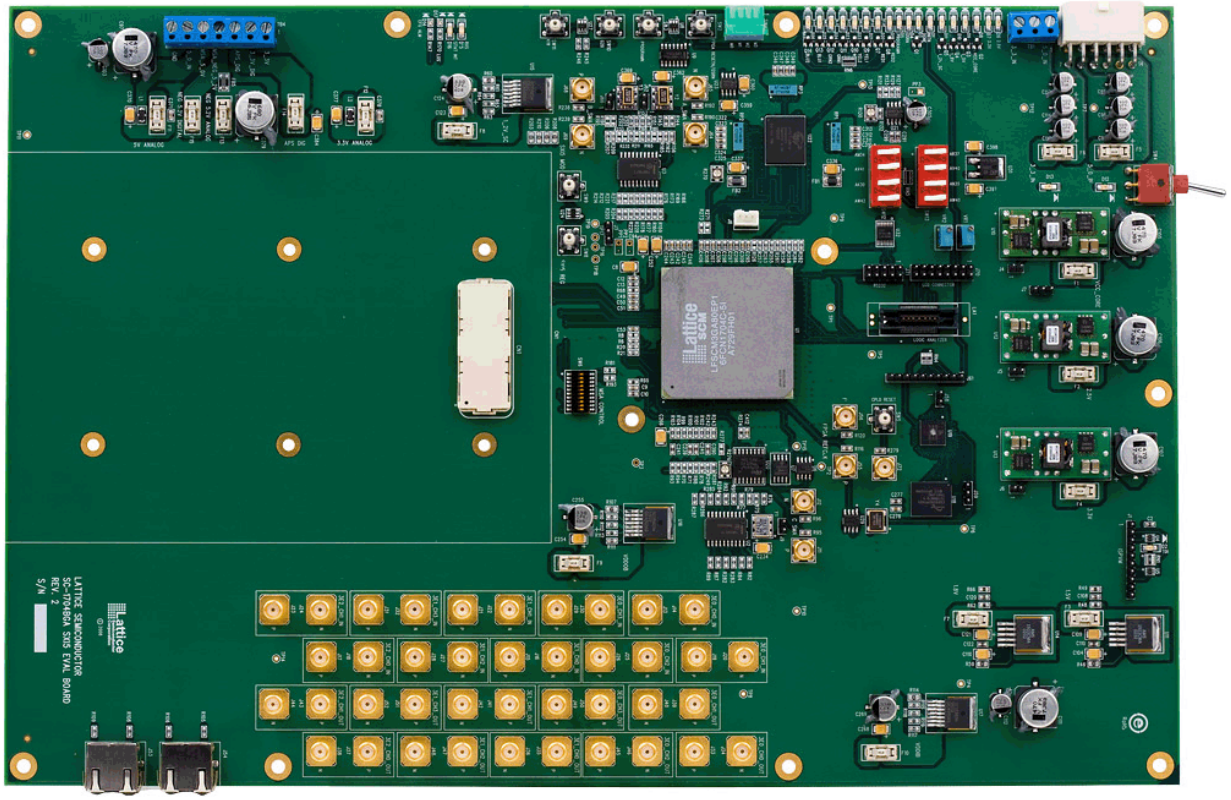
This user's guide describes the LatticeSC SFI5 Evaluation Board featuring the LatticeSC 1704-ball fcBGA FPGA device. The stand-alone evaluation board provides a functional platform for development and rapid prototyping of applications that incorporate high-performance SFI5 interfaces.

The Framer Interface Level 5 (SFI-5) standard supports interoperation with embedded transceivers, providing a 40-Gbps interface for high-performance optical communications applications. The SFI-5 specification is a chip-to-chip standard that ensures interoperability between forward-error correction (FEC) and the framer, as well as from industry-leading optical transponder devices. This evaluation board is used to verify compliance to the SFI-5 standard as it interoperates with the LatticeSC SERDES channels capable of operating at data rates between 600 Mbps and 3.125 Gbps.

The evaluation board includes provisioning to connect high-speed SERDES channels via SMA connectors to test and measurement equipment. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

The board has several debugging and analyzing features for complete evaluation of the LatticeSC device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeSC FPGA.

Figure 1. LatticeSC SFI-5 Evaluation Board



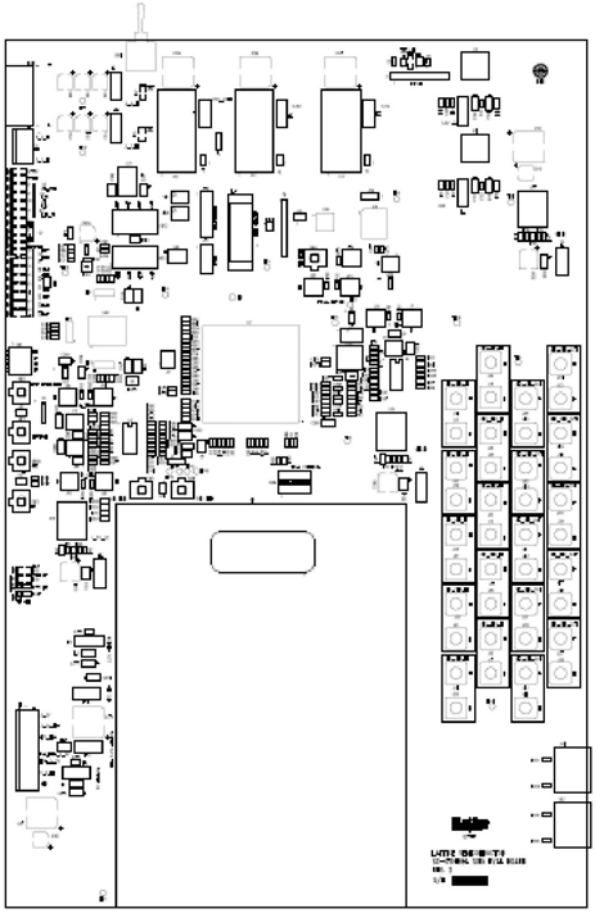
Board Features

- SERDES/FPGA framer SFI-5 interface.
- 40-Gigabit SFI-5 interface via a 300-pin MSA transponder interconnection
- SERDES high-speed interface SMA test points and clock connections

- SERDES connections to RJ-45 connection for physical layer testing to CAT5 cable standards
- 36-bit QDR2+ memory device
- Power connections and power sources
- ispVM® programming support
- On-board and external reference clock sources
- ORCAstra Demonstration Software interface via standard ispVM JTAG connection
- User-defined input and output points
- SMA connectors included for high-speed clock or data interfacing
- Performance monitoring via Agilent Logic Analyzer probe connection

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board.

Figure 2. LatticeSC SFI-5 Evaluation Board Outline Drawing, Top Side



LatticeSC Device

This board features a LatticeSC FPGA with a 1.2V core supply. It can accommodate all pin-compatible LatticeSC devices in the 1704-ball fcBGA (1mm pitch) package. A complete description of this device can be found in the LatticeSC Family Data Sheet on the Lattice website at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFE5S80 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeSC SFI-5 Evaluation Board is ready to power-on. The evaluation system is shipped with AC line cord for the included multi-voltage power supply. Follow these steps to power-on the board.

1. Connect the power supply unit to the board using the attached rainbow cable from power supply the power input connector on the board PWR1.
2. Confirm that the ON-OFF switch, SW4, is in the OFF position.
3. Plug the desktop power supply AC line cord into an electrical outlet supplying the appropriate voltage.
4. Turn on the switch on the desktop unit.
5. Turn SW4 to the ON position. The power indicators (described later in this document) for all regulator modules should illuminate, indicating output from the regulators.

Power Supplies

(See Appendix A, Figure 2-7)

The evaluation board incorporates many different schemes for providing power to the board. The board is equipped to accept a customized ATX supply via the PWR1 connection. This connection is provided to use with the switching supply provided with the kit using a Molex 87427-1203 connector.

This supply sources the intermediate power and is used for turnkey evaluations without the need to control and supply power from other sources. This supply provides intermediate 5.0V DC and 3.3V DC to the secondary power stages of the board. The intermediate supplies can also be sourced from adequately-sized bench-top supplies via banana jacks located near the PWR1 input connector.

The intermediate supplies are fused on-board with indicating fuses and have green LEDs to indicate the power good status of the intermediate supplies.

Table 1. Input Supply Fuses/Indicators, See Appendix A, Figure 4

F5	5.0V DC Input Indicator Fuse
F6	3.3V DC Input Indicator Fuse
D12	5.0V DC Input Source Good Indicator
D13	3.3V DC Input Source Good Indicator

SW4 is used to enable the off-board switching power supply module. The intermediate power supplies are supplied to the secondary POL/linear regulator supply modules. These five independent supplies are used to provide the necessary power supplies for the LatticeSC FPGA and other on-board devices. All five DC-DC outputs are fused on-board with indicating fuses and have green power good indicating LEDs.

Table 2. Board Power Supply Fuses - See Appendix A, Figure 4

Fuse	Indicator Designator	Supply Description
F8	D8	1.2V Linear Regulator- Analog 1.2V
F1	D8	1.2V POL- FPGA Core 1.2V
F2	D6	2.5V POL
F3	D9	1.5V Linear Regulator
F4	D7	3.3V POL
F7	D10	1.8V Linear Regulator

External power can be alternatively connected rather than the ATX supply. The terminal block allows connections to bench-top supplies to source power the secondary rails. Table 3 shows the terminal block TB1connections.

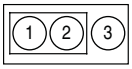
Table 3. Terminal Block Power Connection - See Appendix A, Figure 4

1	Screw terminal for +5V DC
2	Screw terminal for GND
3	Screw terminal for +3.3V DC

VCCIO1 Selection

VCCIO1 is board-programmable using jumpers J3 to select the input for the VCCIO1 voltage. For SPI Flash and Parallel Flash set this to 3.3V.

Table 4. VCCIO1 Bank Voltage Select, J3 – See Appendix A, Figure 2



1	2	3
2.5V	VCCIO1	3.3V

VCCJ

The VCCJ used for the JTAG port power supply of the LatticeSC device is supplied by 3.3V.

Programming/FPGA Configuration

ispVM Download Interface

A programming header is provided on the evaluation board that provides access to the LatticeSC JTAG port. The 10-pin 0.100" pitch header connector plugs directly into the provided mating connector.

Note: An ispDOWNLOAD® Cable is included with each ispLEVER®-Base or ispLEVER-Advanced design tool shipment. Cables may also be purchased separately from Lattice.

A 10-pin JTAG connector (J1) is used in conjunction with the ispVM USB download cable to program and control the device.

Table 5. ispVM JTAG Connector – See Appendix A, Figure 2

Pin	Function
Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN[1]
Pin 5	NC
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE[1]
Pin 10	INITN[1]

1. Optional connections.

Download Procedures

Requirements

- PC with ispVM System v.17 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

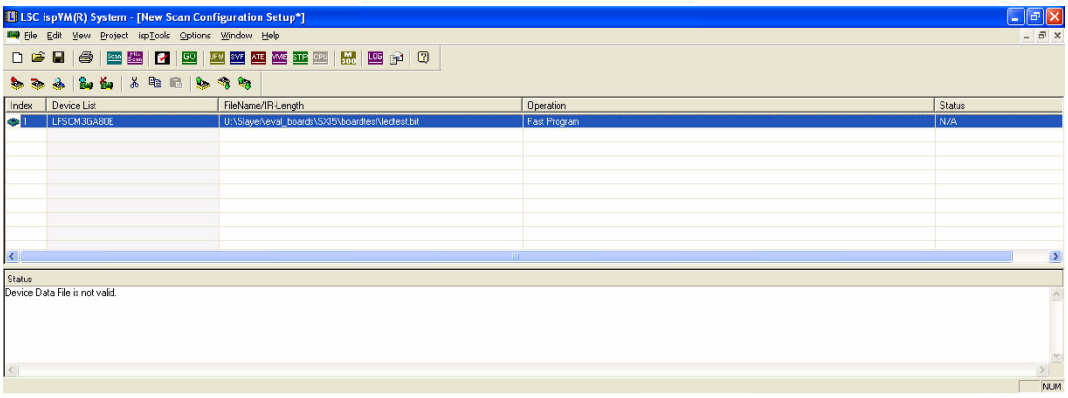
- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download

The LatticeSC device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered-on to retain its configuration when programmed in this fashion.

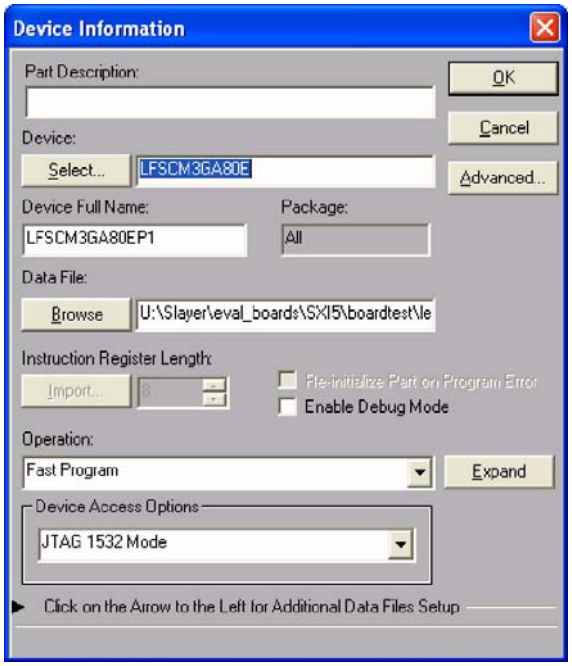
1. Connect the LatticeSC SFI-5 Evaluation Board to the appropriate power sources and power-up board.
2. Connect the ispDOWNLOAD cable to the appropriate header. J1 is used for the 1x10 cable.
3. Start the ispVM System software.
4. Press the **SCAN** button located in the toolbar. The LatticeSC device will be automatically detected.

Figure 3. ispVM System Main Window



5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.

Figure 4. ispVM System Device Information Dialog Box



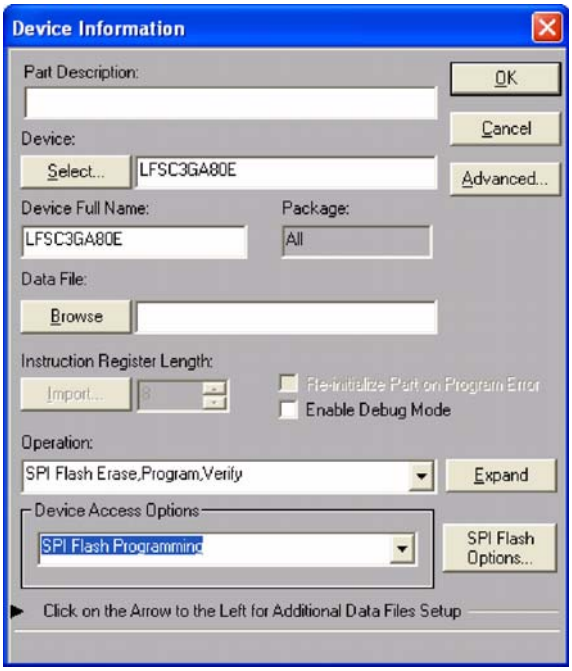
6. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

SPI Flash Programming

Standard Serial Flash is available on-board for non-volatile FPGA bitstream storage. A STMicro M25P64 Flash device, U20, can be programmed using the JTAG interface and the ispVM Download Cable and software.

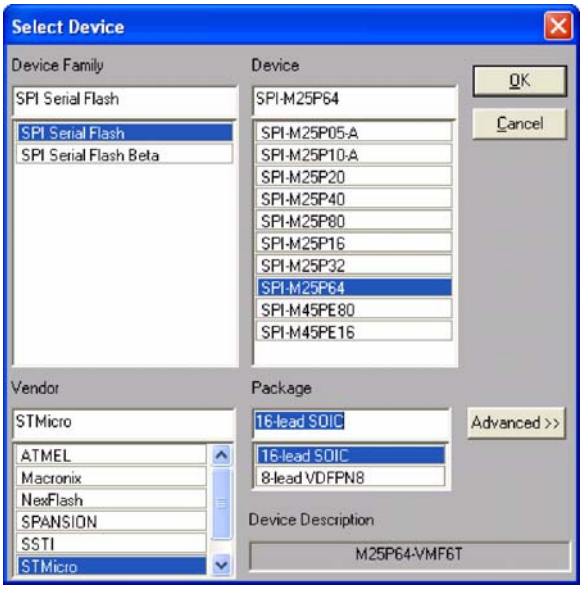
1. Following a procedure similar to the above, select **SPI Flash Programming** in the **Device Access Options** drop-down menu of the **Device Information** dialog box of the ispVM System software, as shown in Figure 5.

Figure 5. ispVM Device Information Setup



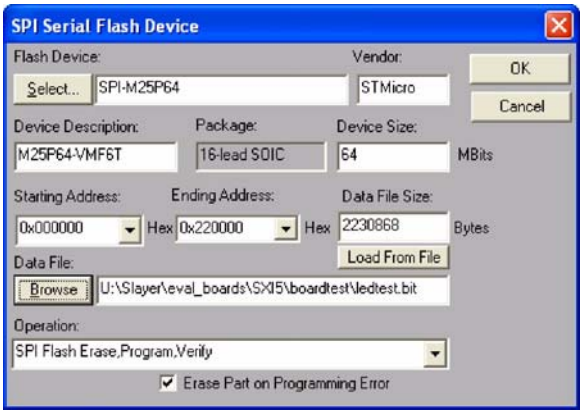
2. Select the proper SPI Flash device information as shown below. This is needed to target the supplied Flash device on the board.

Figure 6. ispVM SPI Flash Selection



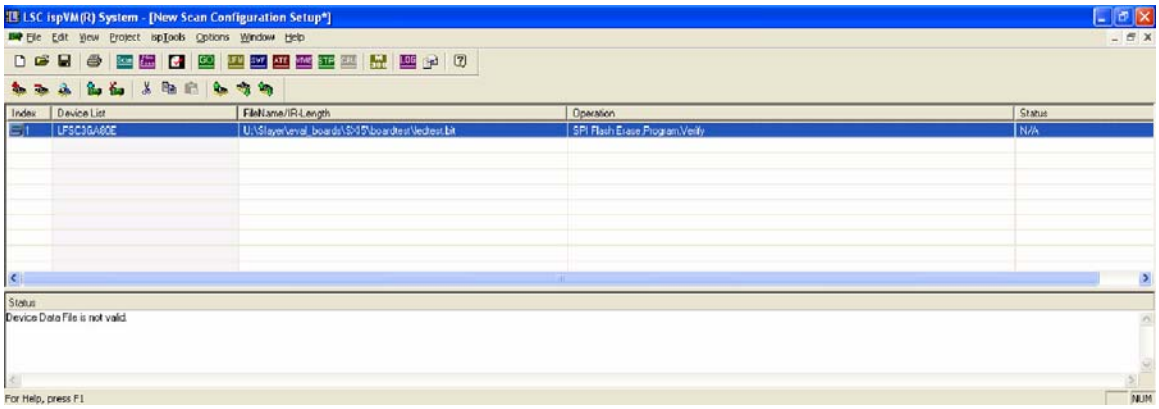
3. Next, select the target bitstream to be written to the Flash device as shown below.

Figure 7. SPI Flash Dialog Box



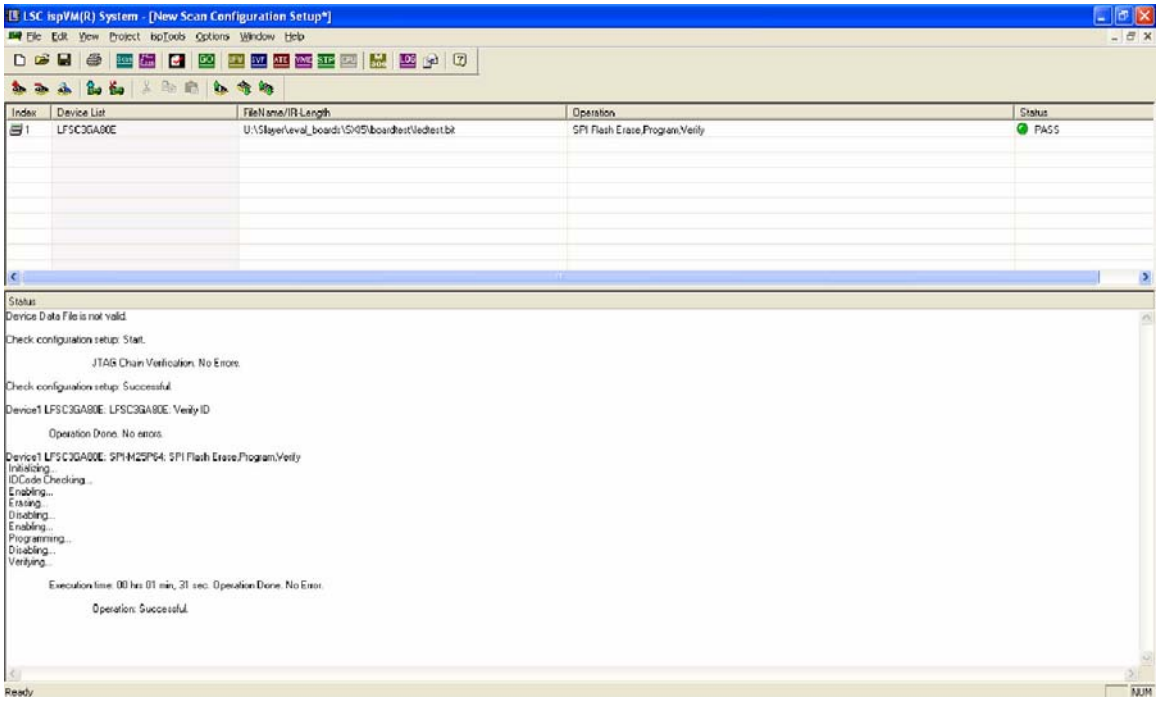
4. The ispVM system is ready to program the Flash device when **GO** is selected form the toolbar.

Figure 8. ispVM SPI Flash Loading Main Window



5. After a successful programming of the Flash device (shown below) the FPGA will read the programmed bit-stream from the Flash on a power-up or assertion of PROGRAMN (SW3)

Figure 9. ispVM Main Window with Successful SPI Flash Programming



Configuration Status Indicators

(See Appendix A, Figure 2)

These LEDs indicate the status of configuration to the FPGA.

- D1 (red) illuminated – This indicates that the programming was aborted or reinitialized, driving the INITN output low.
- D3 (green) illuminated – This indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D2 (green) flashing – This indicates TDI activity.

PROGRAMN and RESETN

(See Appendix A, Figure 2)

These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and RESETN (SW2). Depressing the button drives a logic level "0" to the device.

Red LEDs D5 (PROGRAMN) and D4 (RESETN) will light when the respective push-button above is asserted (depressed).

MODE [3:0]

(See Appendix A, Figure 2)

The FPGA Mode pins can be selected via the SW1 DIP switch. These settings must be selected according to the particular configuration mode. However for ispVM downloading via the download cable, the settings of these pins are required.

When the switches are depressed inward to the board, the respective MODE pin is driven LOW. It is driven HIGH if not depressed.

Clocks

The board is provisioned with several options to provide system-level clocking, including the means to use on-board clock sources. Off-board clocks can be sourced from SMA connections.

SERDES Reference Clock

(See Appendix A, Figure 6)

The SERDES reference clock can be supplied from a 155.52MHz clock source, Y1, to the following SERDES REFCLK pins. Adding a jumper on J9 can disable this oscillator source.

Table 6. Reference Clock Pins

SERDES REFCLK	1704-fcBGA Ball #
A_REFCLK_R[P:N]	G9:H9
B_REFCLK_R[P:N]	L14:M14
C_REFCLK_R[P:N]	J15:K15

The above reference clocks can also be driven from an off-board source from 50-ohm SMA connections.

Table 7. Clock Inputs from SMA Connections

SERDES CLOCK	SMA Designators
REFCLKP	J11
REFCLKN	J12

The SERDES reference clock sources are provisioned via stuffing resistors on the board. These resistor shunts are needed to connect the desired clock source.

Table 8. Clock Source Selection

Reference Clock Source	Stuffing Resistors Designators
Oscillator	R81, R83
SMA	R91, R92

FPGA Reference Clocks

(See Appendix A, Figure 6)

Two 50-ohm SMA connections are provided to use as an off-board clock source to FPGA I/O pins that are connected to FPGA clock routing resources.

Table 9. General FPGA Pins Connected to SMA Connectors

	1704-fcBGA Ball #	SMA Designators
FPGA REFCLKP	U2	J55
FPGA_REFCLKN	V2	J56

Generic FPGA Clock Sources

(See Appendix A, Figure 11)

A 100 MHz clock source is available to be routed to the FPGA input pins. This clock source is optional to the user and can be used for general-purpose clocking to the FLGA fabric.

Table 10. On-Board 100 MHz Clocks Pins

100 MHz Input Clock Available on 1704-fcBGA Ball #
BA27
BB27
AY27

FPGA Test Pins

(See Appendix A, Figure 11)

General-purpose FPGA pins are available for switches or LEDs based on the user's requirements.

Table 11. FPGA Test Switches and LEDs

Switch	Netname	BGA	LED	Netname	BGA
SW12A	Switch1	AM34	D20	RED1	AP34
SW12B	Switch2	AV41	D21	YELLOW1	AW39
SW12C	Switch3	AK30	D23	GREEN1	AL32
SW12D	Switch4	AW42	D25	BLUE1	AY41
SW13A	Switch5	AR37	D19	RED2	AT39
SW13B	Switch6	AV40	D22	YELLOW2	AV37
SW13C	Switch7	AN35	D24	GREEN2	AM31
SW13D	Switch8	AW40	D26	BLUE2	BA40

User Push-buttons

(See Appendix A, Figure 11)

Two push-button switches assert the logic levels on the PB1 (SW10) and PB2 (SW11).

Table 12. Push-button to FPGA Connections

Push-button	1704-fpBGA Ball #
PB1	G20
PB2	K19

Depressing either button drives a logic level "0" to the device.

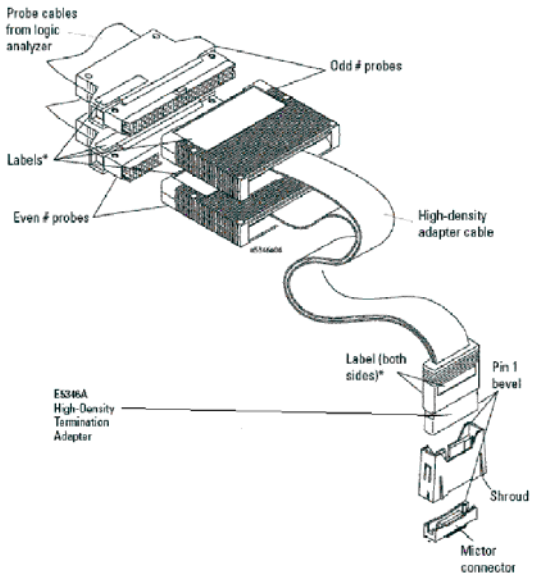
Logic Analyzer Probe

(See Appendix A, Figure 11)

An AMP/TYCO 767004 38-position .025 VERT SMD logic analyzer probe connection is provided for the user to utilize for test points. This connection provides 34 general I/O signals to be observed on a Logic Analyzer probes using Mictor connections such as the Agilent 5346A.

Table 13. Logic Analyzer To FPGA Pin Reference

Signal	1704-fcBGA Ball #	Mictor Pin	Signal	1704-fpBGA Ball #	Mictor Pin
LA1	AM29	5	LA2	AL29	6
LA3	AY39	7	LA4	AY38	8
LA5	AN33	9	LA6	AN32	10
LA7	BA39	11	LA8	BA38	12
LA9	AT37	13	LA10	AT36	14
LA11	AW36	15	LA12	AW35	16
LA13	AM28	17	LA14	AL28	18
LA15	BB38	19	LA16	BB39	20
LA17	AR34	21	LA18	AR33	22
LA19	AV35	23	LA20	AV34	24
LA21	AT33	25	LA22	AT34	26
LA23	BA37	27	LA24	BA36	28
LA25	AP33	29	LA26	AP32	30
LA27	AY36	31	LA28	AY35	32
LA29	AN31	33	LA30	AN30	34
LA31	BB37	35	LA32	BB36	36
LA33	AP31	37	LA34	AP30	38



LCD Interface

(See Appendix A, Figure 11)

A 2x8 header (J70) provides a connection to 16-character x 2 line LCD modules such as Varitronix VDM16265. A ribbon cable connection will allow attachment to the connector. The board includes two variable resistors for LCD adjustments. VR1 adjusts the backlight and VR2 provides contrast adjustment. A user design must be included in the FPGA to drive this feature.

RS-232

(See Appendix A, Figures 11)

A 2x10 header (J71) provides a connection for simple RS-232 communications to the FPGA via a level shifter IC. The FPGA is required to contain the RS232 communications design.

Table 14. RS-232 Signals

RS-232 Signal	1704-fpBGA Ball #
TXD	BB34
RXD	AN29

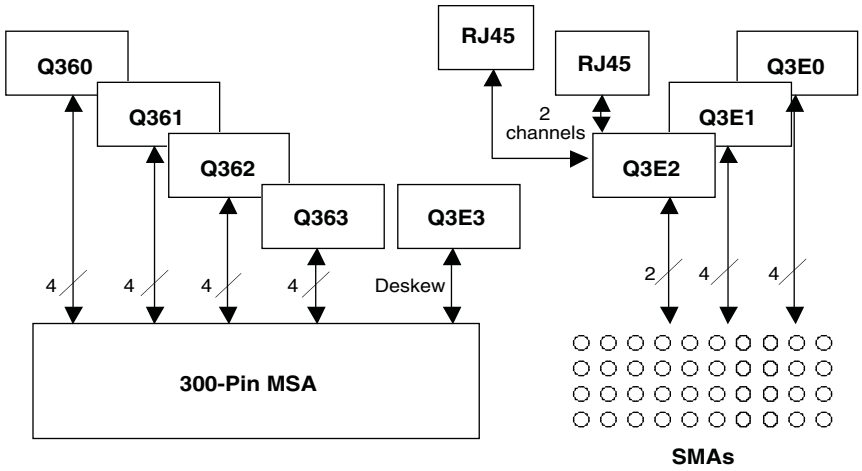
An I^2C bus is included on-board. It interfaces between the FPGA, the 300-pin MSA transponder and two peripheral components. An I^2C design is needed inside the FPGA to communicate across this bus.

The peripheral components are a Maxim MAX6692 temperature sensing IC (U6) which is interfaced to the FPGA temperature sensing diode and an I^2C accessible EEPROM (U7) which is available for user-defined requirements.

SERDES Channels

The SERDES are allocated on the evaluation board for several functions. The board is designed primarily for SFI-5 applications. Other SERDES resources not required for SFI-5 can be used for other generic applications or demonstrations.

Figure 10. SERDES Provisioning Block Diagram



DC-coupled SMA connectors connect to the SERDES Tx and Rx channels. These pins are directly coupled to the designated SMA connector, creating a path for both input and output differential data.

Table 15. SERDES Connectors - See Appendix A, Figure 6

SERDES CHANNEL	1704-fpBGA Ball #	SMA	SERDES CHANNEL	1704-fpBGA Ball #	SMA
3E0_CH0_INP_SC	C1	J13	3E1_CH0_INP_SC	D6	J15
3E0_CH0_INN_SC	D1	J14	3E1_CH0_INN_SC	E6	J16
3E0_CH1_INP_SC	D3	J19	3E1_CH1_INP_SC	D7	J21
3E0_CH1_INN_SC	E3	J20	3E1_CH1_INN_SC	E7	J22
3E0_CH2_INP_SC	D4	J25	3E1_CH2_INP_SC	D8	J27
3E0_CH2_INN_SC	E4	J26	3E1_CH2_INN_SC	E8	J28
3E0_CH3_INP_SC	D5	J29	3E1_CH3_INP_SC	D9	J31
3E0_CH3_INN_SC	E5	J30	3E1_CH3_INN_SC	E9	J32
3E0_CH0_OUTP_SC	A3	J33	3E1_CH0_OUTP_SC	B7	J35
3E0_CH0_OUTN_SC	B3	J34	3E1_CH0_OUTN_SC	A7	J36
3E0_CH1_OUTP_SC	B4	J39	3E1_CH1_OUTP_SC	B8	J41
3E0_CH1_OUTN_SC	A4	J40	3E1_CH1_OUTN_SC	A8	J42
3E0_CH2_OUTP_SC	A5	J45	3E1_CH2_OUTP_SC	B9	J47
3E0_CH2_OUTN_SC	B5	J46	3E1_CH2_OUTN_SC	A9	J48
3E0_CH3_OUTP_SC	A6	J49	3E1_CH3_OUTP_SC	B10	J51
3E0_CH3_OUTN_SC	B6	J50	3E1_CH3_OUTN_SC	A10	J52
3E2_CH0_INP_SC	D10	J17	3E2_CH0_OUTP_SC	B11	J37
3E2_CH0_INN_SC	E10	J18	3E2_CH0_OUTN_SC	A11	J38
3E2_CH1_INP_SC	D11	J23	3E2_CH1_OUTP_SC	B12	J43
3E2_CH1_INN_SC	E11	J24	3E2_CH1_OUTN_SC	A12	J44

300-pin MSA SFI5 Transponder Interface

(See Appendix A, Figure 13)

The MSA1 connector provides an interface for interoperability to 300-pin SFI-5 transponders. The interface is complete with high-speed parallel connections to the LatticeSC device, as well as clocking, status, control, and power. The high-speed interface pin-out is outlined in Table 16.

Table 16. SXI/SFI-5 Data Channels

1704-fpBGA Ball #	SERDES Channel	SXI-5 Signal	300-MSA	1704-fpBGA Ball #	SERDES Channel	SXI-5 SIGNAL	300-MSA
D38	360_CH3_INP_SC	SXI5_RXD0P	A1	A37	360_CH3_OUTP_SC	SXI5_TXD0P	A20
E38	360_CH3_INN_SC	SXI5_RXD0N	A2	B37	360_CH3_OUTN_SC	SXI5_TXD0N	A21
D39	360_CH2_INP_SC	SXI5_RXD1P	A4	A38	360_CH2_OUTP_SC	SXI5_TXD1P	A23
E39	360_CH2_INN_SC	SXI5_RXD1N	A5	B38	360_CH2_OUTN_SC	SXI5_TXD1N	A24
D40	360_CH1_INP_SC	SXI5_RXD2P	A7	B39	360_CH1_OUTP_SC	SXI5_TXD2P	A26
E40	360_CH1_INN_SC	SXI5_RXD2N	A8	A39	360_CH1_OUTN_SC	SXI5_TXD2N	A27
C42	360_CH0_INP_SC	SXI5_RXD3P	A10	A40	360_CH0_OUTP_SC	SXI5_TXD3P	A29
D42	360_CH0_INN_SC	SXI5_RXD3N	A11	B40	360_CH0_OUTN_SC	SXI5_TXD3N	A30
D34	361_CH3_INP_SC	SXI5_RXD4P	C1	B33	361_CH3_OUTP_SC	SXI5_TXD4P	C20
E34	361_CH3_INN_SC	SXI5_RXD4N	C2	A33	361_CH3_OUTN_SC	SXI5_TXD4N	C21
D35	361_CH2_INP_SC	SXI5_RXD5P	C4	B34	361_CH2_OUTP_SC	SXI5_TXD5P	C23
E35	361_CH2_INN_SC	SXI5_RXD5N	C5	A34	361_CH2_OUTN_SC	SXI5_TXD5N	C24

Table 16. SXI/SFI-5 Data Channels (Continued)

1704-fpBGA Ball #	SERDES Channel	SXI-5 Signal	300-MSA	1704-fpBGA Ball #	SERDES Channel	SXI-5 SIGNAL	300-MSA
D36	361_CH1_INP_SC	SXI5_RXD6P	C7	B35	361_CH1_OUTP_SC	SXI5_TXD6P	C26
E36	361_CH1_INN_SC	SXI5_RXD6N	C8	A35	361_CH1_OUTN_SC	SXI5_TXD6N	C27
D37	361_CH0_INP_SC	SXI5_RXD7P	C10	B36	361_CH0_OUTP_SC	SXI5_TXD7P	C29
E37	361_CH0_INN_SC	SXI5_RXD7N	C11	A36	361_CH0_OUTN_SC	SXI5_TXD7N	C30
D30	362_CH3_INP_SC	SXI5_RXD8P	E1	B29	362_CH3_OUTP_SC	SXI5_TXD8P	E20
E30	362_CH3_INN_SC	SXI5_RXD8N	E2	A29	362_CH3_OUTN_SC	SXI5_TXD8N	E21
E31	362_CH2_INP_SC	SXI5_RXD9P	E4	B30	362_CH2_OUTP_SC	SXI5_TXD9P	E23
F31	362_CH2_INN_SC	SXI5_RXD9N	E5	A30	362_CH2_OUTN_SC	SXI5_TXD9N	E24
D32	362_CH1_INP_SC	SXI5_RXD10P	E7	B31	362_CH1_OUTP_SC	SXI5_TXD10P	E26
E32	362_CH1_INN_SC	SXI5_RXD10N	E8	A31	362_CH1_OUTN_SC	SXI5_TXD10N	E27
D33	362_CH0_INP_SC	SXI5_RXD11P	E10	B32	362_CH0_OUTP_SC	SXI5_TXD11P	E29
E33	362_CH0_INN_SC	SXI5_RXD11N	E11	A32	362_CH0_OUTN_SC	SXI5_TXD11N	E30
D26	363_CH3_INP_SC	SXI5_RXD12P	G1	B25	363_CH3_OUTP_SC	SXI5_TXD12P	G20
E26	363_CH3_INN_SC	SXI5_RXD12N	G2	A25	363_CH3_OUTN_SC	SXI5_TXD12N	G21
D27	363_CH2_INP_SC	SXI5_RXD13P	G4	B26	363_CH2_OUTP_SC	SXI5_TXD13P	G23
E27	363_CH2_INN_SC	SXI5_RXD13N	G5	A26	363_CH2_OUTN_SC	SXI5_TXD13N	G24
D28	363_CH1_INP_SC	SXI5_RXD14P	G7	B27	363_CH1_OUTP_SC	SXI5_TXD14P	G26
E28	363_CH1_INN_SC	SXI5_RXD14N	G8	A27	363_CH1_OUTN_SC	SXI5_TXD14N	G27
D29	363_CH0_INP_SC	SXI5_RXD15P	G10	B28	363_CH0_OUTP_SC	SXI5_TXD15P	G29
E29	363_CH0_INN_SC	SXI5_RXD15N	G11	A28	363_CH0_OUTN_SC	SXI5_TXD15N	G30
E17	3E3_CH3_INP_SC	SXI5_RXDSCP	J1	B18	3E3_CH3_OUTP_SC	SXI5_TXDSCP	J20
F17	3E3_CH3_INN_SC	SXI5_RXDSCN	J2	A18	3E3_CH3_OUTN_SC	SXI5_TXDSCN	J21

Reference clocks are available to interface via the SFI/SXI-5 interface. These clocks are connected between FPGA differential I/O pins and the MSA connector.

Table 17. SFI-5 Clock Interface

1704-fpBGA Ball #	FPGA I/O	SFI5 SIGNAL	300-MSA
AA9	PCLKT2_2-LVDS IN	SXI5_RXDCKP	J4
AB9	PCLKC2_2-LVDS IN	SXI5_RXDCKP	J5
R1	PCLKT2_0-LVDS OUT	SXI5_TXDCKP	J23
T1	PCLKC2_0-LVDS OUT	SXI5_TXDCKP	J24
T3	PCLKT2_1-LVDS IN	SXI5_TXCKSRCP	J26
U3	PCLKC2_1-LVDS IN	SXI5_TXCKSRCN	J27

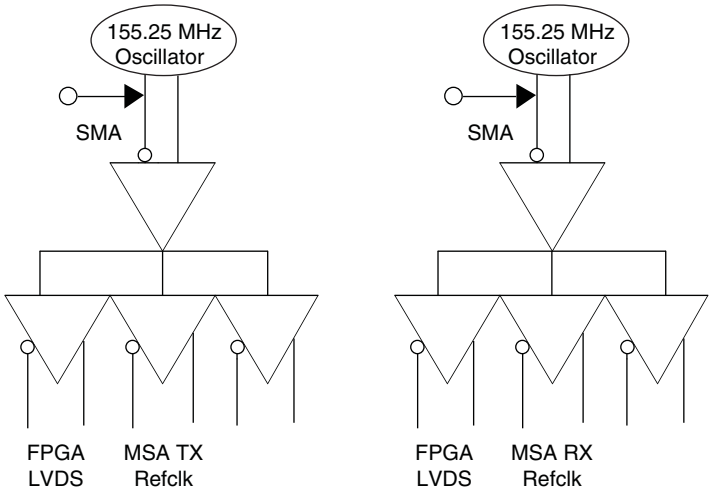
MSA Reference Clocks

Reference clocks needed for MSA-based transponders are sourced from a clock distribution network on the board. The board allows for a fixed frequency oscillator or SMA input to drive the clock distribution. The clock is fanned out to the MSA reference clocks needed to operated the transponder and to pre-defined FPGA inputs that drive clock routing resources of the FPGA fabric.

Table 18. MSA Clock Resources

Net Name	MSA Pin	1704-fpBGA Ball #	Source Clock
SXI5_RXREFCLKP	J7	R42	Oscillator (Y2) SMA J64 and J65
SXI5_RXREFCLKN	J8	T42	
SXI5_TXREFCLKP	J29	T40	Oscillator (Y3) SMA J68 and J69

Figure 11. MSA Clock Distribution



MSA Power Supplies

(See Appendix A, Figure 14)

The MSA is powered by off-board connections to external supplies not provided with the evaluation board. Some of the supply connections are fuse protected on-board. If an optical transponder in used in conjunction with this board, all supplies used by the transponder must be carefully selected and connect to the supplied screw terminal connection (TB4).

Table 19. MSA Power Indicators - See Appendix A, Figure 14

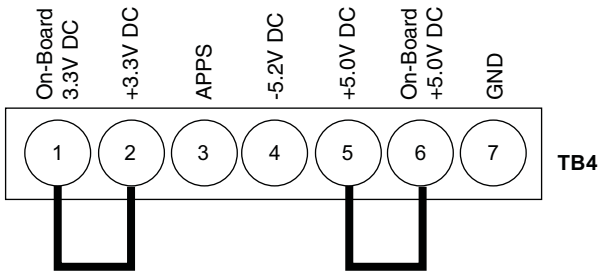
F14	MSA APPS Supply Fuse
F12	MSA +3.3V DC Analog Supply Fuse
F11	MSA +5V DC Analog Supply Good Fuse
F13	MSA -5.2V DC Analog Supply Good Fuse
F15	MSA -5.2V DC Digital Supply Good Fuse

Terminal Block TB4 connects to external supplies for supplying the 300-pin module. The connector requires external supplies to source power to the MSA-defined supplies.

Table 20. External Power Connection for MSA Supplies

Terminal	Required Supply
2	+3.3V DC
3	APPS Supply transponder specific
4	-5.2V DC
5	+5V DC
6	GND

Figure 12. MSA Power Input Detail



Note: Terminals 1 and 6 should be no connects except when needed to connect on-board 3.3V and 5V supplies. In this scenario, a jumper between Terminals 1 and 2 or 5 and 6 will allow for the on-board supplies to provide the respective supplies to the MSA.

MSA Status Indicators

The status signals of the MSA interface are observed via the LED indicators listed below

Table 21. MSA Status Indicators – See Appendix A, Figure 12

D14	MSA CFG_ALM (red = 0, green = 1)
D17	MSA LOS (red =0, green =1)
D16	MSA STATUS INTERUPT ALARM (red = active)
D15	MSA RXS ALARM (red = active)

MSA Control Switches

SW8 and SW9 are push-button switches used to drive the MSA REG_RSTN and MOD_RSTN pins to logic "0" when depressed.

The SW6 DIP switch is included on-board to set static setting to the MSA control pins.

Positions 1, 2, and 3 select the I^2C address for the MSA transponder.

Position 9 disables the transponder laser when placed in the ON position

Position 10 selects the TX LINE SEL of the MSA module.

FPGA Control of MSA Pins

There are several MSA pins that can be controlled and monitored from pins of the FPGA design.

Table 22. MSA Signals to FPGA

MSA Signal	1704-fcBGA Ball #
TXLINETIMSEL0	AU23
LASERENABLE	AY23
STAT_INT	AN23
RXS	AW24
CFG_ALM	AM23
LOS	BB24
REG_RSTN	AU24
MOD_RSTN	BA25

Dedicated VDDIB/VDDOB SERDES Power Supplies

VDDIB and VDDOB supplies are provided on-board by two independent regulators. Each regulator is factory-provisioned to provide a fused 1.2V termination supply to the LatticeSC SERDES.

Table 23. VDDIB/VDDOB Fuses

Supply	Fuse
VDDOB	F9
VDDIB	F10

Miscellaneous Hardware

SFI5 Electrical Loop-back

This evaluation board includes a loop-back PCB that can be alternately used in place of the optical module. The loop-back board includes the proper electrical connections for the SERDES to transmit and receive for far-end loop-back testing.

SFI5 Electrical SMA Breakout

The loop-back board will also serve as the SMA breakout board. The loop-back function and the SMA breakout is connected to the SERDES outputs.

Cat5/5E/6 Electrical Media RJ-45 Connection

(See Appendix A, Figure 6)

RJ-45 connections are included on the board for the purpose of testing and demonstrating the physical layer electrical performance of the SERDES. Interconnections between the SERDES CML I/Os allow for electrical loop-back between the two RJ-45 connectors with CAT cabling.

Table 24. RJ-45 Pinout

RJ-45 CAT5 (TIA-568) Pairing 1-2 3-6 4-5 7-8	J53	SERDES Channel	1704-fcBGA Ball #
	1	3E2_CH2_INP_SC	D12
	2	3E2_CH2_INN_SC	E12
	3	3E2_CH3_OUTP_SC	B14
	4	3E3_CH0_OUTN_SC	A15
	5	3E3_CH0_OUTP_SC	B15
	6	3E2_CH3_OUTN_SC	A14
	7	3E3_CH1_INN_SC	F15
	8	3E3_CH1_INP_SC	E15
	J54	**SERDES Channel**	**1704-fcBGA Ball #**
	1	3E2_CH2_OUTP_SC	B13
	2	3E2_CH2_OUTN_SC	A13
	3	3E2_CH3_INP_SC	D13
	4	3E3_CH0_INN_SC	E14
	5	3E3_CH0_INP_SC	D14
	6	3E2_CH3_INN_SC	E13
	7	3E3_CH1_OUTN_SC	A16
	8	3E3_CH1_OUTP_SC	B16

QDR2+ Memory Interface Support

The LatticeSC SFI-5 Evaluation Board is equipped with a Cypress CY7C1165V18 QDR2+ memory device (U22). The memory interface includes a 36-bit wide bus to the FPGA. The evaluation board includes termination of address, command, and control lines to the device.

Table 25. QDR2+ Memory Interface- Appendix A, Figure 9

1704-fcBGA Ball #	QDR2 Device BGA	Signal
AD39	R3	QDR_A0
AC39	R4	QDR_A1
AB42	P4	QDR_A2
AA42	R5	QDR_A3
AB38	P5	QDR_A4
AA38	N5	QDR_A5
Y41	N6	QDR_A6
W41	N7	QDR_A7
AA36	P7	QDR_A8
Y40	R7	QDR_A9
W40	P8	QDR_A10
AC32	R8	QDR_A11
Y39	R9	QDR_A12
W39	B4	QDR_A13
AB35	C5	QDR_A14
Y38	C7	QDR_A15
W38	B8	QDR_A16
AF41	P10	QDR_D0
AF39	N11	QDR_D1
AG39	M11	QDR_D2
AH36	K10	QDR_D3
AG35	J11	QDR_D4
AH42	G11	QDR_D5
AJ41	E10	QDR_D6
AJ37	D11	QDR_D7
AE41	C11	QDR_D8
AE31	N10	QDR_D9
AG36	M9	QDR_D10
AF40	L9	QDR_D11
AG33	J9	QDR_D12
AH33	G10	QDR_D13
AK42	F9	QDR_D14
AJ42	D10	QDR_D15
AK37	C9	QDR_D16
AK41	B9	QDR_D17
AE32	B3	QDR_D18
AG40	C3	QDR_D19
AK34	D2	QDR_D20
AG34	F3	QDR_D21

Table 25. QDR2+ Memory Interface- Appendix A, Figure 9 (Continued)

1704-fcBGA Ball #	QDR2 Device BGA	Signal
AH34	G2	QDR_D22
AG41	J3	QDR_D23
AF38	L3	QDR_D24
AE42	M3	QDR_D25
AF42	N2	QDR_D26
AG37	C1	QDR_D27
AH37	D1	QDR_D28
AF31	E2	QDR_D29
AH35	G1	QDR_D30
AG42	J1	QDR_D31
AH41	K2	QDR_D32
AF32	M1	QDR_D33
AJ40	N1	QDR_D34
AK40	P2	QDR_D35
AD37	P11	QDR_Q0
AC34	M10	QDR_Q1
V6	L11	QDR_Q2
U42	K11	QDR_Q3
AE33	J10	QDR_Q4
AE36	F11	QDR_Q5
AF37	E11	QDR_Q6
AB41	C10	QDR_Q7
AE37	B11	QDR_Q8
AA41	P9	QDR_Q9
AD33	N9	QDR_Q10
AD29	L10	QDR_Q11
AE35	G9	QDR_Q13
AB37	F10	QDR_Q14
AD40	E9	QDR_Q15
AD38	D9	QDR_Q16
AB36	B10	QDR_Q17
AD36	B2	QDR_Q18
AA37	D3	QDR_Q19
AC40	E3	QDR_Q20
AF34	F2	QDR_Q21
AD35	G3	QDR_Q22
AD42	K3	QDR_Q23
AC33	L2	QDR_Q24
AC38	N3	QDR_Q25
AF33	B1	QDR_Q27
AA35	C2	QDR_Q28
AB31	E1	QDR_Q29
AC37	F1	QDR_Q30
AC31	L1	QDR_Q33

Table 25. QDR2+ Memory Interface- Appendix A, Figure 9 (Continued)

1704-fcBGA Ball #	QDR2 Device BGA	Signal
AC29	M2	QDR_Q34
AD34	P1	QDR_Q35
AC42	P6	QDR_QVLD
AK36	B6	QDR_K
AL36	A6	QDR_K_#
AF29	A8	QDR_READ_N
AG29	A4	QDR_WRITE_N
U41	A11	QDR_CQ
V41	A1	QDR_CQ#

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
		

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
November 2008	01.0	Initial release.

Appendix A. Schematic

Figure 13. Cover Page

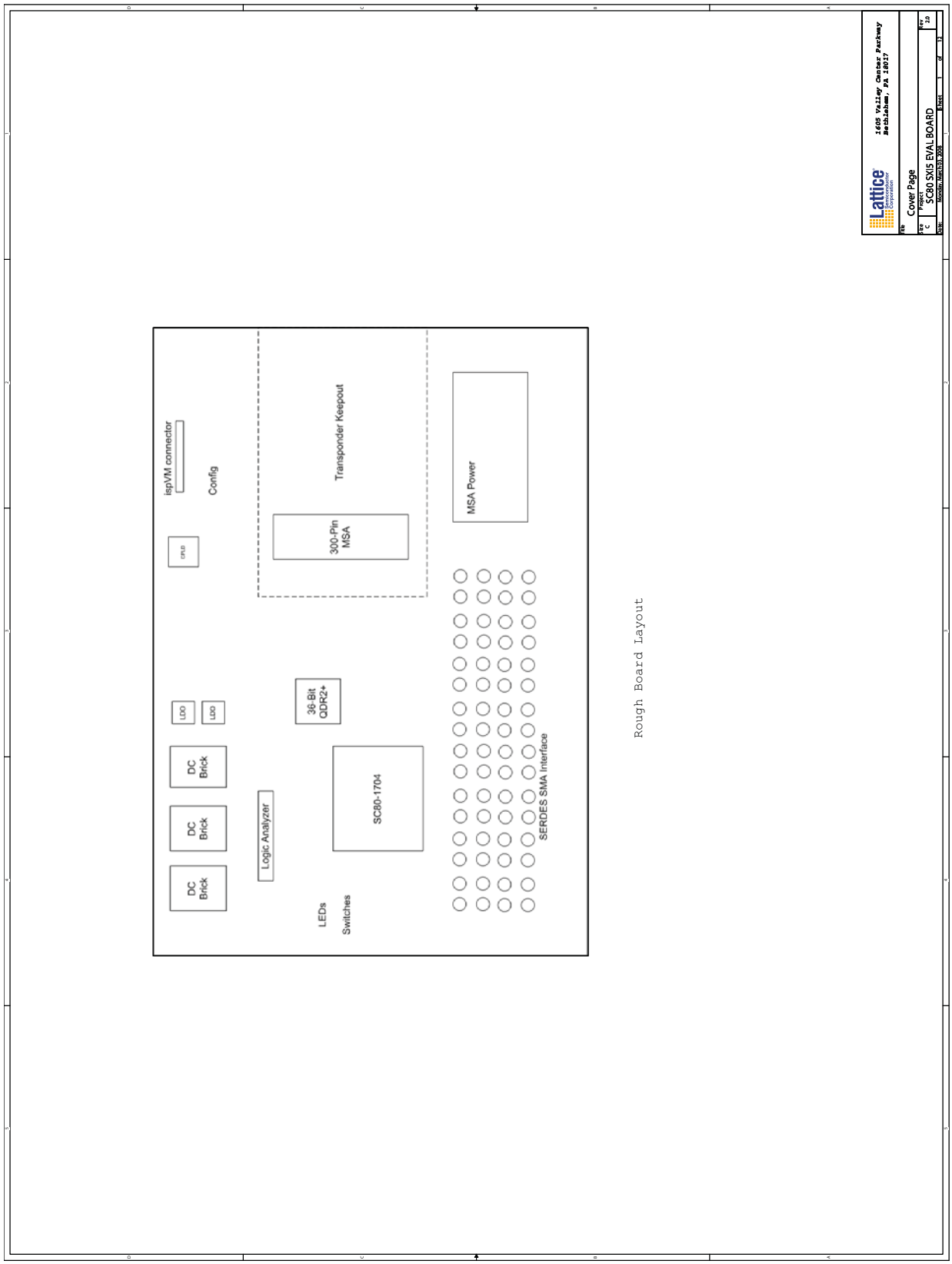


Figure 14. Configuration

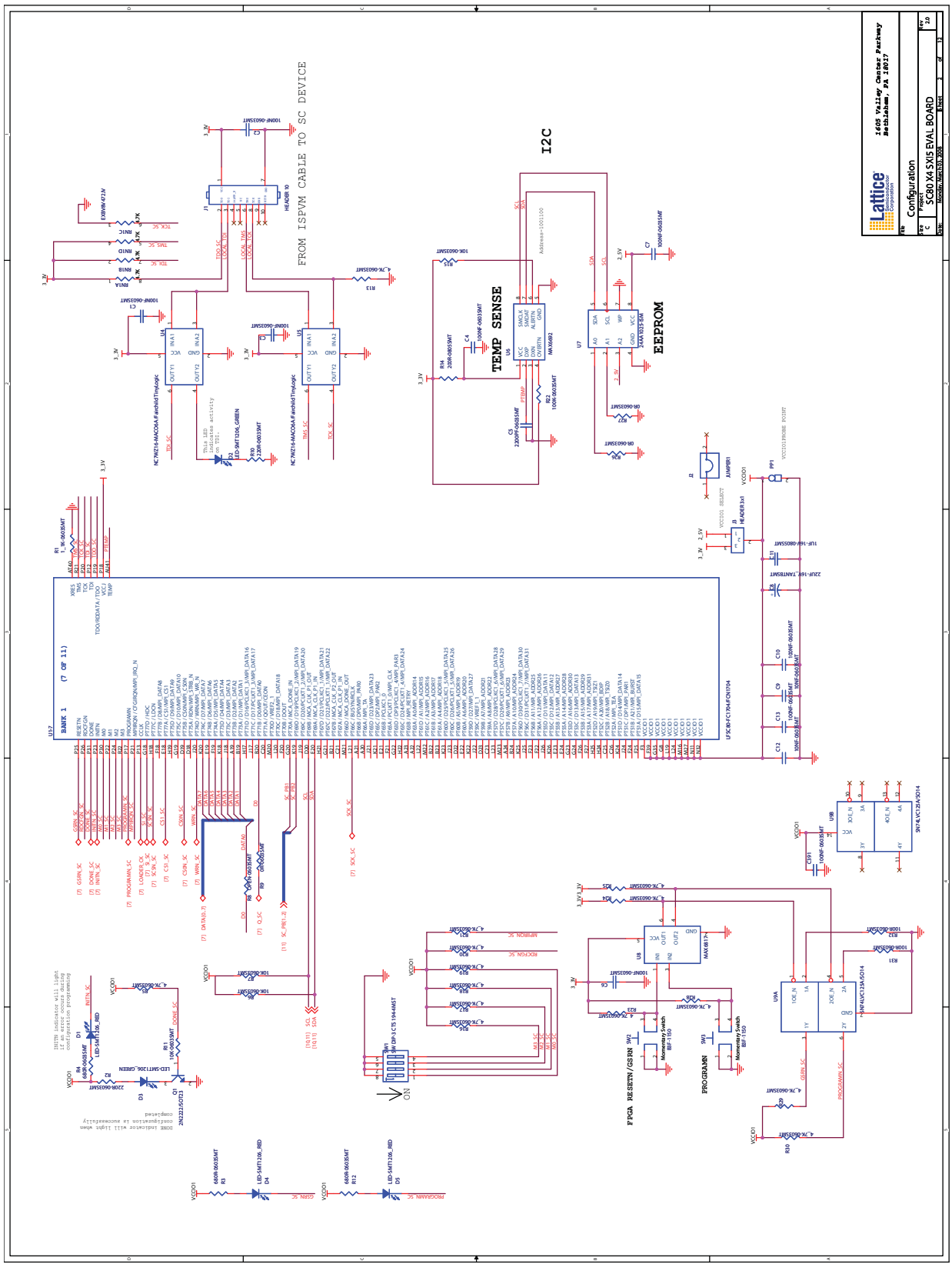


Figure 15. Power Supplies SC 1

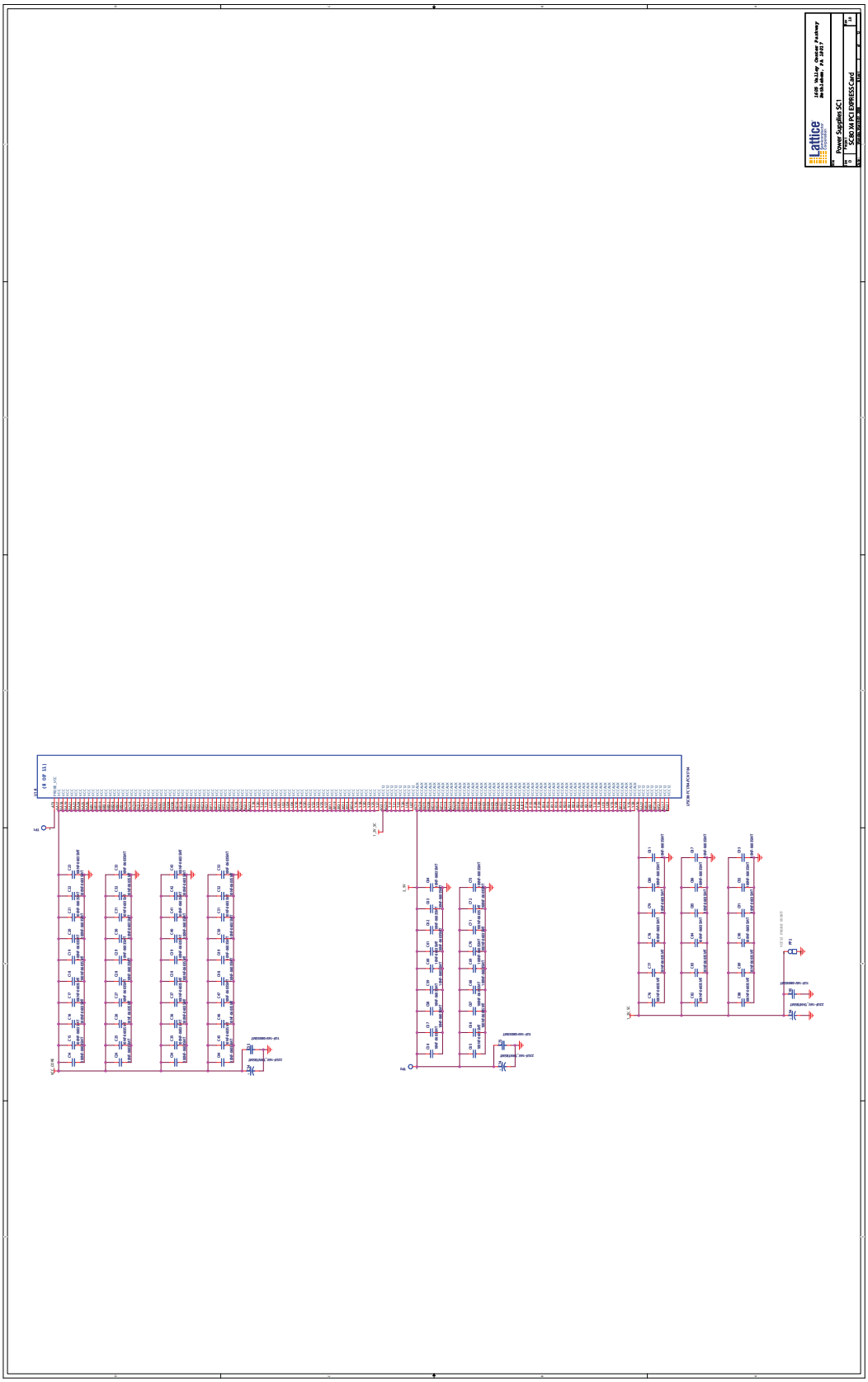


Figure 16. DC/DC Conversion

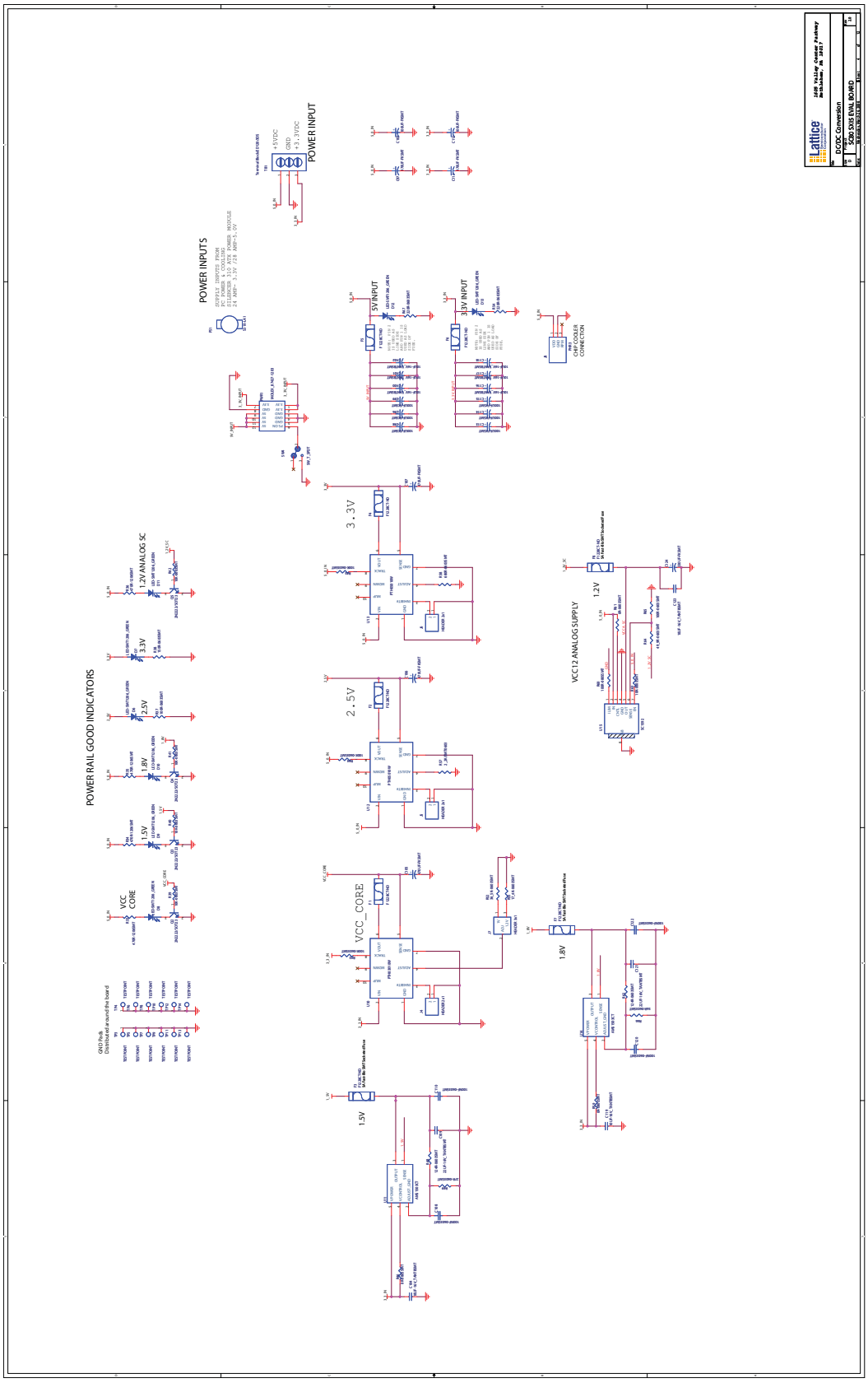


Figure 17. VSS/Decoupling

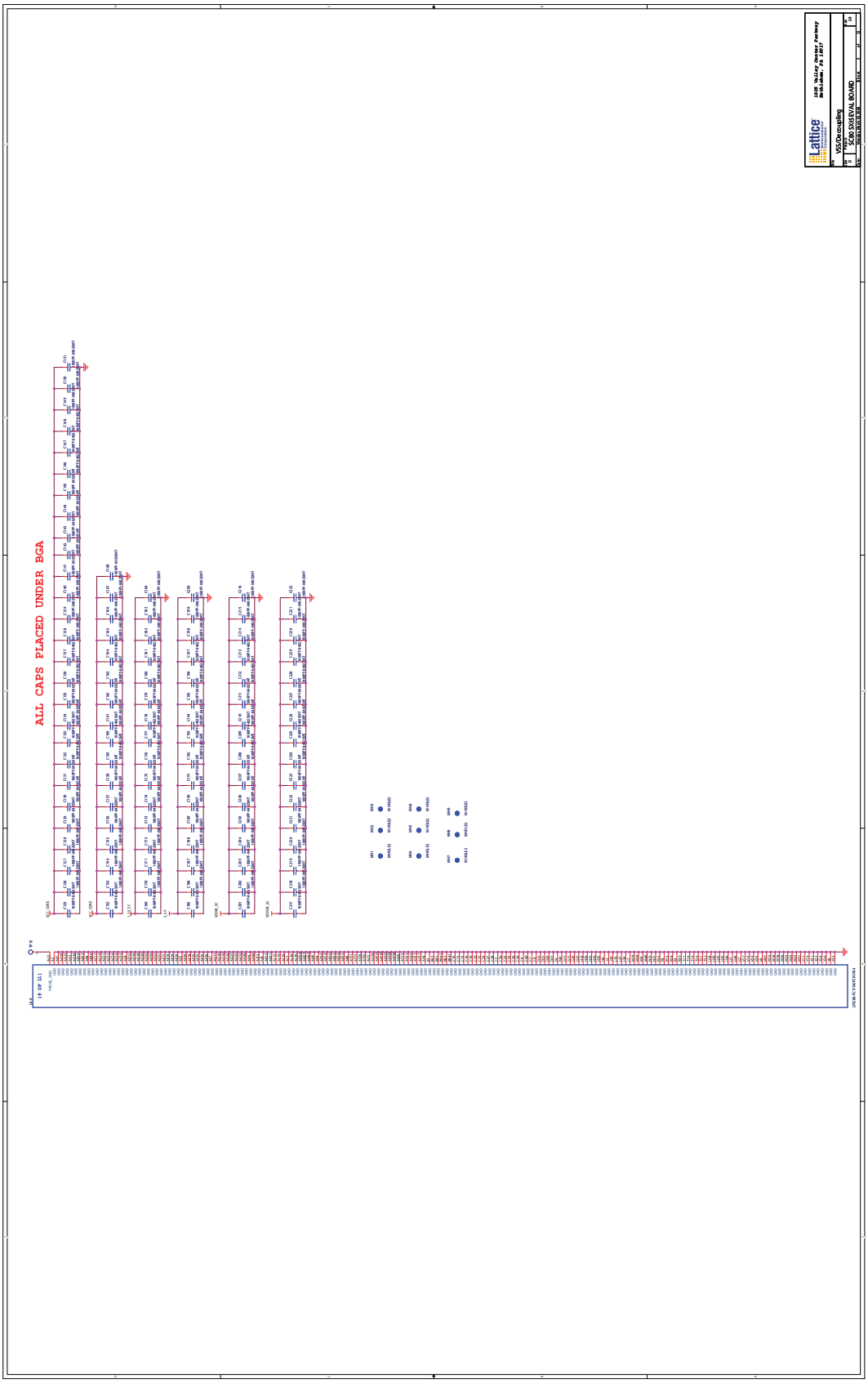


Figure 18. SERDES

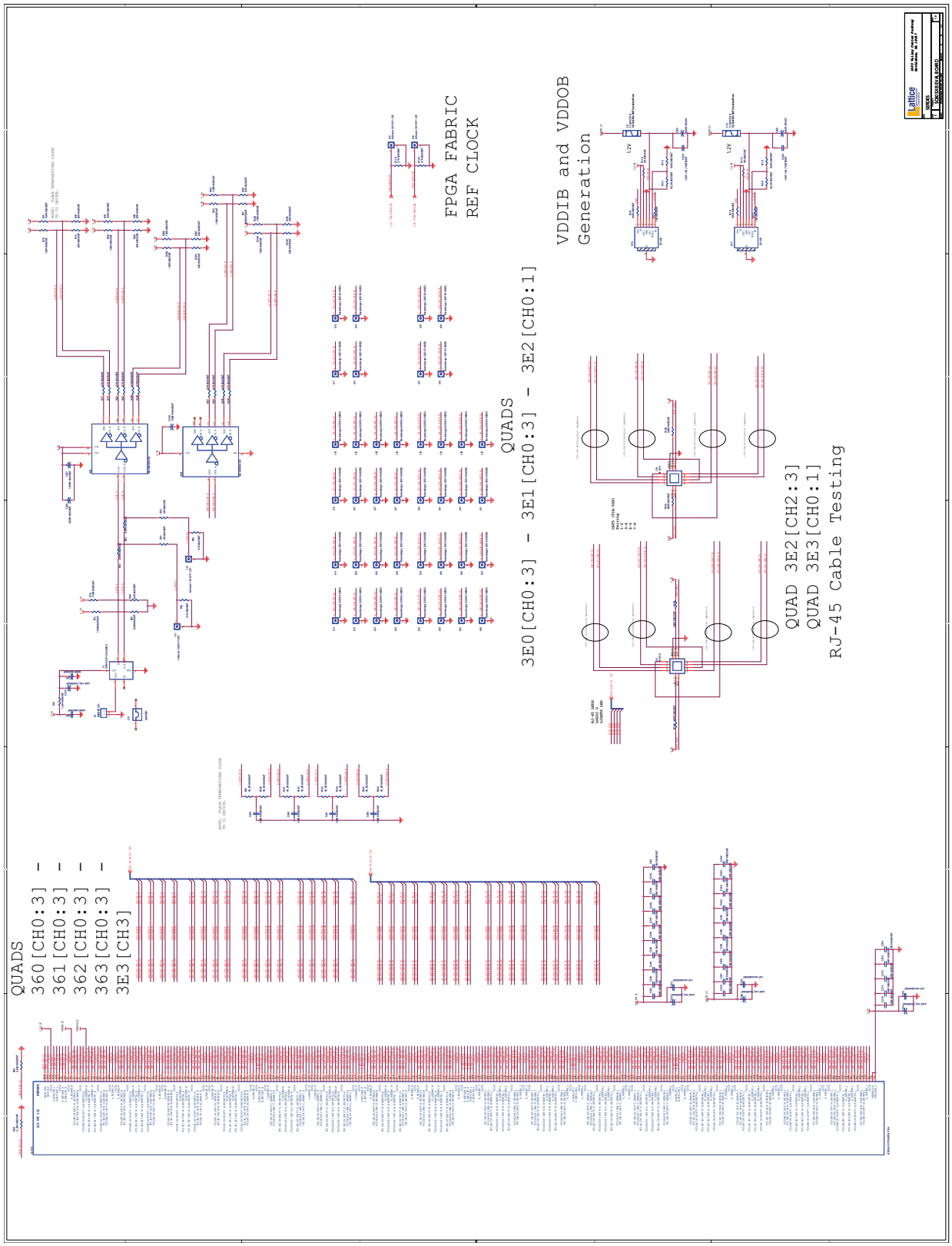


Figure 19. Flash Configuration

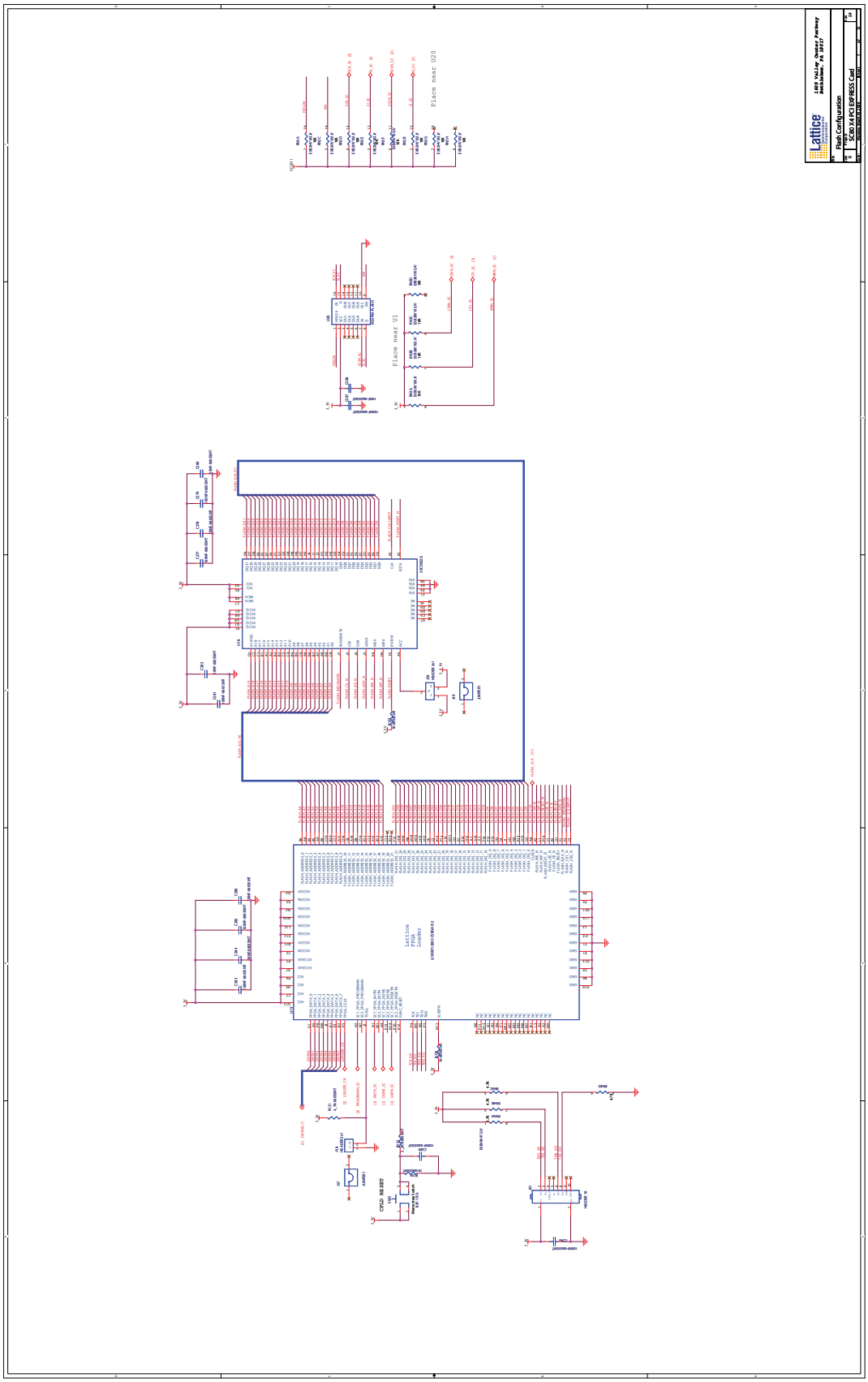


Figure 20. Memory Control Interface

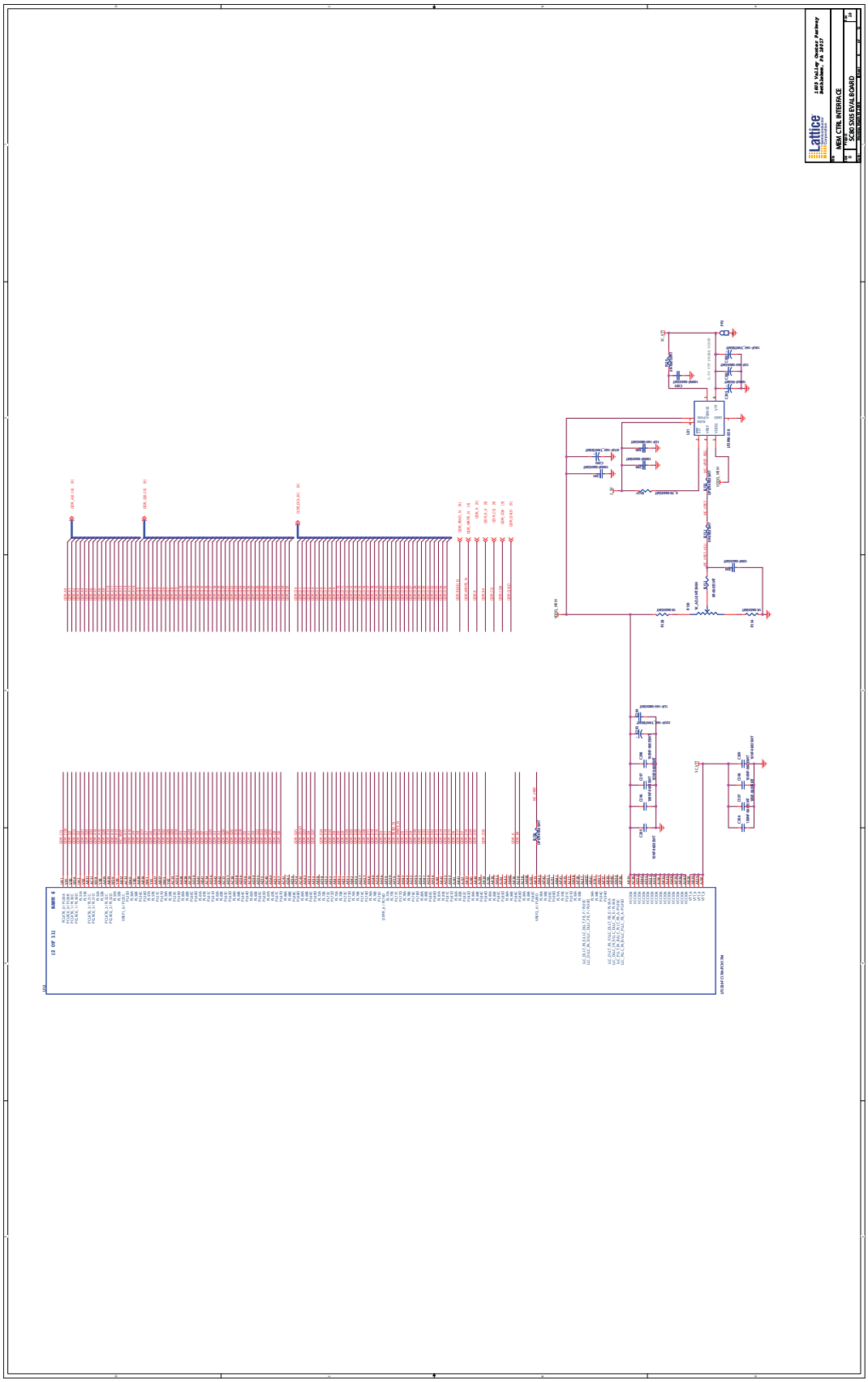


Figure 21. QDR Memory Device

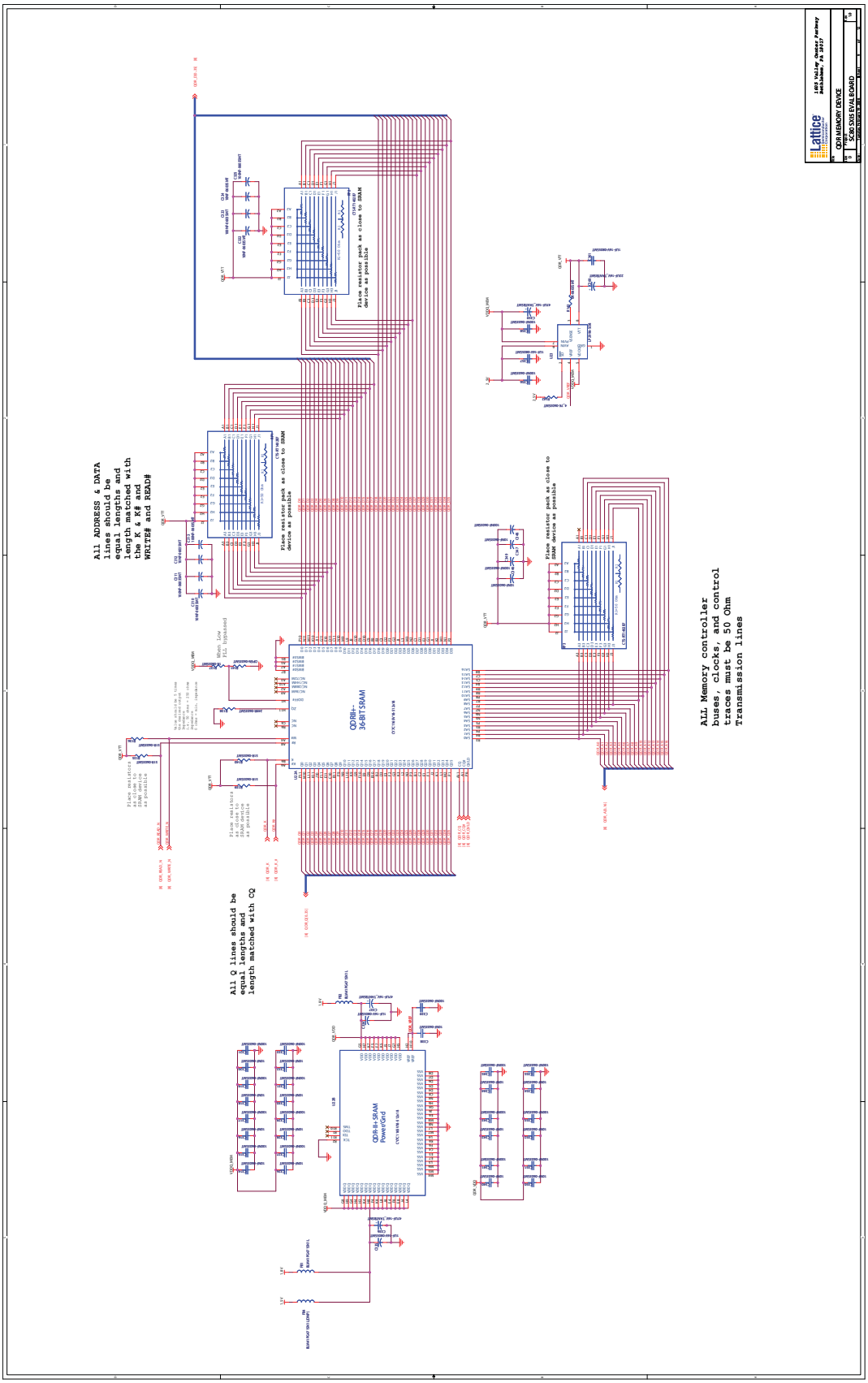


Figure 22. SFI-5 MSA Connection

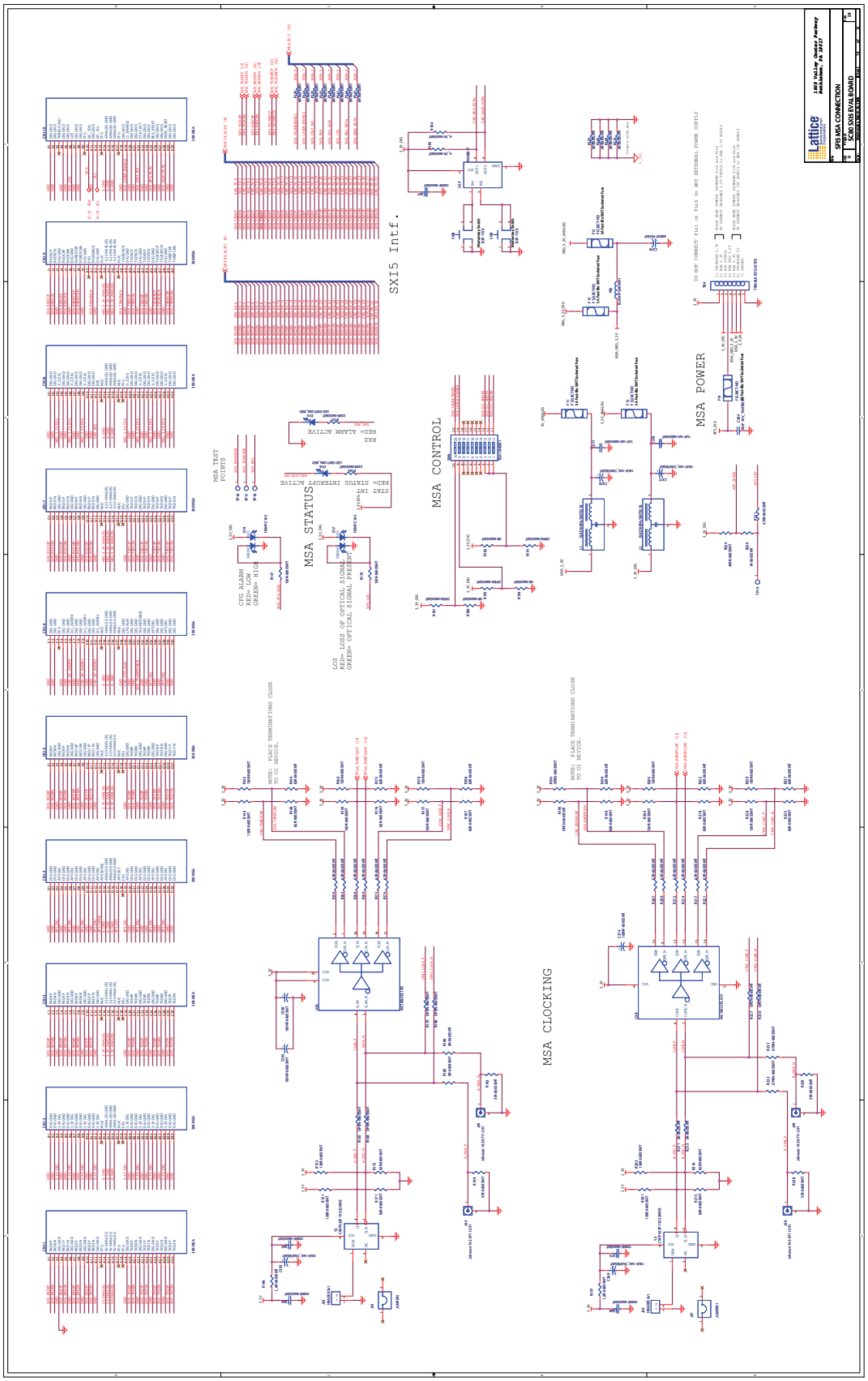


Figure 23. Test Pins

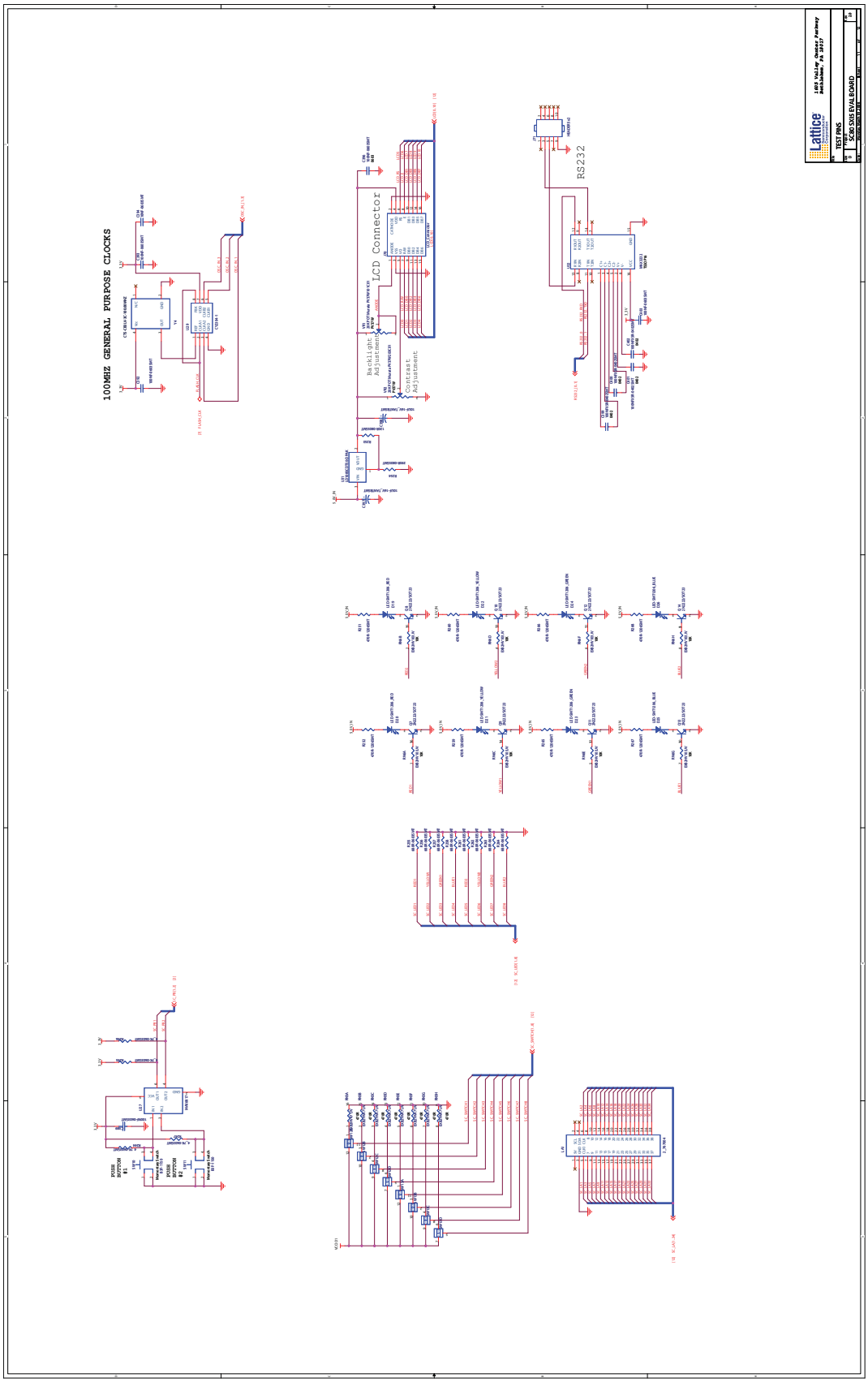


Figure 24. Other Device Pins