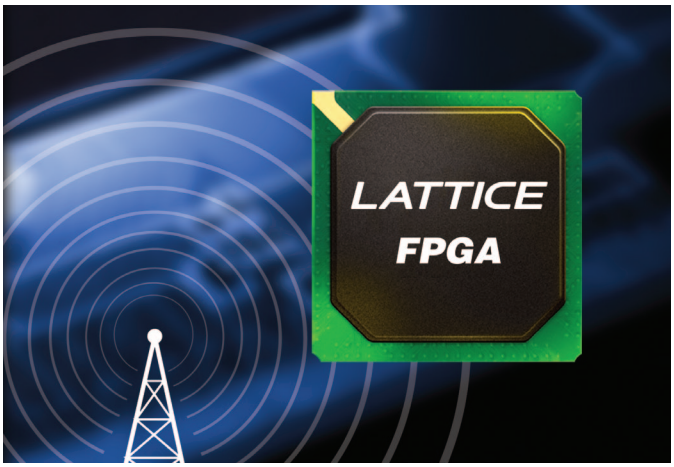
Lattice Wireless Solutions

Ready-to-Use Wireless Portfolio

Lattice provides designers with low-cost and low-power programmable solutions that are ready-to-use right out of the box. For wireless applications, a full suite of tested solutions are available that include:

- **FPGAs with Embedded SERDES Compliant to CPRI, Ethernet, Serial RapidIO 2.1, PCIe and JESD204A Standards**
- **FPGAs with I/O to Support High-Speed Parallel Interfaces Found on Data Conversion Devices**
- **FPGAs with Embedded, High Performance DSP Blocks**
- **A Portfolio of Soft IP Cores and Reference Designs**
- **Application Specific Development Boards and Demonstration Designs**
- **Test and Interoperability Reports for PMA, PCS and Generic I/O**

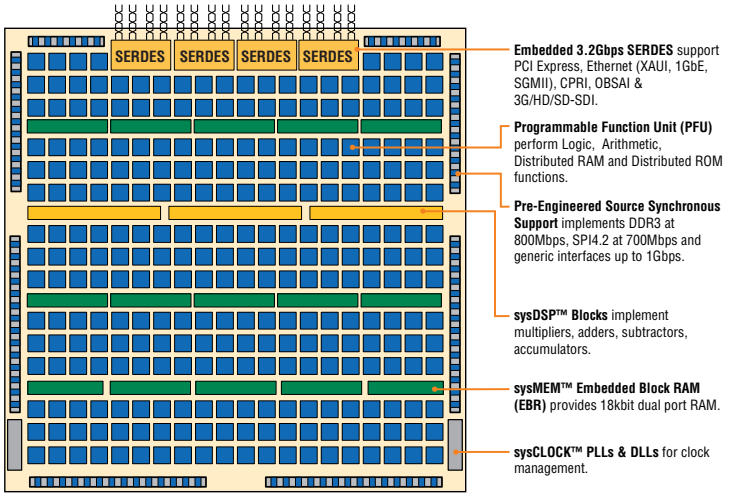


SILICON: INDUSTRY LEADING PROGRAMMABLE WIRELESS PLATFORM

LatticeECP3™ Features

- **Low-Cost Digital SERDES**
  - Ideal for low-cost chip-to-chip and small form-factor backplane applications
- **Up to 16 Channels per Device**
  - Supports CPRI, OBSAI, Serial RapidIO, JESD204A, PCI Express, Ethernet (GbE, XAUI, SGMII) and SMPTE
  - Complete End-to-End Solution
  - Soft IP implementations for connectivity and RF/BB processing applications
- **Very Low Power**
  - 110mW Per Channel (Typical @ 3.2Gbps)
- **Low-Power, High-Value FPGA Fabric**
  - High end features at low cost
  - Cascadable DSP with 54-bit ALU
- **Small Form Factor**
  - Small, low-cost 17x17mm wirebond packages

LatticeECP3 Block Diagram



LatticeECP3 Selector Guide

Parameter	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
EBR Block SRAM (K bits)	700	1327	4420	4420	6850
Distributed RAM (K bits)	36	68	145	188	303
18x18 Embedded Multipliers	24	64	128	128	320
3.2Gbps SERDES Channels	4	4	12	12	16
Number of PLLs/DLLs	2+2	4+2	10+2	10+2	10+2
Power Grades[1]	-S, -L	-S, -L	-S, -L	-S, -L	-S, -L
Speed Grades[2]	-6, -7, -8	-6, -7, -8, -9	-6, -7, -8, -9	-6, -7, -8, -9	-6, -7, -8, -9
Packages & SERDES / I/O Combinations					
328-ball csBGA (10 x 10 mm)	2/116				
256-ball ftBGA (17 x 17 mm)	4/133	4/133			
484-ball fpBGA (23 x 23 mm)	4/222	4/295	4/295	4/295	
672-ball fpBGA (27 x 27 mm)		4/310	8/380	8/380	8/380
1156-ball fpBGA (35 x 35 mm)			12/490	12/490	16/586

1. -S = Standard Power; -L = Low Power
2. -9 = High-Speed Device

Low Latency CPRI

- Supports the Physical Link Layer (Layer 1) and Data Link Layer (Layer 2) of the CPRI v4.0 Specification
- Supports the three Standard Bit Rates of the CPRI Specification and 3G (614.4 Mbps, 1228.8 Mbps, 2457.6 Mbps, 3072 Mbps)
- Supports 8b/10b Encoding/Decoding Performed in the PCS/SERDES
- Supports Code-violation Detection Performed in the PCS/SERDES
- Performs CPRI Hyperframe Framing
- Performs Synchronization and Timing as Defined in Section 4.2.8 of the CPRI Specification
- Supports low Latency Variation Requirements for Multi-hop Topologies
- Supports the L1 Inband Protocol
- Provides a Parallel Interface for Merging Vendor Specific Data into the CPRI Frame
- Provides a Start-up Sequence State Machine in Hardware for both REC and RE Nodes
- Performs Link Maintenance as Defined in Section 4.2.10 of the CPRI Specification - LOS Detection, LOF Detection, RAI Indication

Serial RapidIO 2.1

- Serial RapidIO 2.1 Endpoint Core for Processor Bridging, Control Plane Interfaces and Bridging to Legacy Interface Applications in a Small Footprint
- Allows for 1x, 2x, 4x Lane Configurations at up to 3.125Gbps per Lane
- Implements Physical Layer, Transport Layer, Maintenance Transaction Handling and Error Management Extensions.
- Provides Infrastructure Support for External Logical Layer Functions, Enabling Maximum Flexibility
- Provides a Choice of Logical Layer Functions that are Important for the Application
- Provides a Choice of how logic layer Functions Interact with the rest of the System - SOC Bus or Streaming Interfaces
- Supports Software Implementations of Control Plane Oriented Functions such as Doorbells and Messages
- Backward Compatible with the v1.3 Specification
- Demo platform and Interop and Throughput Documentation available

SGMII / Gigabit Ethernet

- Implements PCS Functions of the Cisco SGMII Specification, Revision 1.7
- Implements PCS Functions for IEEE 802.3z (1000BaseX)
- Dynamically Selects SGMII/1000BaseX PCS Operation
- Supports MAC or PHY Mode for SGMII Auto-negotiation
- Supports (G)MII data rates of 1Gbps, 100Mbps, 10Mbps
- Includes Easy Connect Option for Seamless Integration with Lattice's Tri-Speed MAC (TSMAC) IP Core

PCI Express Endpoint IP (x1, x4)

- 125 MHz User Interface
- Credit Interface for Transmit and Receive for PH, PD, NPH, NPD, CPLH, CPLD Credit Types
- Upstream/downstream, Single Function Endpoint Topology

High-Speed Data Conversion

- Support for High-Speed LVDS-based ADCs
- Support for High-Speed ADCs Utilizing the SERDES-based, JESD204A Specification
- Reference Designs and Evaluation Platforms Available for both LVDS-based and JESD204-based Applications

4G Multi-Channel DUC/DDC

- Compliant with the WiMAX transmit spectral mask
- Four complex (I and Q channels) DDC/DUC for sampling frequency of 89.6 MHz
- 18-bits data and coefficient widths, with pre-determined coefficient values
- Includes evaluation test bench and scripts for simulation and implementation
- Includes scripts to create IPs and simulation libraries
- Self-checking test bench with programs to generate golden output
- Verilog source code is provided to enable customization of the design

Block Viterbi Decoder

- Compatible with the Following Standards: IEEE 802.16-2004 SC PHY/ OFDM PHY, IEEEE802.11a, 3GPP, 3GPP2, and DVB-S
- Supports Multiple Code Rates
- Variable Constraint Length from 3 to 9
- Supports Dynamically Variable Code Rates and Puncture Patterns
- Dynamic BER Estimation Option

Dynamic Block Reed-Solomon Encoder

- 3- to 12-bit Symbol Width
- Configurable Field Polynomial
- Configurable Generator Polynomial: Starting Root and Root Spacing
- User-defined Codewords
- Selectable Following Communications Standards: OC-192, DVB, CCSDS, ATSC, and more

FFT/iFFT Compiler

- Wide Range of Points Sizes: 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384
- Choice of High-performance (Streaming I/O) and Low Resource (Burst I/O) Versions
- Run-time Variable FFT Point Size
- Forward, Inverse or Port-Configurable Forward/ Inverse Transform Modes

FIR Filter Generator

- Variable number of taps up to 2048
- Input and coefficients widths of 4 to 32 bits
- Multi-channel support for up to 256 channels
- Decimation and Interpolation ratios from 2 to 256
- Support for half-band filter
- Signed or unsigned data and coefficients
- Coefficients symmetry and negative symmetry optimization
- Re-loadable coefficients support
- Selectable output width, precision, overflow (wrap-around or saturation) and rounding

Distributed Arithmetic-FIR Filter Generator

- Variable number of taps up to 1024
- Multi-channel support (up to 32 channels)
- Polyphase interpolation/decimation filters
- Halfband filters
- Interpolation and Decimation ratios from 2 to 32
- Input data and coefficient widths from 4 to 32 bits
- Signed or unsigned data and coefficients
- Selectable output width, precision, overflow (wrap-around or saturation) and rounding
- Configurable pipelining to increase performance

CORDIC

- Supports Vector rotation (polar to rectangular), Vector translation (rectangular to polar), Sin and cos, Arctan
- Input data widths from 8 to 32 bits
- Configurable number of iterations used to derive output from 4 to 32
- Optional pre-rotation module
- Optional amplitude compensation scaling module to compensate for the CORDIC algorithm's output amplitude scale factor
- Selectable rounding
- Selectable word-serial architectural configuration for area optimization
- Signed 2's complement data

Cascaded Integrator-Comb (CIC) Filter

- 1-32-bit Input Data Width
- 1-8 Cascaded Stages
- 1-4 Cycles Differential Delay, Run-time Programmable for Both Decimation and Interpolation
- 2-16,384 Decimation and Interpolation Sampling Rate Factor, Run-time Programmable Rates for Both Decimationand Interpolation
- Multi-channel (up to 4 Channels) Support for Both Decimation and Interpolation
- Fully Synchronous, Single-clock Design

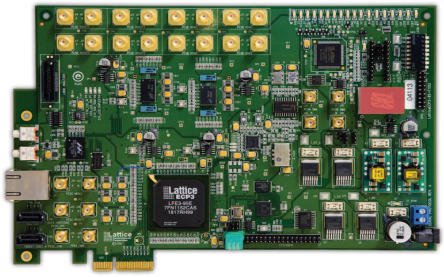
OBSAI (Reference Design)

- Supports the Physical Link Layer and the Data Link Layer of the OBSAI RP3-01 Specification
- Supports the three Standard Bit Rates of the OBSAI RP3 Specification (768 Mbps, 1536 Mbps, and 3072 Mbps)
- OBSAI Data Link Parameter Values Specified via Separate Dedicated I/O Allowing Hardwired Configuration or Register-based Programmable Control of Core Functionality. See the User's Guide for Parameter and Range Details
- GUI-selectable CDMA and WCMA, GSM/EDGE, 802.16 Evaluation Configurations

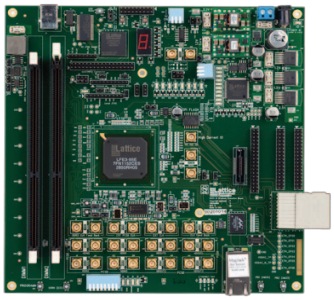
Lattice Wireless Evaluation Platforms

Platform	Board Name	Other Interfaces		
LatticeECP3	Serial Protocol Board	• SMAs for SERDES (4 channels) • RJ-45	• PCIe x4 Edge Finger • SMAs for LVDS I/O	• DDR3 Component (8 bit) • DDR2 Component (18 bit)
	I/O Protocol Board	• SMAs for SERDES (4 channels) • RJ-45	• SPI4.2 Connector • SMAs for LVDS I/O	• DDR3 Memory Dual DIMM (64 bit) • DDR2 Component (18 bit)
	AMC Card	• VITA 57 Connector for FMC • RJ-45 Interface for GMII/RGMII	• SFP Cage for SGMII Support • SERDES Backplane (FatPipes, 8 Channels)	• SERDES via FMC (FatPipe, 4 Channels) • Front Panel USB Port

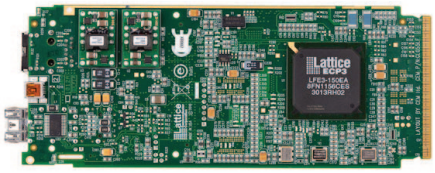
LatticeECP3 Serial Protocol Board



LatticeECP3 I/O Protocol Board



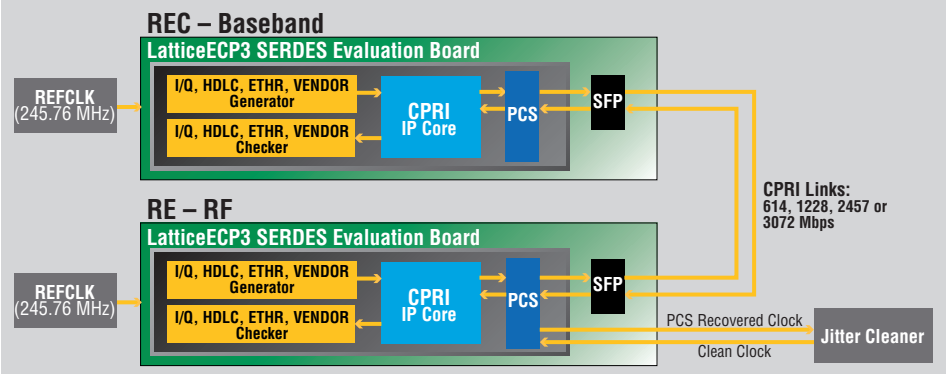
LatticeECP3 AMC Card



CPRI REC-to-RE and REC Standalone Loopback Demos

The LatticeECP3 CPRI demo demonstrates the performance of the LatticeECP3 PCS with the CPRI IP core at 1.228/2.457/3.072 Gbps. The CPRI Demo Design is a single-channel CPRI core with data generator/checker. The PCS serializes the data in the transmit direction, and de-serializes it in the receive direction.

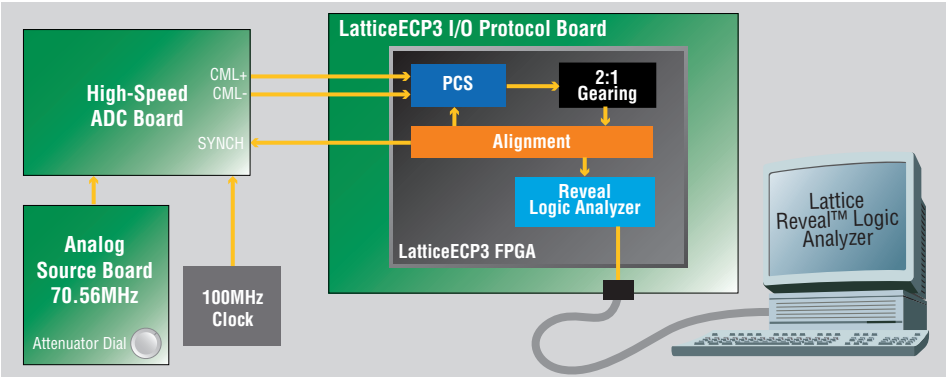
CPRI REC-TO-RE DEMO – FULL SYSTEM EMULATION



JESD204A ADC Reference Design

The LatticeECP3 provides seamless support for the JESD204A specification as it relates to high-speed Analog-to-Digital Converters (ADCs). Lattice has partnered with NXP to provide a reference design using the low-cost LatticeECP3 FPGA and a LatticeECP3 I/O Protocol board. This provides designers an ideal platform for a low-cost, low power and small footprint solution for FPGA-based serial data acquisition and processing.

JESD204A ADC REFERENCE DESIGN BLOCK DIAGRAM



Lattice IPexpress™ Tool

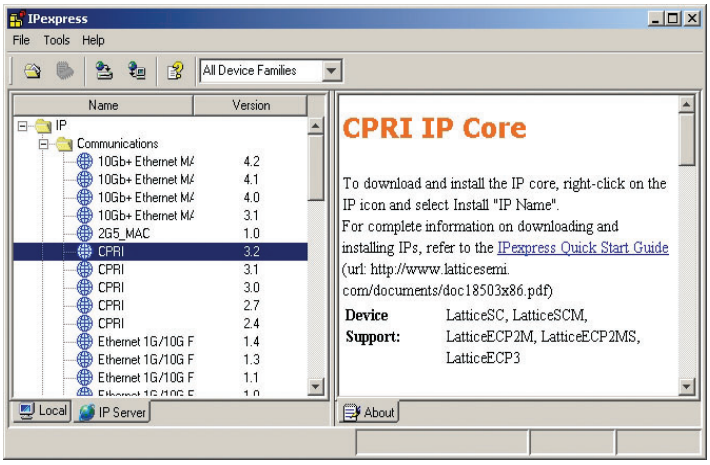
IPexpress, a key element of the Lattice Diamond® design environment, revolutionizes and simplifies IP design. The IPexpress design flow enables users to fully parameterize IP in real-time. The designer can then instantiate the user-configured IP and complete the design process, including full timing simulation and bitstream generation.

VIEW IP CORES AVAILABLE FOR DOWNLOAD

From the Lattice IP Server Tab within IPexpress, you can view available LatticeCORE™ user-configurable IP cores for download.

INSTALL OR DOWNLOAD IP CORES

You can download and install LatticeCORE user-configurable IP cores on your computer, or you can simply download them and install them later.



Easily configure a growing selection of IP cores with Lattice's IPexpress tool.

WIRELESS IP PORTFOLIO

Function	IP and Reference Designs for LatticeECP3 and ECP2M FPGAs
Serial Baseband Interconnect	• Low Latency CPRI IP Core for Baseband Data Transport • RP3-01 OBSAI IP Core for Baseband Data Transport • SRIO Endpoint Core (x1, x2, x4) • SGMII / Gigabit Ethernet • PCI Express Endpoint (x1, x4)
Data Conversion	• JESD204A IP Core • ADC Interface Reference Design
Signal Processing	• Multi-channel, Multi-mode Digital Up/Down Conversion (DUC, DDC) for WCDMA, LTE and WiMAX • Digital Pre-Distortion and Crest Factor Reduction IP Cores • Block Viterbi Decoder IP Core • Dynamic Block Reed-Solomon Encoder IP Core • FFT Compiler IP Core • Numerically Controlled Oscillator IP Core • FIR Filter Generator IP Core • 3GPP-LTE CTC Decoder and WiMAX 802.16 CTC Decoder IP Cores from TurboConcept
DSP Building Blocks	Lattice, and our LatticeCORE Connections Partners, offer a wide range of DSP IP cores and reference designs. Go to www.latticesemi.com for a complete list.
Embedded Processors	• LatticeMico8 open source microcontroller • LatticeMico32 open source microprocessor

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August 2012
Order #: I0197C