Lattice Semiconductor Corporation

Power Estimation in ispMACH 4000ZE Devices

August 2008 **Technical Note TN1187**

Introduction

The ispMACH® 4000ZE family offers an ideal mix of both high speed and low power in the same device. With an advanced low-power electrically erasable non-volatile memory cell and a full CMOS logic design approach, the ispMACH 4000ZE family offers fast pin-to-pin propagation delays for designs requiring high speed, while consuming only microamps of static current. The low standby and dynamic power of the ispMACH 4000 family is achieved without the need for any "turbo bits" or other power management schemes associated with traditional low power CPLD approaches.

1.8V Core E^2CMOS® Technology

The ispMACH 4000ZE devices have an internal core voltage of 1.8V. Because device I_{CC} is proportional to capacitance and switching voltage, the lower 1.8V core voltage helps reduce dynamic power consumption.

Special Standby I_{CC} Considerations

The Standby I_{CC} component given in the ispMACH 4000ZE Family Data Sheet does not include any current due to bus maintenance options such as Pull-up, Pull-down or Bus Hold, and does not allow for any application-specific DC I/O loads. A designer interested in the lowest possible standby I_{CC} must evaluate which bus maintenance option is appropriate, taking into consideration which device outputs need to be enabled during Standby. For example, if the designer selects pull-up for bus maintenance, each steady-state active low output will add an I_{PU} load to the standby I_{CC} given in the ispMACH 4000ZE Family Data Sheet. If bus maintenance is not required, designers must avoid floating inputs.

Lattice recommends that all inputs and I/Os be driven or pulled to either ground or V_{CCO} at all times. This recommendation includes unused inputs and I/O pins. Without bus maintenance, the lowest standby current is achieved when inputs are at ground.

Lattice recommends a pull-down resistor for TCK, one per chain, placed near the programming header and after each driver output used to buffer TCK, if buffers are used.

Power Estimation

This section describes how to estimate the power consumption of the ispMACH 4000ZE devices. It is recommended to confirm these estimates with the actual design under the intended operating conditions. Power consumption in the ispMACH 4000ZE devices depends on three primary factors:

1. Operating clock frequency
2. Operating voltage
3. Power dissipated by the I/O drive current

The total current consumption for the ispMACH 4000ZE can be estimated using the following equation:

$$I_{CC} = A + B * N * f_{MAX} * AF + I_{CCO} + I_{CCOSC} \quad (1)$$

- I_{CC} = Current consumed by the ispMACH 4000ZE (mA)
- A = Static component, given in the ispMACH 4000ZE Family Data Sheet (mA)
- B = Macrocell Power Coefficient, given in the device data sheet (mA/MHz)
- N = Number of macrocells in the design (see report file)

- f_{MAX} = Maximum Operating clock frequency (MHz)
- AF = Activity Factor of the nodes in the design
- I_{CCO} = Current attributable to output pins (mA). Only a small percentage of I_{CCO} power is dissipated internal to the device.
- I_{CCOSC} = Operating supply current of the internal oscillator when enabled

Power estimation coefficients A, B and Iccosc are given in the ispMACH 4000ZE Family Data Sheet along with the typical I_{CC} vs. frequency plots.

I_{CCO} Calculation

Each active output pin will add current draw to the system. The sum of the current used by the I/O pins depends on the operating voltage, capacitance, output voltage swing, number of output pins and the average output frequency. The variable *m* in Equation 2 is the number of outputs in the design. V_{OH} and V_{OL} can be found in the ispMACH 4000ZE Family Data Sheet in the corresponding device section.

$$I_{CCO} = \sum_{n=1}^{m} C_n * (V_{OH} - V_{OL}) * F_n \tag{2}$$

- I_{CCO} = Current attributable to output pins (mA)
- F_n = Output Frequency of output n (MHz)
- C_n = Sum of Capacitive loading of output n (nF). When the output pin is connected to a CMOS input, typical load is 0.005 to 0.010 nF. (Note: the units nF are used to make the final I_{CC} units be mA).
- V_{OH} = Output voltage high of the output (V)
- m = number of outputs

Activity Factor Calculation

The Activity Factor relates to how often a register transitions. Each transition of a register adds to the current consumption of a device. The average of all the registers Activity Factors will give you the device AF. Take for example a 16-bit counter, the LSB node of a 16-bit counter is switching every clock rising edge, its Activity Factor is 1. The second node is switching every other clock rising edge that corresponds to an Activity Factor of 1/2. The third node is switching every fourth clock rising edge for an Activity Factor of 1/4. The series for the sequence of 16 nodes is 1 + 1/2 + 1/4 + 1/8 + 1/16 + ... + 1/215 converges to 2. Assuming a sum of 2 for the counter, divide by the total number of nodes (16) to measure the average AF per counter of 2/16 = 0.125.

Power Guard disconnects the CPLD array logic from external input signal changes. In other words, a toggling I/O pin will not cause any internal dynamic power consumption. This results in the Activity Factor of 0 when the Power Guard is enabled.

Power Saving Design Practices

To take advantage of the ispMACH4000ZE low power, designers should follow the following techniques:

- Where possible, reduce clock speeds and limiting the bus loadings.
- Use Power Guard to selectively power down portions of the design.
- Fast slew mode that switches between states at the fastest rate and uses less power.
- Ensure inputs are properly terminated. If they are not, inputs can use an inordinate amount of power as the signal moves between high and low logic levels. Programmable termination options include the following four settings: bus-keeper latch, pull-up, pull-down or no termination.

Estimated Power Consumption Example Calculation

The following is an example calculation of the current consumption of an ispMACH 4032ZE device. The Power Consumption section of the ispMACH 4000ZE Family Data Sheet shows graphs that reflect the relationship between I_{CC} and operating frequency for the ispMACH 4000ZE at typical operating voltage and room temperature. The pattern used in the device to generate the graphs is a 16-bit up-down counter, with an Activity Factor equal to 0.125, clocking every macrocell at frequency. The graphs provided only show the core current consumption and do not include the current required for output switching. Additional current drawn by the switching of the output pins needs to be added by calculating $I_{CCO.}$

For this example, the ispMACH 4032ZE is used with two 16-bit counters. As described above, a single 16-bit counter has an Activity Factor which series sums to a value approximating 2. Summing the two counters' Activity Factors results in a value of ~4 (i.e. 2 + 2). Dividing the accumulated register activity factors by the total number of registers results in 4/32 or ~0.125. From the ispMACH 4000ZE Family Data Sheet, the power estimation coefficients for A and B are 0.009mA and 0.010mA/MHz for the ispMACH 4032ZE. The onboard oscillator is disabled I_{CCOSC} = 0mA. Calculate the core I_{CC} for an ispMACH 4032ZE clocked at 150MHz (not including the I_{CCO} factor as shown in Equation 1) as follows:

$$\text{Core } I_{CC} = A + B * N * f_{MAX} * AF + I_{CCOSC} \tag{3}$$

- Core I_{CC} = Core current (no outputs) consumed by the ispMACH 4032ZE (mA)
- A = 0.010 (mA)
- B = 0.009 (mA/MHz)
- N = 32 Macrocells
- f_{MAX} = 150 (MHz)
- AF = 0.125
- I_{CCOSC} = 0 (mA)

$$\text{Core } I_{CC} = 0.010 \text{ mA} + 0.009 \text{ mA/MHz} * 32 * 150 \text{ MHz} * 0.125 + 0 = 5.41 \text{ mA}$$

Now add the current drawn from each output. If the least significant four bits are routed from each counter to pins on the ispMACH 4032ZE, four frequency components would need to be used to calculate I_{CCO}. For the four least significant bits, an output would switch at 150 MHz, 75 MHz, 37.5 MHz and 18.75 MHz. Assume that each output drives a single LVCMOS load of 10pF with the exception of the two least significant bits of each counter, which will be 20 pF. The following shows the I_{CCO} calculation for a V_{CCO} of 1.8V:

$$I_{CCO} = \sum_{n=1}^{m} C_n * (V_{OH} - V_{OL}) * F_n \tag{4}$$

- I_{CCO} = Total current attributable to output pins (mA).
- F_n => F_1 = 150 MHz, F_2 = 75 MHz, F_3 = 37.5 MHz, F_4 = 18.75 MHz, F_5 = 150 MHz, F_6 = 75 MHz, F_7 = 37.5 MHz, F_8 = 18.75 MHz
- Cn = 0.01 (nF) Assume worst case typical capacitance for all output pins accept the 150 MHz pins which will be 0.02 (nF) for this example
- $V_{OH} = V_{CCO}$ - 0.4 = 1.6 (V)
- V_{OL} = 0.2 (V)
- m = 8

$$I_{CCO} = \sum_{n=1}^{m} [(0.02\text{ nF} * 1.4\text{ V} * 150\text{ MHz}) + (0.01\text{ nF} * 1.4\text{ V} * 75\text{ MHz}) + (0.01\text{ nF} * 1.4\text{ V} * 37.5\text{ MHz}) + (0.01\text{ nF} * 1.4\text{ V} * 18.75\text{ MHz}) + (0.02\text{ nF} * 1.4\text{ V} * 150\text{ MHz}) + (0.01\text{ nF} * 1.4\text{ V} * 75\text{ MHz}) + (0.01\text{ nF} * 1.4\text{ V} * 37.5\text{ MHz}) + (0.01\text{ nF} * 1.4\text{ V} * 18.75\text{ MHz})]$$

$$\begin{aligned} I_{CCO} &= 0.01\text{ nF} * 1.4\text{ V} * (75 + 37.5 + 18.75 + 75 + 37.5 + 18.75)\text{ MHz} + 0.02\text{ nF} * 1.4\text{V} * (150 + 150)\text{ MHz} \\ &= 3.675\text{mA} + 8.4\text{mA} \\ &= 12.075\text{ mA} \end{aligned}$$

To calculate the overall current consumption of the device, add the Core I_{CC} to I_{CCO} to get the final power estimation for the device and pattern being used at 150 MHz is:

$$I_{CC} = \text{Core } I_{CC} + I_{CCO} = 5.41\text{ mA} + 12.075\text{ mA} = 17.485\text{ mA}$$

Technical Support Assistance

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Revision History

Date	Version	Change Summary
August 2008	01.0	Initial release.