Interfacing ispClock5600A with Reference Clock Oscillators

August 2008 Application Note AN6079

Introduction

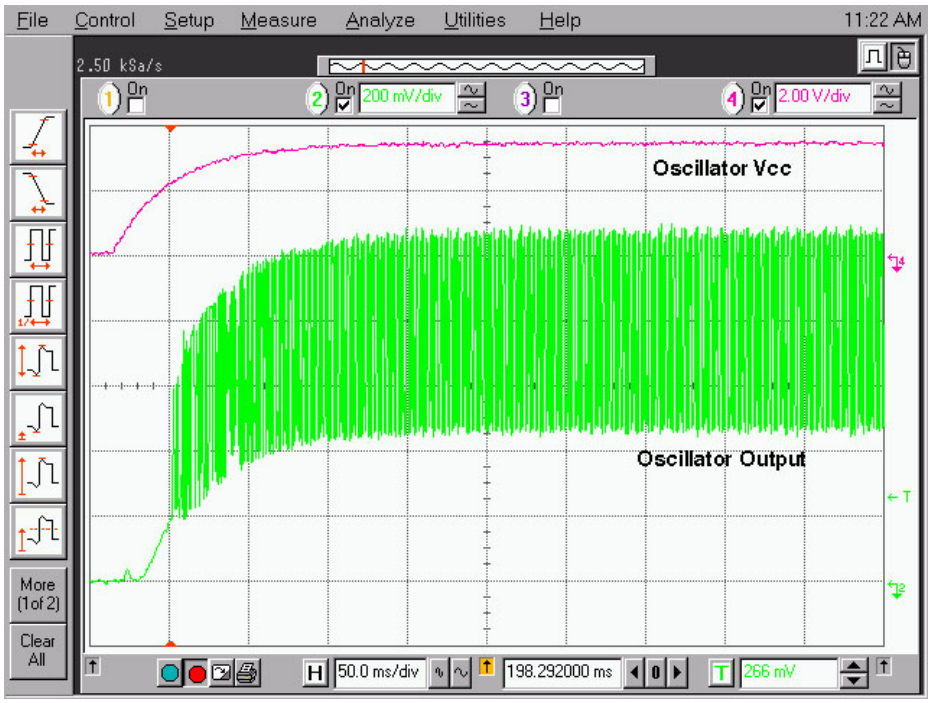
Lattice ispClock™5620A and ispClock5610A are in-system programmable zero delay clock generator ICs with integrated universal fan-out buffers. In some applications these devices are required to generate multiple clock output frequencies from a single reference oscillator clock source.

The input to output clock phase relation is guaranteed only when the reference clock high pulse width or low pulse width are greater than the data sheet $t_{CLOCKHI}$ and $t_{CLOCKLOW}$ specifications. If either specification is violated the input to output clock phase relationship can be restored by activation of the RESET pin of the ispClock 5600A device. This application note examines two common conditions when the reference oscillator clock could violate the $t_{CLOCKHI}$ or $t_{CLOCKLOW}$ specifications and warrant the activation of the RESET pin.

Powering Up Reference Oscillator After ispClock5600A

Figure 1 details the start-up behavior of a typical oscillator module. Note that for the first 50ms the output is active, the amplitude and offset are ramping up. It is during this time that the ispClock may see a very narrow clock pulse because the thresholds at the ispClock inputs are fixed but the oscillator output is changing. In this case the RESET pin of the ispClock should be activated after the oscillator output is stable.

Figure 1. Powering Up a Reference Oscillator



Oscillator Enabled Asynchronously

Figure 2 shows the general behavior of a typical oscillator module when the output enable pin is controlled by an asynchronous enable signal. The output is held low when the enable pin is low and oscillates when the enable pin goes high. Figure 3 zooms in on the initial output transitions and reveals two short pulses that would result in a timing violation for the reference clock input of the ispClock.

Figure 2. CMOS Oscillator Enabled

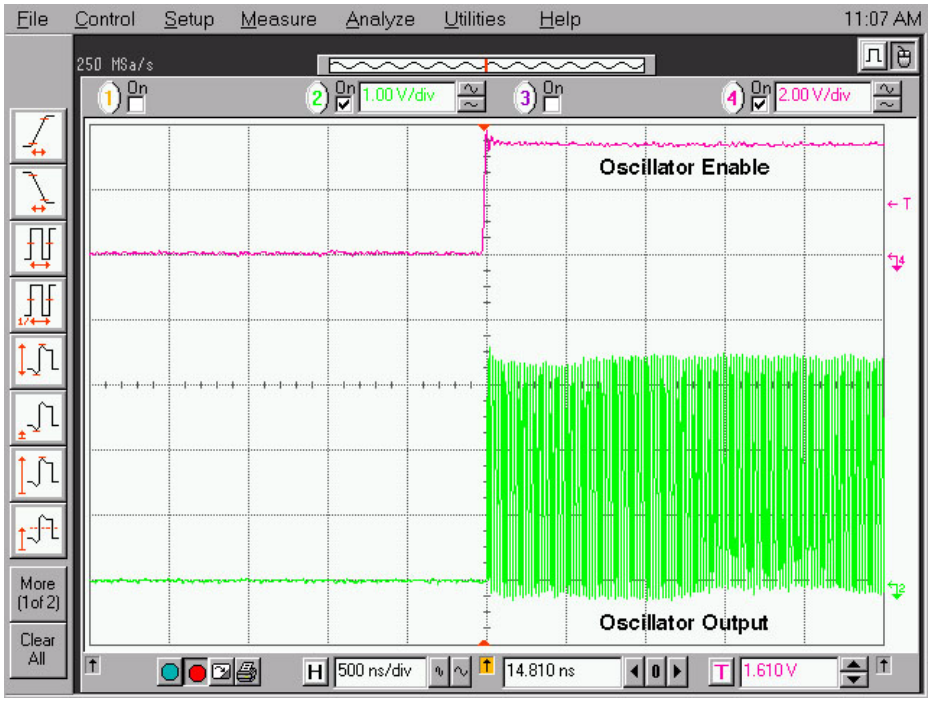


Figure 3. Initial Transitions of Enabled Oscillator

In this case where the reference oscillator is gated on, either by the output enable pin of the oscillator or by other means of asynchronous enable, the RESET pin should be activated after the reference has been enabled and the clock input to the ispClock is stable.

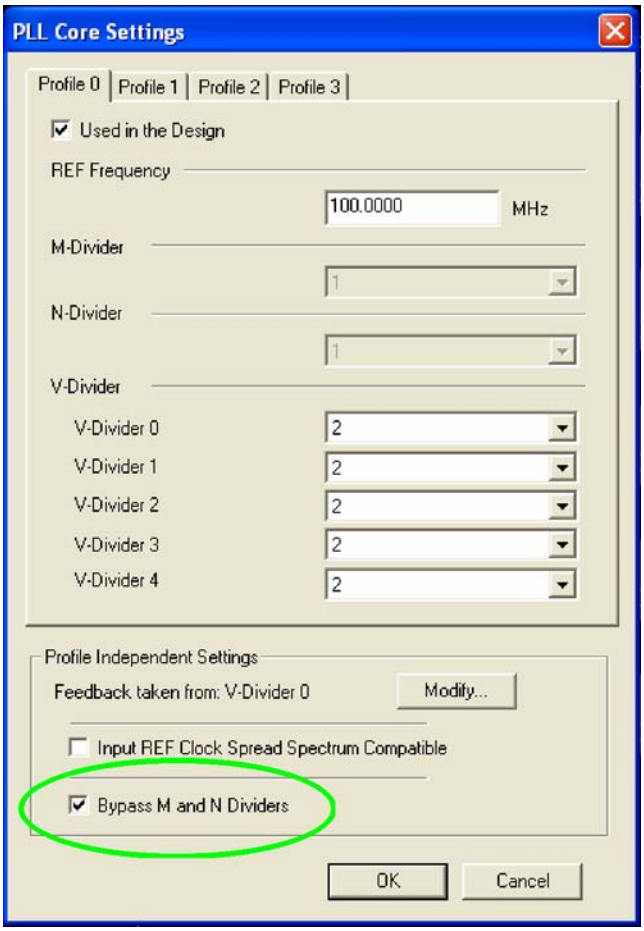
Reference and Feedback MUXes

The ispClock5620A has an input MUX for both the clock reference and the feedback inputs to the phase detect circuitry. If the select line for either MUX is asynchronously changed then it may result in a timing violation similar to the waveforms shown in Figure 3. This also can result in an output phase relationship that would require the activation of the RESET pin to correct.

M and N Divider Bypass

Bypassing the M and N dividers will allow the ispClock device to accept clock pulses that are much shorter than the $t_{CLOCKHI}$ or $t_{CLOCKLOW}$ specifications without resulting in unpredictable input to output phase relationships. The M and N dividers can be placed in bypass mode by checking the box in the PLL Core Settings dialog box of PAC-Designer, which is shown in Figure 4. Placing M and N into bypass mode results in a divider value of unity for both M and N resulting in reduced frequency synthesis options.

Figure 4. Bypassing M and N Dividers in PAC-Designer



Summary

Activate the RESET pin after the reference clock is stable to prevent out of phase issues with the ispClock. When Possible, M and N dividers can be bypassed to prevent out of phase issues.

Related Literature

- ispClock5600A Family Data Sheet

Technical Support Assistance

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Revision History

Date	Version	Change Summary
August 2008	01.0	Initial release.