LatticeECP2M™ PCI Express x4 Evaluation Board – Revision B

User's Guide

January 2009
Revision: EB34_01.2

Introduction

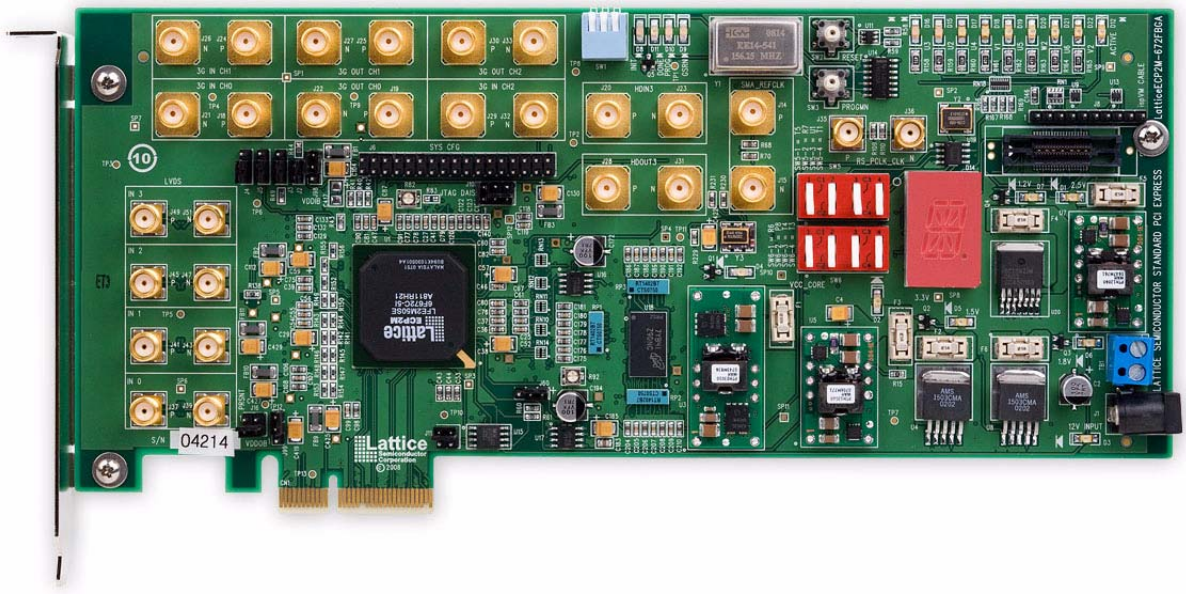
This user's guide describes the LatticeECP2M PCI Express x4 Evaluation Board Revision B featuring the LatticeECP2M FPGA device. The evaluation board has been designed to support the LatticeECP2M35 device and the LatticeECP2M50 device. Different versions of the evaluation board are available that contain either the LatticeECP2M35 device or the LatticeECP2M50 device. The stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces to PCI Express protocols and SERDES bridge interfaces using SMA interconnections.

The evaluation board includes provisioning to connect high-speed SERDES channels via SMA connectors to test and measurement equipment. Please note that boards populated with the LatticeECP2M-35 device have all available SERDES channels routed to the PCI Express, and in this case the SMAs are not active. The SMAs are available in larger density LatticeECP2M FPGAs fitting the same footprint, but with additional SERDES channels. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

The board has several debugging and analyzing features for complete user evaluation of the LatticeECP2M device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP2M FPGA.

This document describes boards marked with "Rev B" on the PCB silkscreen, next to the Lattice logo. For boards marked "Rev A", refer to the LatticeECP2M PCI Express x4 Evaluation Board - Revision A User's Guide.

Figure 1. LatticeECP2M PCI Express x4 Evaluation Board - Revision B



Board Features

- SERDES interface to x4 PCI Express edge fingers
- DDR2 memory device
- SERDES high-speed interface SMA test points (active with LatticeECP2M-50 and larger FPGAs only) and clock connections
- Power connections and power sources
- ispVM® programming support

- On-board and external reference clock sources
- Interchangeable clock oscillators
- ORCAstra demonstration software interface via standard ispVM JTAG connection
- Various high-speed layout structures
- User defined input and output points
- SMA connectors included (10) for high-speed clock or data interfacing
- Performance monitoring via test headers, LEDs and switches

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 1 shows the functional partitioning of the board.

Figure 2. LatticeECP2M PCI Express x4 Evaluation Board Revision B

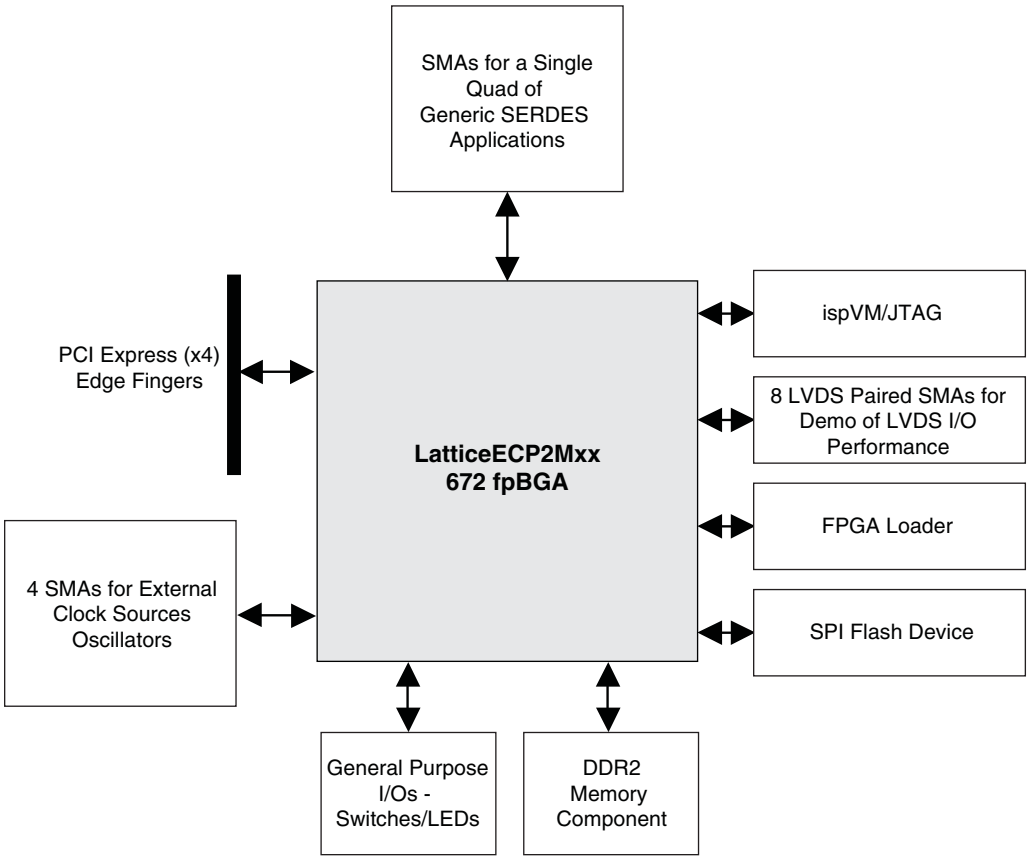
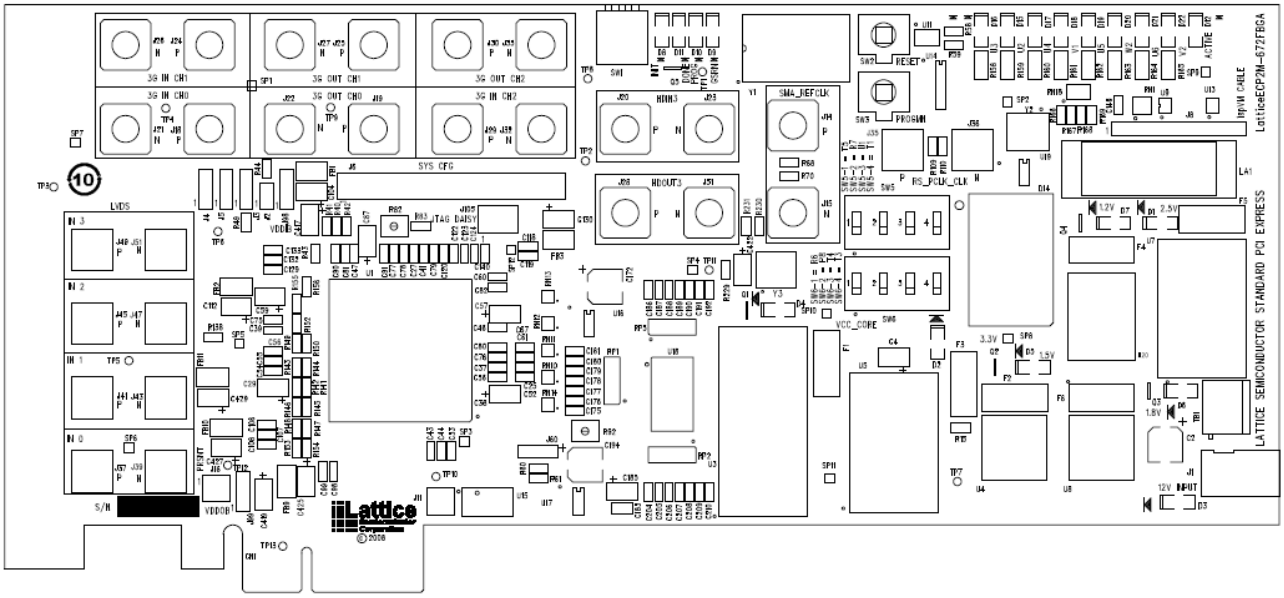


Figure 3. LatticeECP2M PCI Express x4 Evaluation Board Revision B, Top View



Additional Resources

For additional information and resources related to this board, including updated documentation and software demos, please see the Lattice web site at: www.latticesemi.com/boards, and navigate to the appropriate page for this board.

Lattice makes its best effort to provide evaluation board designs to help users with evaluation and development. However it remains the user's responsibility to verify proper and reliable operation of Lattice products in their end application by consulting documentation provided by Lattice. Differences in component selection and/or PCB layout in the user's application may significantly affect circuit performance and reliability.

LatticeECP2M Device

This board features a LatticeECP2M FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP2M devices in the 672-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP2M Family Data Sheet on the Lattice web site at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFE2M35E-FF672 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeECP2M PCI Express x4 Evaluation Board is ready to power on. The board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a bench top supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J1 and plug the wall transformer into an AC wall outlet.

Power Supplies

(see Appendix A, Figure 7)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided for use with a bench top supply adjusted to provide a nominal 12V DC.

All input power sources and on-board power supplies are fused with surface mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 1. Board Power Supply Fuses (see Appendix A, Figure 6)

F1	1.2V Core Fuse
F2	1.5V Fuse
F3	3.3V Fuse
F4	1.2V Fuse
F5	2.5V Fuse
F6	1.8V Fuse

Table 2. Board Power Supply Indicators (see Appendix A, Figure 6)

D1	2.5V Source Good Indicator
D2	3.3V Source Good Indicator
D3	12V Input Good Indicator
D4	1.2V VCC Core Source Good Indicator
D5	1.5V Source Good Indicator
D6	1.8V Source Good Indicator
D7	1.2V Source Good Indicator

External power can be alternatively connected rather than the wall transformer power pack.

Table 3. Board Supply Disconnects (see Appendix A, Figure 6)

TB1	Screw Terminal for 12V DC Pin1 (Square PCB Pad) -> +12V DC Pin2 -> Ground

PCI Express Power Interface

Power can be sourced to the board via the PCB edge finger (CN1). This interface allows the user to provide power from a PCI Express host board.

Programming/FPGA Configuration

(see Appendix A, Figure 8)

A programming header is provided on the evaluation board, providing access to the LatticeECP2M JTAG port.

ispVM Download Interface

J8 is an 10-pin JTAG connector, providing access to the LatticeECP2M JTAG port. It can be used in conjunction with the ispVM System software and Lattice USB download cable to program and control the device.

Table 4. ispVM JTAG Connector (see Appendix A, Figure 8)

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN
Pin 5	NC
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE
Pin 10	INITN

Download Procedures

Requirements:

- PC with ispVM System v.16.1.2 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). The latest ispVM System software can be downloaded from the Lattice web site at www.latticesemi.com/ispvm.

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (HW-DLN-3C, HW-USBN-2A, or equivalent)

JTAG Download

The LatticeECP2M device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

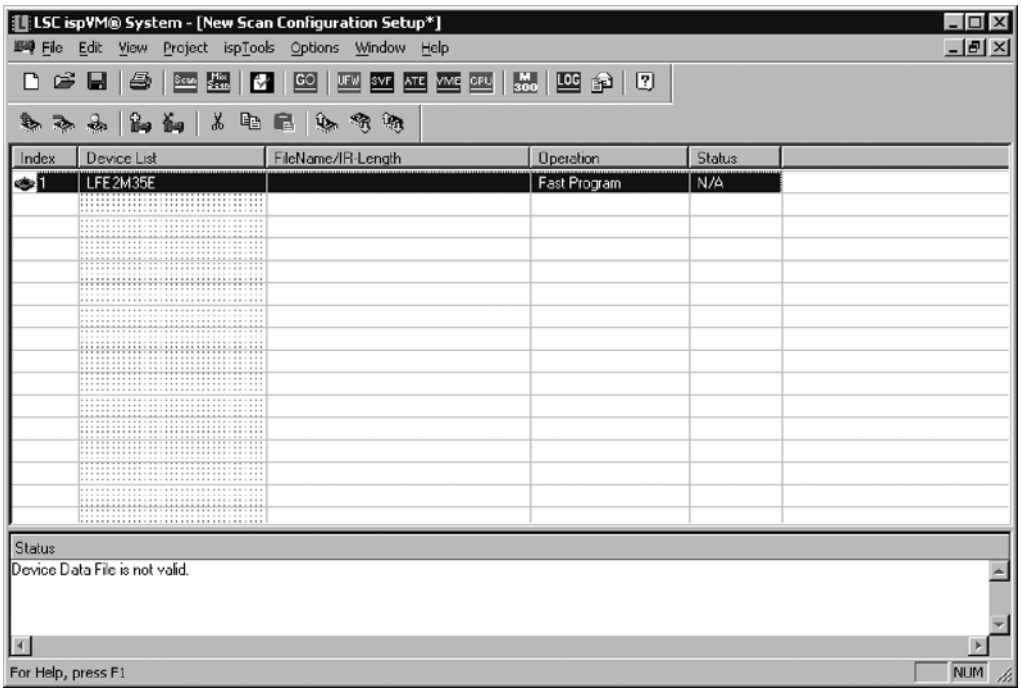
1. Connect the ispDOWNLOAD Cable to the appropriate header. J8 is used for the 1x10 cable.

   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2M FPGA device and render the board inoperable.*

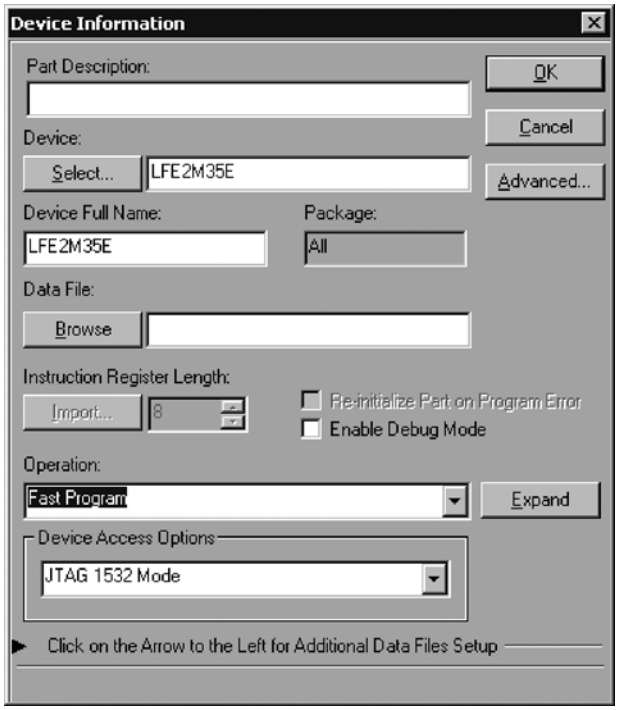
2. Connect the LatticeECP2M Evaluation Board to the appropriate power sources and power up board.

3. Start the ispVM System software.

4. Press the **SCAN** button located in the toolbar. The LatticeECP2M device should be automatically detected.



5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.



6. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Configuration Status Indicators
(see Appendix A, Figure 8)

These LEDs indicate the status of configuration to the FPGA.

- D8 (RED) illuminated, this indicates that the programming was aborted or reinitialized driving the INITN output low.
- D11 (GREEN) is illuminated, this indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D12 (GREEN) will flash indicating TDI activity.
- D10 (RED) illuminated, this indicates that PROGRAMN is low.
- D9 (RED) illuminated, this indicates that GSRN is low.

PROGRAMN and GSRN
(see Appendix A, Figure 8)

These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and GSRN (SW2). Depressing the button drives a logic level "0" to the device.

CFG [2:0]
(see Appendix A, Figure 8)

The FPGA CFG pins are set on the board for a particular programming mode via the SW1 DIP switch. JTAG programming is independent of the MODE pins and is always available to the user

On-Board Flash Memory
(see Appendix A, Figure 8)

Two memory devices (U12 and U15) are on-board for non-volatile configuration memory storage. These two devices occupy the same Flash slot on the board. U15 is populated with an 8M or smaller 8-pin SOIC device. U12 is a 16-pin TSSOP 64M Flash device. J11 is used to control the selection of the Flash memory to be accessed. A jumper can select whether U12 or U15 is accessed by the configuration memory. Placing a jumper between pins 1 and 2 on J11 will select U12(64M Flash). Placing a jumper between pins 3 and 4 will select U15 is a 8M device.

FPGA Clock Management

(see Appendix A, Figure 12)

The evaluation board includes various features for generating and managing on-board clocks. The clocks are generated from either input provided from SMAs (see table below) or from crystal oscillators (Y1, Y2 and Y3). Y1 is socketed for interchangeability and Y2 is a 100MHz surface-mounted oscillator which is fanned out around U1 for reference clocks with a fan-out buffer IC. Y3 is a 312.5MHZ clock oscillator that is connected to the SERDES reference clock input. SMA J14 and J15 can be used as an alternative input to the SERDES clock inputs for the L_REFCLK. This is discussed in the following section.

Y1 can be a 4-pin DIP type oscillator like the Connor-infield XO-400 series.

SERDES

(see Appendix A, Figure 9)

SERDES Reference Clock

The 50-ohm terminated SMA J14 and J15 connectors are provided to supply reference clocks directly to the LatticeECP2M device. This drives clocks to both SERDES quads via 100-ohm LVDS signaling. On-board clock oscillators mentioned in the previous sections can be chosen to drive the same SERDES reference clocks. There

are several board connections that can be altered by adding and removing shunt resistors. Adding shunts to R79 and R80 will connect the output of Y3 oscillator. Shunts R67 and R69 will connect the SMAs to the REFCLK inputs. The board can also be provisioned to source the clock from the PCI Express edge fingers directly to the SERDES REFCLK pins.

SERDES Channels

(see Appendix A, Figure 9)

DC coupled top-mounted SMA connectors connect to the three SERDES Tx and Rx channels of the L-Quad SERDES. These pins are directly coupled to the designated SMA connector creating a path for both input and output differential data.

Table 5. SERDES Connectors (see Appendix A, Figure 9)

SMA	Channel Name
J18	L_HDINP0
J20	L_HDINP3
J22	L_HDOUTN0
J24	L_HDINP1
J26	L_HDINN1
J28	L_HDOUTP3
J30	L_HDOUTP2
J32	L_HDINN2

SMA	Channel Name
J19	L_HDOUTP0
J21	L_HDINN0
J23	L_HDINN3
J25	L_HDOUTP1
J27	L_HDOUTN1
J29	L_HDINP2
J31	L_HDOUTN3
J33	L_HDOUTN2

SERDES PCI Express Channels

(see Appendix A, Figure 9)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge fingers (CN1) to fit directly into an x4 host receptacle. Power can be supplied directly from the PCI Express host via the edge finger connections.

FPGA Test Pins

(see Appendix A, Figure 14)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to switches and LEDS designated according to Table 6.

Table 6. FPGA Test Pins (see Appendix A, Figure 11)

Switch	BGA	Netname
SW6D	T30	Switch1
SW6C	T4	Switch2
SW6B	P8	Switch3
SW6A	R6	Switch4
SW5D	T1	Switch5
SW5C	U1	Switch6
SW5B	R7	Switch7
SW5A	T5	Switch8

LED	BGA	NetName
D16	U3	RED1
D17	U4	YELLOW1
D19	U5	GREEN1
D21	U6	BLUE1
D15	U2	RED2
D18	V1	YELLOW2
D20	W2	GREEN2
D22	V2	BLUE2

Note: LEDs will illuminate if connected to an unprogrammed FPGA pin. It is recommended that a pull-down be programmed on FPGA output pins.

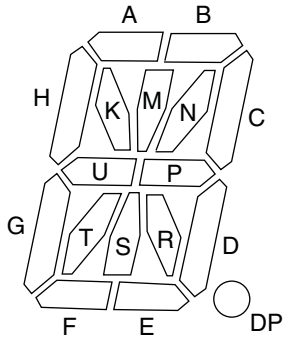
17-Segment LED Display

(see Appendix A, Figure 14)

General-purpose FPGA pins are connected to a 17-segment display according to the following table. These pins can be driven low to illuminate the display segments.

Figure 4. 17-Segment LED Display

Segment	BGA
A	H2
B	J3
C	G1
D	H3
E	J7
F	H5
G	G5
H	G6
K	F3
M	J8
N	E1
P	J9
R	E3
S	F5
T	D3
U	F6
DP	C2



Test SMA Connections

General-purpose FPGA pins are available via SMA test connections. These connections are designed to permit the evaluation of several types of FPGA I/O buffers. The use of several termination schemes permits an easy interface for each buffer type.

Table 7. FPGA I/O Test SMA Connectors (see Appendix A, Figure 13)

SMA Designation	Name	LFE2M35E Signal	672-BGA	Termination Description	Termination Resistor(s)
J37	LVDS_INP0	PR37A	N23	100-ohm Differential	R130
J39	LVDS_INN0	PR37B	M21		
	LVDS_INP1	PR41A	P24	100-ohm Differential	R132
	LVDS_INN1	PR41B	P23		
J45	LVDS_INP2	PR51A	T24	100-ohm Differential	R134
J47	LVDS_INN2	PR51B	U24		
J49*	LVDS_INP3	PR57A	V24	100-ohm Differential	R136
J51*	LVDS_INN3	PR57B	W24		
J38	LVDS_OUTP0	PR50A	T23	100-ohm Differential	R131
J40	LVDS_OUTN0	PR50B	T22		
J42	LVDS_OUTP1	PR53A	V26	100-ohm Differential	R133
J44	LVDS_OUTN1	PR53B	V25		
J46	LVDS_OUTP2	PR55A	W26	100-ohm Differential	R135
J48	LVDS_OUTN2	PR55B	W25		

Table 7. FPGA I/O Test SMA Connectors (see Appendix A, Figure 13) (Continued)

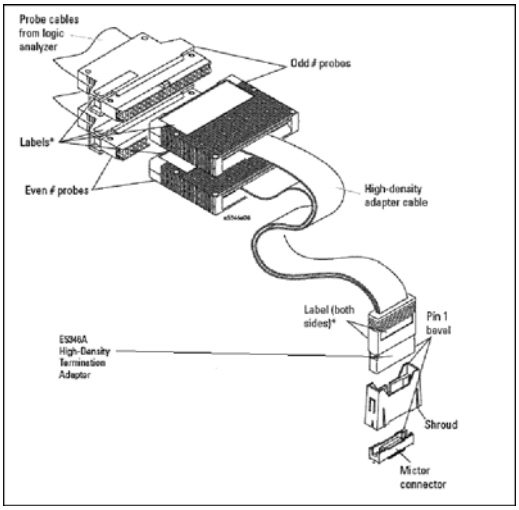
SMA Designation	Name	LFE2M35E Signal	672-BGA	Termination Description	Termination Resistor(s)
J50	LVDS_OUTP3	PR59A	Y26	100-ohm Differential	R137
J52	LVDS_OUTN3	PR59A	AA26		

Logic Analyzer Probe
(see Appendix A, Figure 10, LA1)

An AMP/TYCO 767004 38-position .025 VERT SMD logic analyzer probe connection is provided for the user to utilize for test points. This connection provides 24 general I/O signals to be observed on a Logic Analyzer probe using Mictor connections such as the Agilent 5346A.

Table 8. Test Pad Array BGA Reference

Mictor Pin	BGA	Mictor Pin	BGA
5	AA20	6	E24
7	V17	8	P26
9	W20	10	P25
11	AC25	12	U21
13	AC23	14	U19
15	AD26	16	V21
17	AB21	18	not used
19	AC22	20	not used
21	Y18	22	not used
23	AA19	24	not used
25	W17	26	not used
27	AC21	28	not used
29	Y17	30	not used
31	AA18	32	not used
33	AA17	34	not used
35	AB6	36	not used
37	E23	38	not used



High Speed Test Point
(see Appendix A, Figure 13)

DP1

General-purpose FPGA pins are available to a differential test pad. These connections allow a high-impedance probe to measure the performance of a coupled- differential output buffer pair.

DDR2 Memory
(see Appendix A, Figure 14)

U18

The LatticeECP2M Evaluation Board is equipped to an 84-ball BGA DDR2 SDRAM memory device such as a Micron MT47H16M16BG-3 device. The DDR2 memory interface includes a 16-bit wide device. The evaluation board includes termination of address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP2M device

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP2M35 PCI Express x4 Evaluation Board Revision B (Non-RoHS, Obsolete)	LFE2M35E-P4-EV	
LatticeECP2M50 PCI Express x4 Evaluation Board Revision B (Non-RoHS, Obsolete)	LFE2M50E-P4-EV	
LatticeECP2M50 PCI Express x4 Evaluation Board Revision B (RoHS Compliant)	LFE2M50E-P4-EVN	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2008	01.0	Initial release.
May 2008	01.1	Various minor updates to clarify text.
January 2009	01.2	Updated ordering information.

Appendix A. Schematics

Figure 5. Cover Page

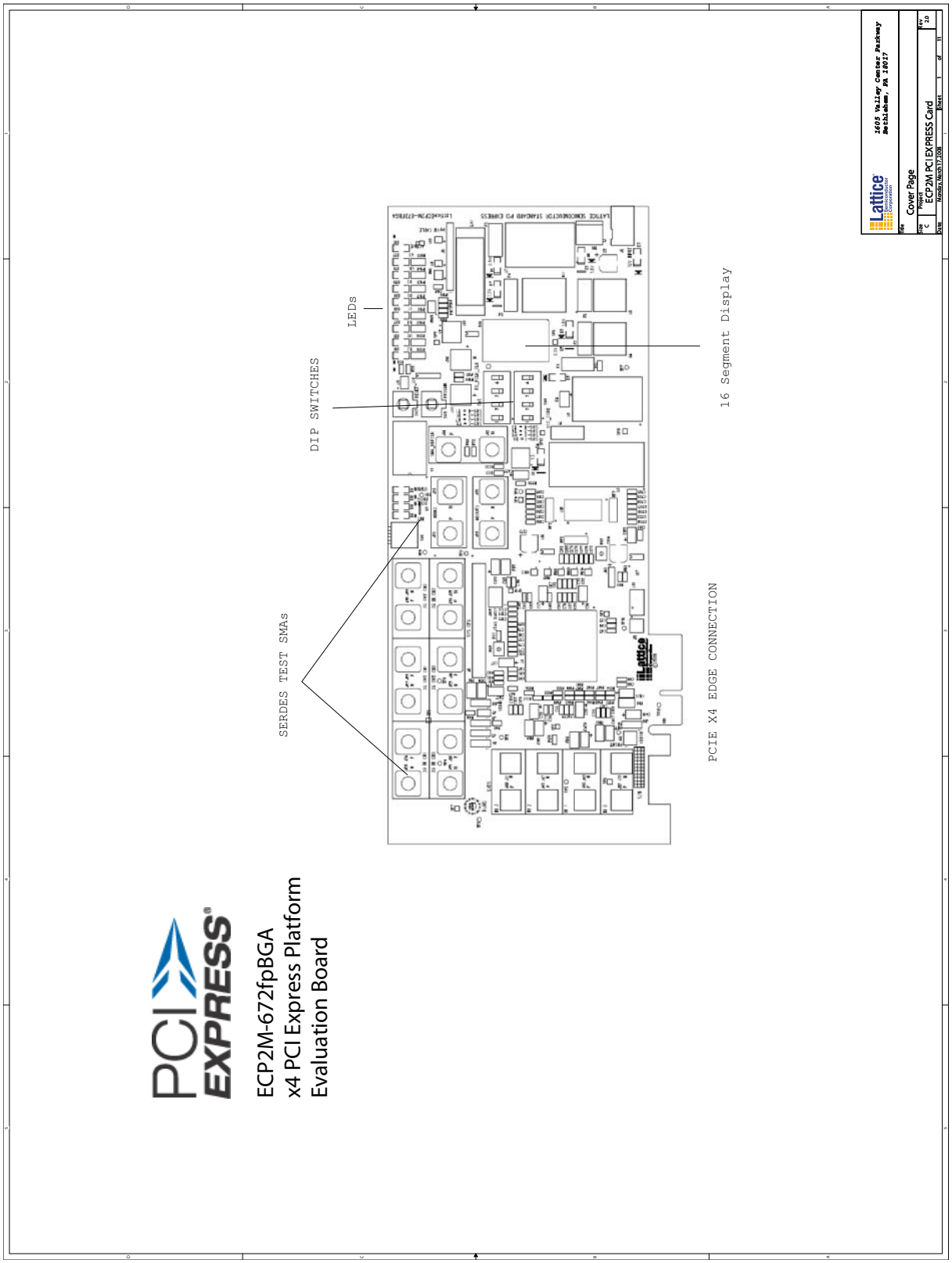


Figure 6. DC/DC Conversion

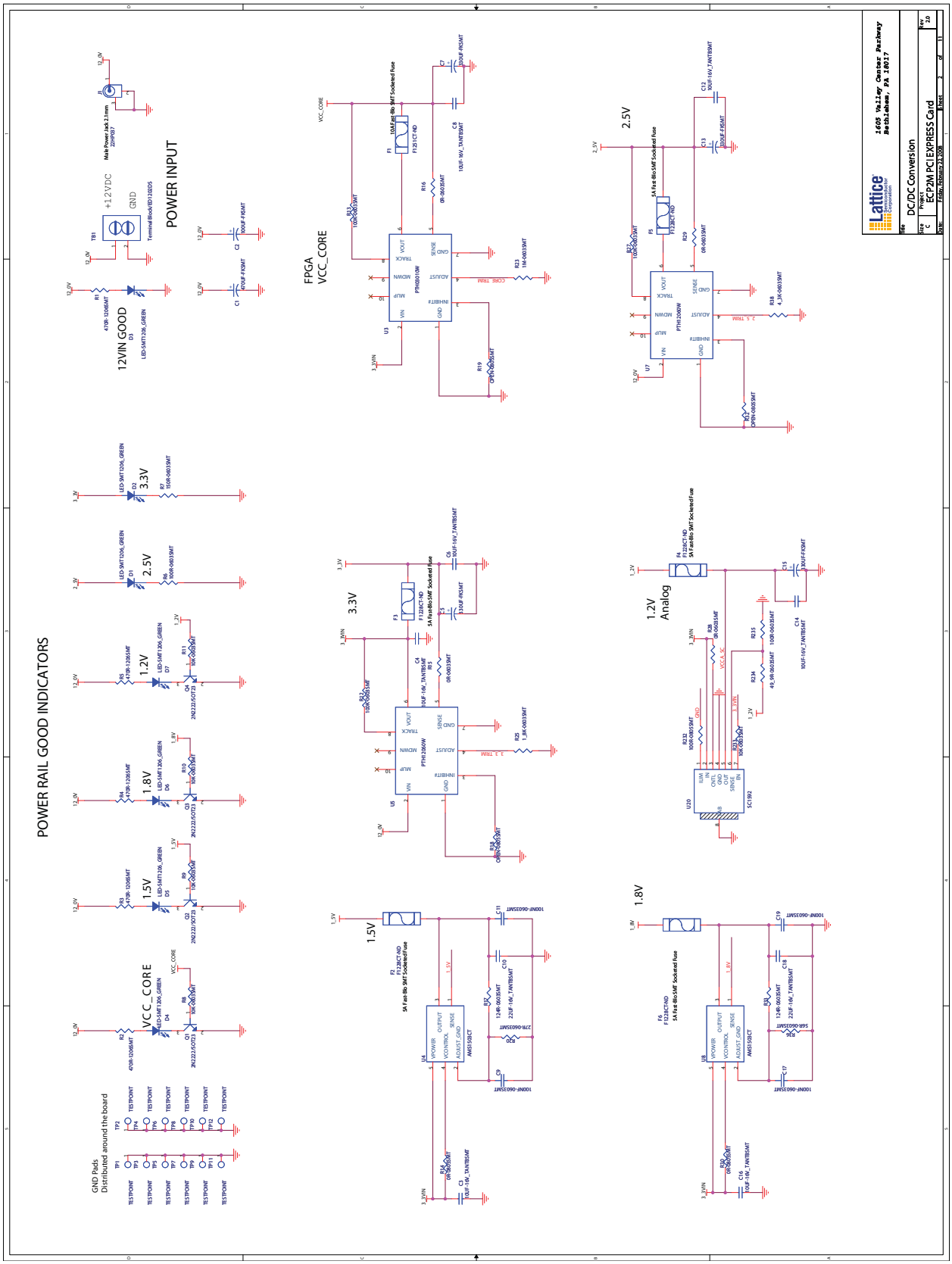


Figure 7. Power Supplies

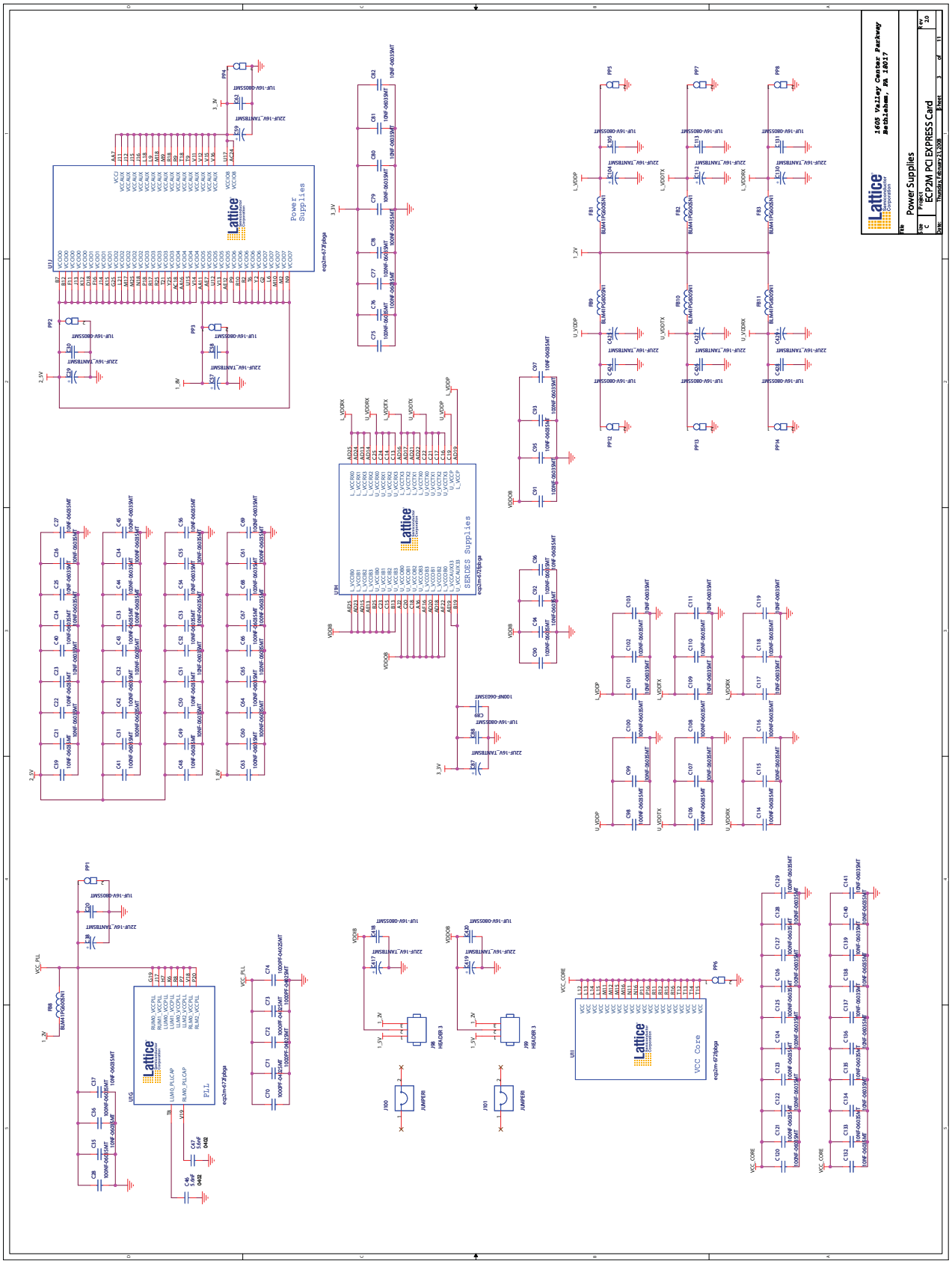


Figure 8. Configuration/Testpoints

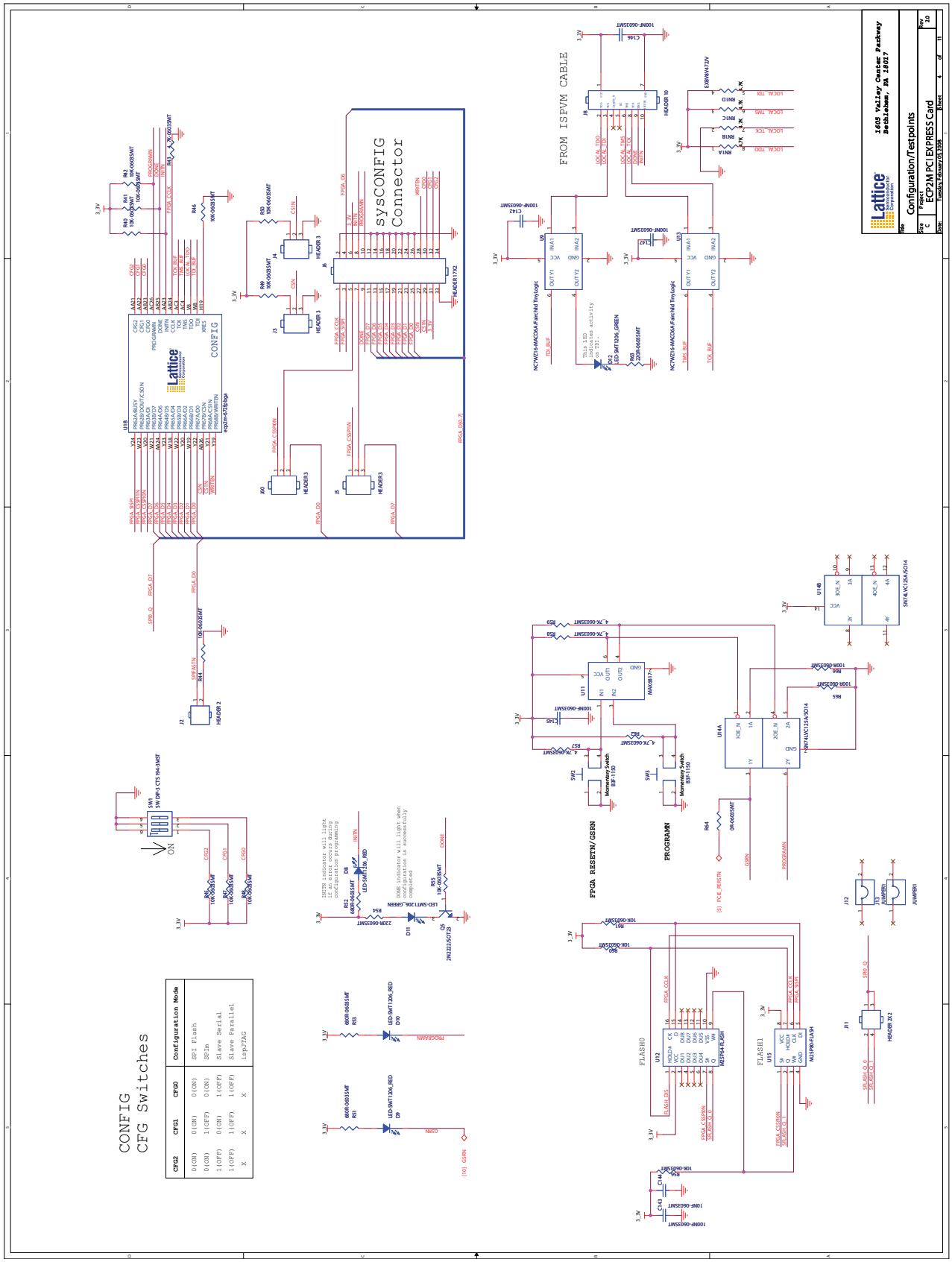


Figure 9. SERDES

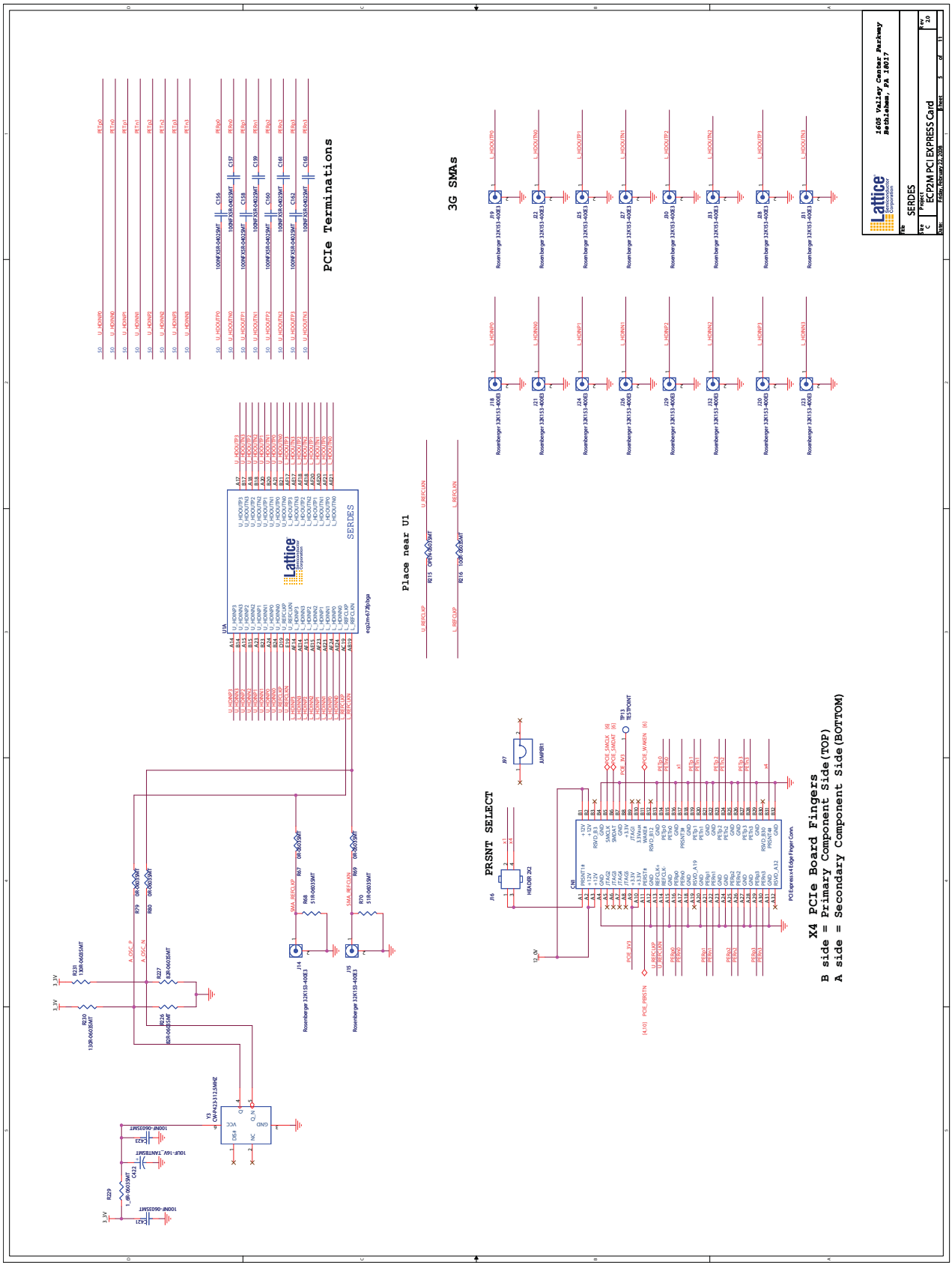


Figure 10. DDR2 FPGA Controller

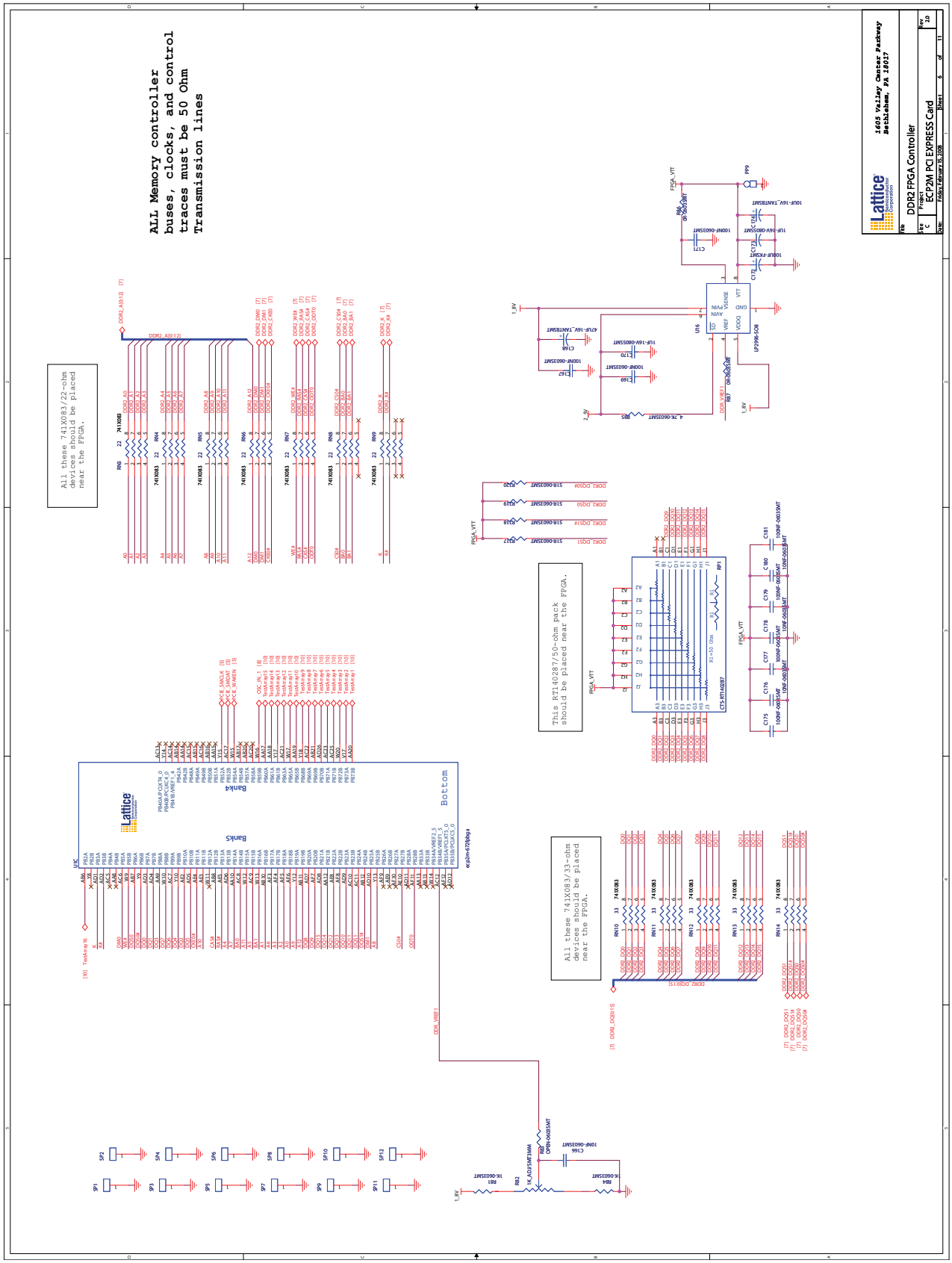


Figure 11. DDR2 Device/Termination

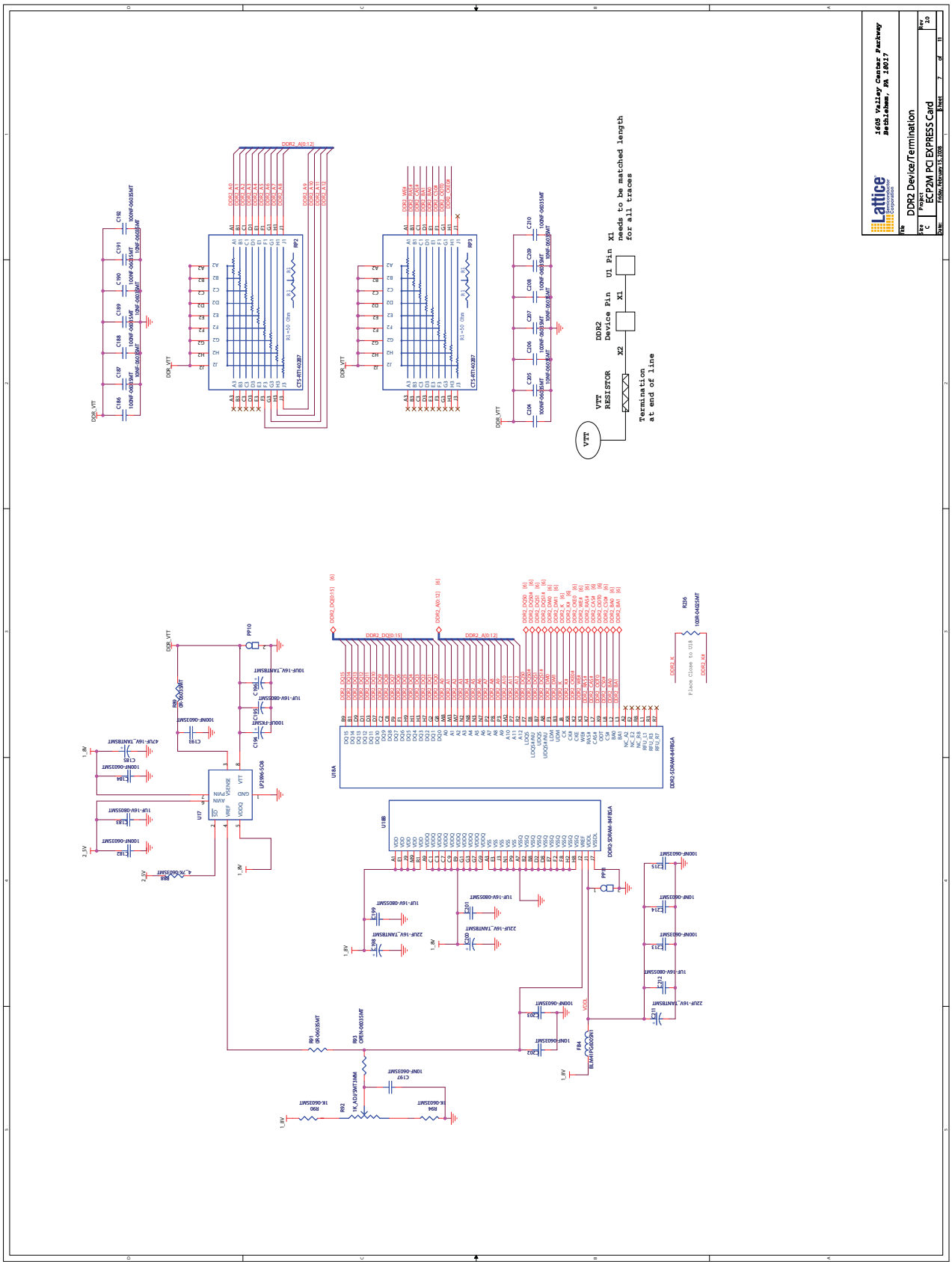


Figure 12. Clocks

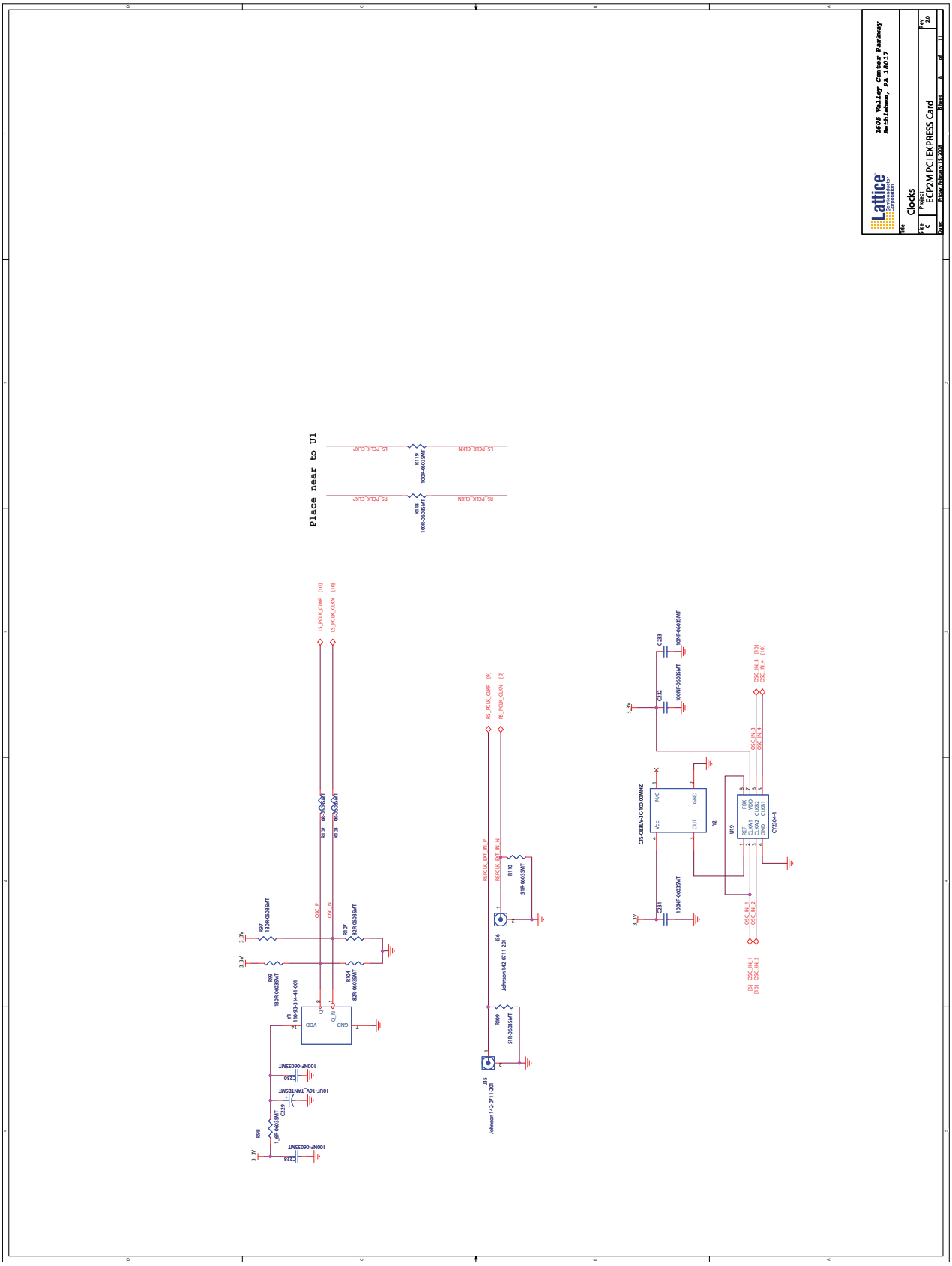


Figure 13. Differential I/O Loops

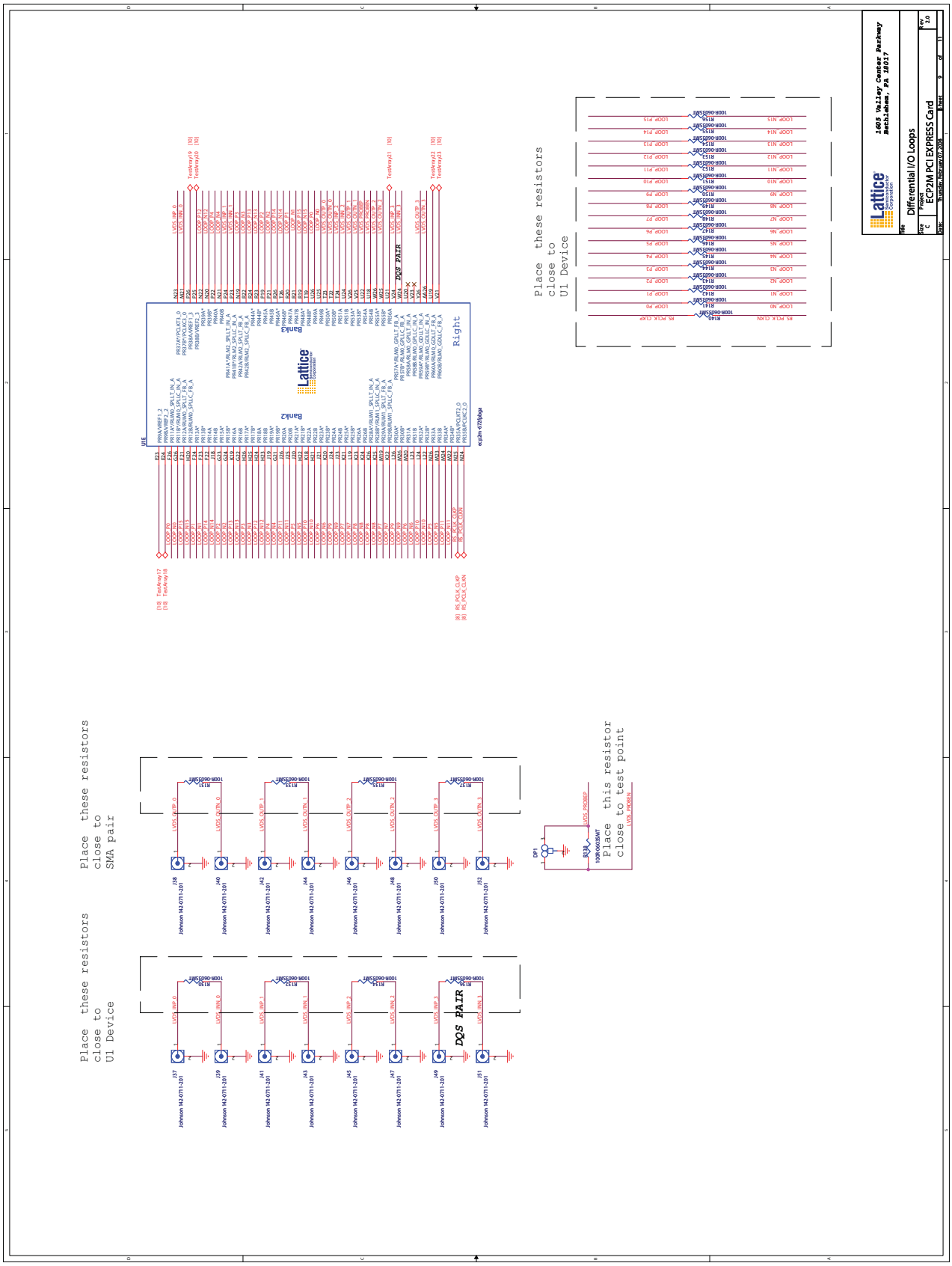


Figure 14. FPGA Test

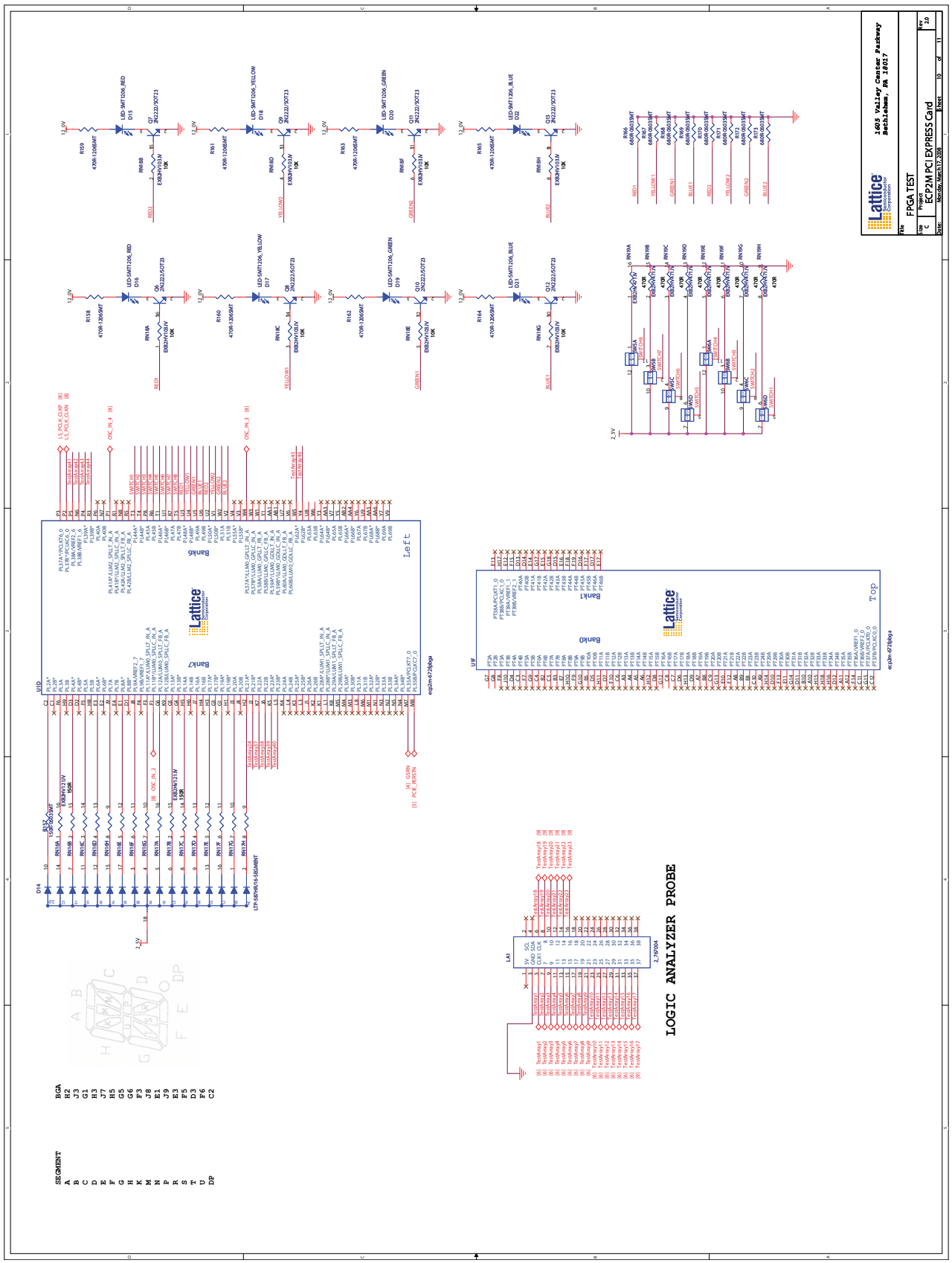


Figure 15. VSS/Decoupling