Lattice PCI Express Demo Installation

User's Guide

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Lattice PCI Express Demo Overview

Introduction

This user's guide describes how to install and run the various Lattice PCI Express (PCIe) demos. This guide covers the installation procedures for Windows 2000/XP/Server2003. The installation process is the same for all Lattice PCI Express demo packages. Different demo packages provide different features and may have different user interfaces, but they all are installed and started using the same steps. This installation guide covers installation of the Windows demo application, device driver and hardware evaluation board(s). Troubleshooting and uninstalling instructions are also provided.

The PCI Express demos show the capabilities of the Lattice FPGA and the PCI Express IP core functioning in a PCI Express slot in a Windows PC. The demos are designed to be simple and easy to use and require no test equipment. The demos use a Windows application to allow the user to access memory and registers on the board. This provides real-time interaction with the evaluation board hardware to demonstrate a functional PCI Express communications path between the application and driver software (running on the PC CPU) and the FPGA IP. The demo source code and IP reference designs can be obtained as separate installation packages from the Lattice website.

A demo package consists of a Lattice PCI Express evaluation board, Lattice FPGA bitstream, Windows driver and Windows application all running in a Windows PC. The evaluation board and the Lattice FPGA bitstream provide the PCI Express hardware while the driver and application provide the software to allow the user to exercise the PCI Express link. Figure 1 shows a typical demo setup using a PC motherboard without a case.

Figure 1. Typical Demo Setup

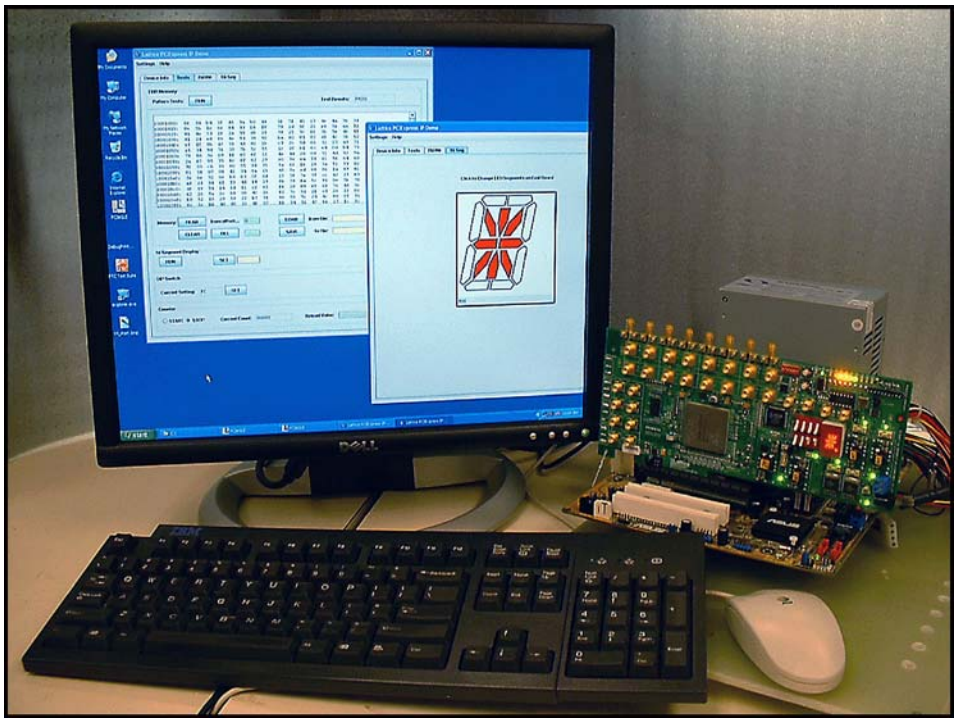
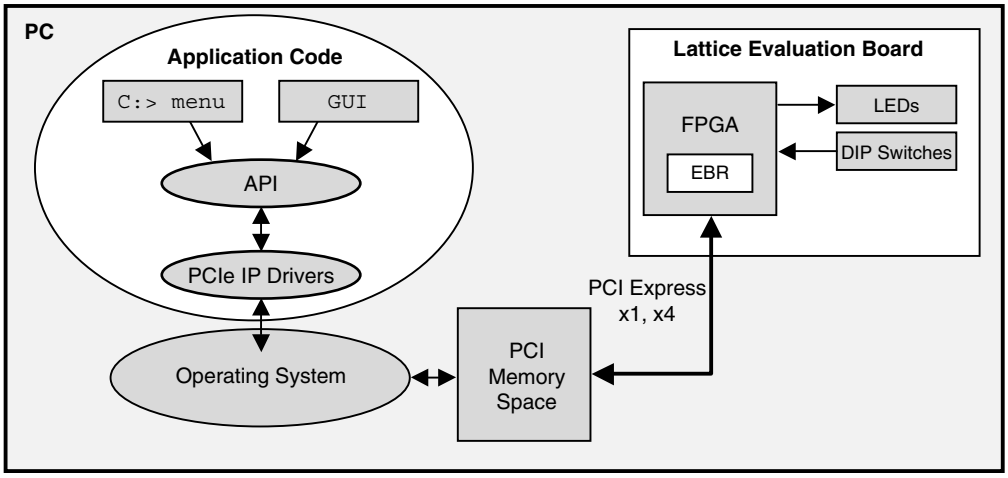


Figure 2 shows the relationship of the hardware and software components of the demo.

Figure 2. PCI Express Demo Block Diagram



The PCI Express IP core in the Lattice FPGA acts as a PCI Express endpoint. A PCI Express endpoint device looks like a regular PCI device to application software executing on a PC. It is a memory-mapped device occupying a certain range(s) of the PCI memory space. When the PC boots, the BIOS and OS probe the PCI Express and PCI buses and detect the devices present on the buses and assign them ranges in the PCI memory space. The PCI memory space is mapped into the application software's memory space by the supplied driver via OS kernel calls. Once the mapping is done, application IP registers, sitting on top of the PCI Express IP stack, can be read/written as memory locations by the application software. The demo software can now write to the LED register, read and display the DIP switch setting and read/write the EBR memory.

The demo software shows that the Lattice PCI Express IP core correctly handles the PCI Express protocol in a PC through the interaction with the devices on the evaluation board. The demos exercise the following functions:

1. Displays Operating System information on the detected Lattice evaluation board.
2. Displays information about the PCI Express IP core, such as reading and displaying all the pertinent information in the configuration registers, extended capability registers and control registers.
3. Performs GPIO Register Access: blink LED's; read DIP switches and display value.
4. Performs Memory Access: writes a pattern of values into internal FPGA EBR memory, reads back and verifies that all accesses are error-free.
5. Certain demos use hardware interrupts generated by the demo IP to indicate need for service.
6. Certain demos perform DMA access to the PC system memory.

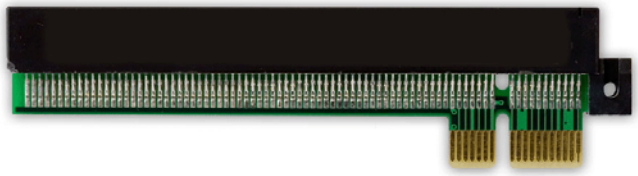
The PCI Express demo software does not programmatically control the PCI Express link size or operating mode. The PC BIOS and/or Windows sets these parameters during boot-up. The PCI Express board is detected through a bus enumeration device driver in Windows. Register reads and writes are done through the Windows bus driver and their operation is governed internally by Windows, the HAL, BIOS and possibly root complex register settings. The driver and application software are Windows WDM compliant. This means that they only use the APIs exposed by Windows to perform operations on the hardware. No attempt is made to directly control the root complex's PCI Express behavior.

In order to demonstrate the low-level PCI Express connection protocols, a test equipment exerciser and analyzer are needed (or at least an analyzer between the Root Complex and the endpoint). An external piece of test equipment is needed to generate, capture and examine training sequences, flow control, ACKs, NAK, message packets, configuration packet, memory packets, etc.

Adapter Boards

Each evaluation board needs to be installed in an available PCI Express slot in a PC. Since some of these boards are physically x4 and x8 connectors, an adapter board can be used to install an evaluation board in a PCI Express x1 slot. Figure 3 shows an adapter that allows any of the evaluation boards to be used in a x1 slot.

Figure 3. Adapter Board



When using an adapter card, only the lanes of the adapter card that plug into the motherboard are terminated. This poses a problem. SERDES inputs that are connected to SERDES channels that are powered up should not be left unterminated. For this reason the user should create (or use) a special bitstream for use with the adapter card.

Note: See the Bitstreams directory in the demo installation for specific downgraded bitstreams, i.e. a x1 for a LatticeSC80 x8 evaluation board.

Table 1. Examples of Adapter Usage

Evaluation Board	PCI Express Slot Used	Hardware Adapter Required	PCI Express IP Source
LatticeSC-80 PCI Express x8	x4 PCI Express	x4 Adapter	LatticeSCM MACO flexiMAC™ and LTSSM plus Soft IP
LatticeSC-80 PCI Express x8	x1 PCI Express	x1 Adapter	LatticeSCM MACO flexiMAC and LTSSM plus Soft IP
LatticeSC-25 PCI Express x1	x1 PCI Express	None	LatticeSCM MACO flexiMAC plus Soft IP
LatticeECP2M-35/50 PCI Express x4	x4 PCI Express	None	LatticeECP2M Soft IP
LatticeECP2M-35/50 PCI Express x4	x1 PCI Express	x1 Adapter	LatticeECP2M Soft IP

Background Knowledge

This Installation User's Guide assumes the user is familiar with basic PCI Express technology and is comfortable installing new hardware and software packages in a Windows PC. Some experience in these areas is helpful to install the evaluation board and the software.

Installation Guide

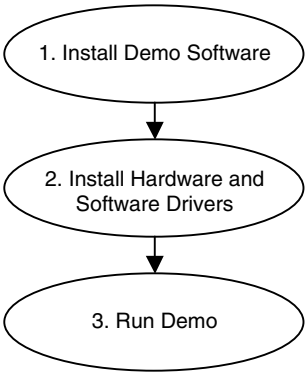
The Lattice PCI Express demo package is released as a Windows install executable. The package typically includes the Windows driver, FPGA bitstreams, Java GUI, Java runtime, and all demo source code. The executable needs to be run to unpack all the files. After the files are installed on the PC, the drivers are available to be installed when the evaluation board hardware is installed and detected.

This section discusses installing the demo package. The installation of the software and evaluation board hardware are discussed. Please read this section completely before attempting to install the package so that you understand the steps involved and how they apply to your specific situation.

Installation Overview

The following three steps are taken to install and run a demo:

Figure 4. Installation Procedure

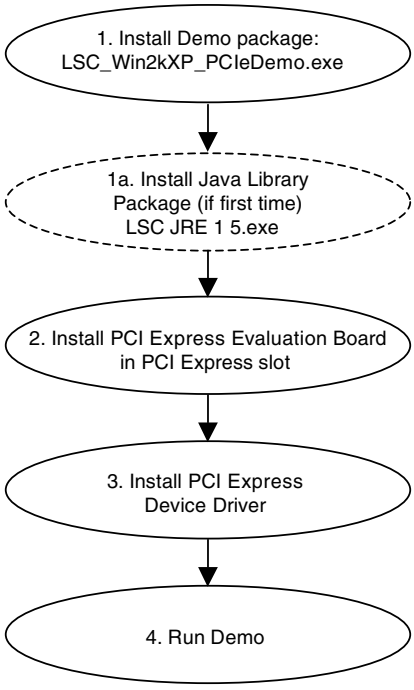


NOTE: LATTICE IS NOT LIABLE FOR ANY LOSS OF DATA OR DAMAGES THAT MAY RESULT FROM THE INSTALLATION OF THE HARDWARE AND EXECUTION OF THE DEMO SOFTWARE. DO NOT INSTALL AND OPERATE ON MISSION-CRITICAL SYSTEMS.

Installation

The following steps are taken to install and run the demo. The first step is to install the demo package. The FPGA bitstreams are available after installation. The evaluation board should then be programmed with the correct bitstream (if it has not been previously loaded). This should be done without installing the board in the PC. Use the ispVM USB download cable and the external power supply. Then install the board in the PC and install the driver when Windows finds new hardware. The demo can now be run.

Figure 5. Demo Installation Flow



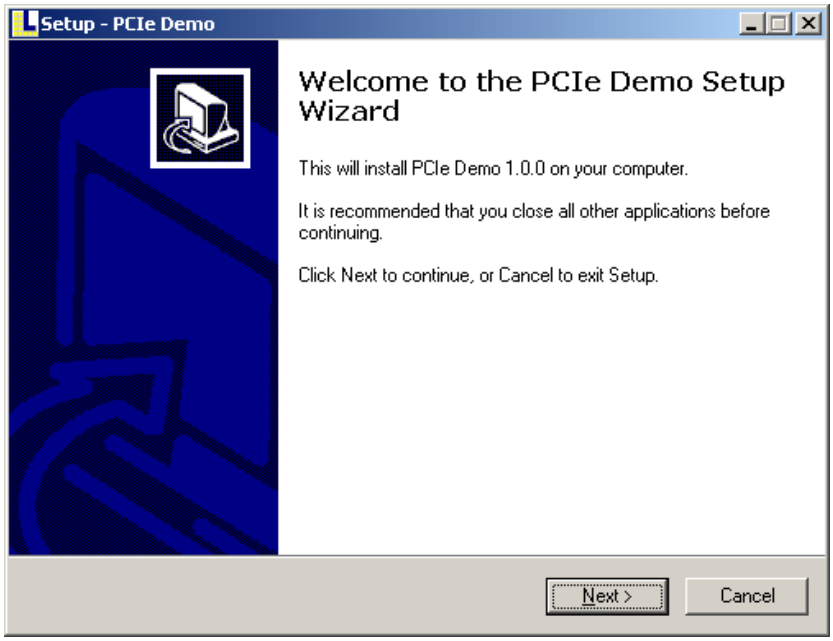
Demo Package Software Installation

Double click on the executable demo installation program to start the installation process. You may need administrator rights to install in the default location of **C:\Program Files**.

Note: The following screens are an example installation. The demo you are installing may have different information on the screens, but the procedures are the same.

Double-click on the installation program to start the installation process.

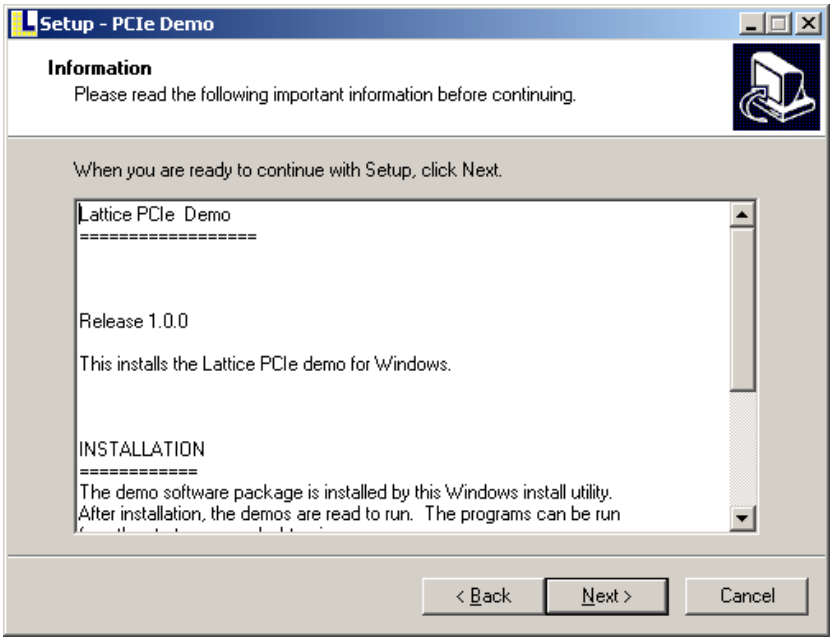
Figure 6.



Click **Next** to continue.

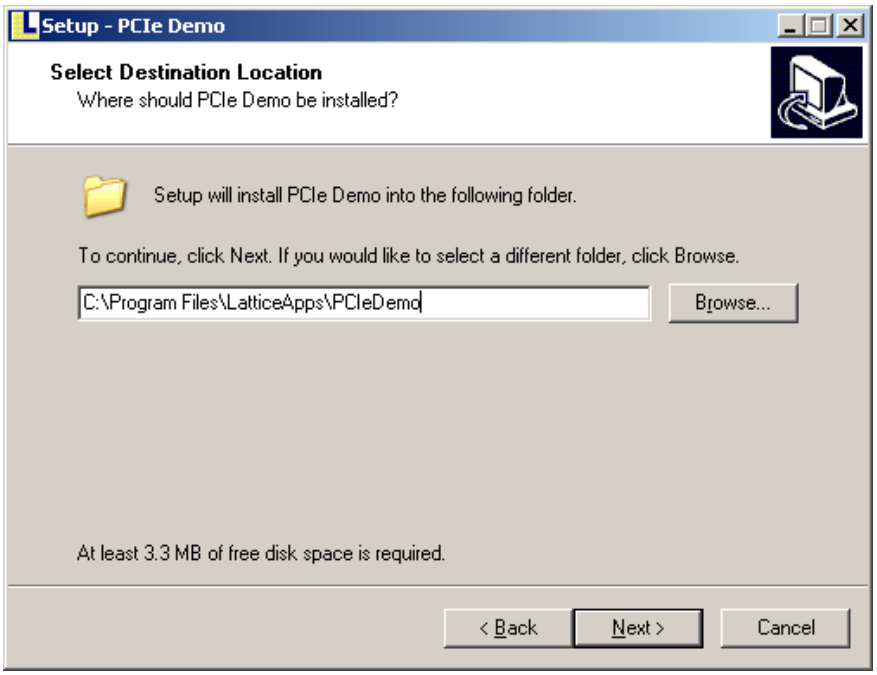
Click **Accept** to accept the license and then **Next** to view the installation notes. Be sure to read the Installation Notes that provide additional information on installation, which evaluation boards are supported, and where to find demo documentation that should be consulted for demo operation.

Figure 7.



The next page lets you choose the installation location. The default location of **c:\Program Files\LatticeApps** is recommended. The demo program may rely upon other Lattice libraries and packages (the Java JRE package for example) which it expects to find in **C:\Program Files\LatticeApps**.

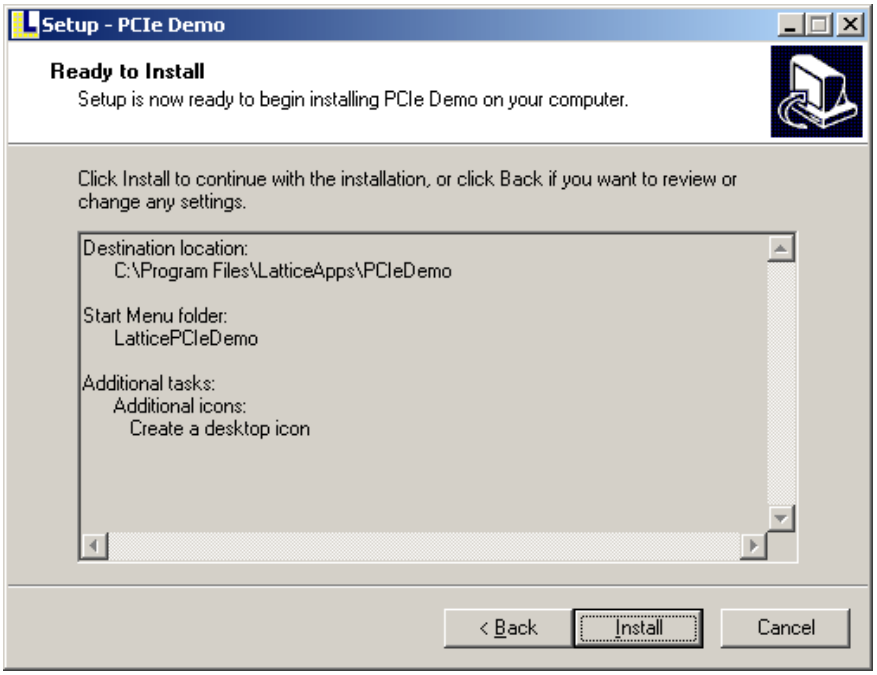
Figure 8.



Click **Next** and then click Next again to accept the start menu program group name. Select **Create Desktop Icon**.

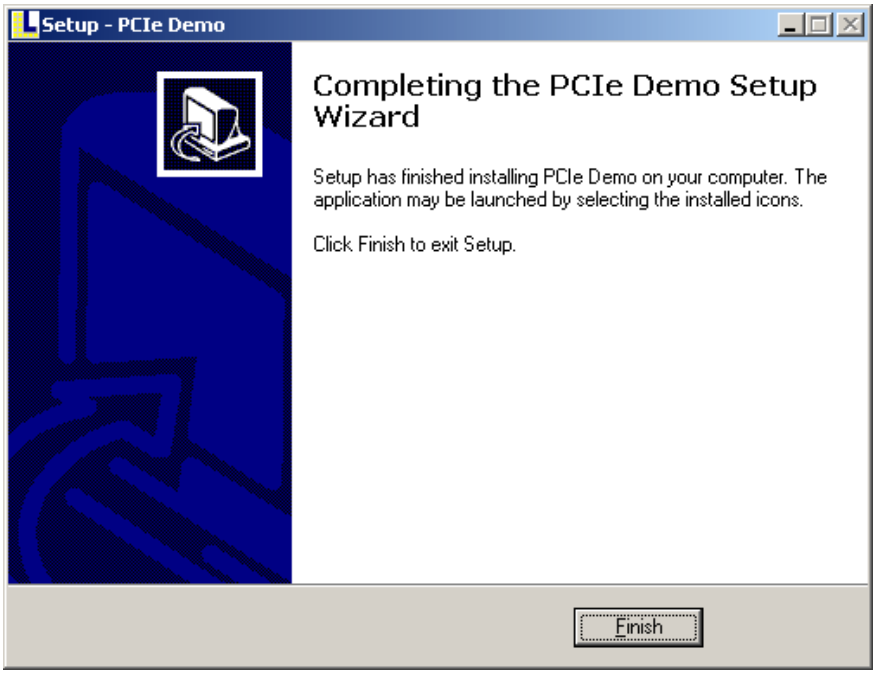
The Default Install configuration will be:

Figure 9.



Click **Install** to begin the process.

Figure 10.



After a successful installation, the above screen will appear and demo icons will appear on the desktop, as well as a Lattice PCI Express specific demo program group in the **Start->Programs** menu bar.

Demo Java Library Package Software Installation

The Lattice PCI Express demo GUIs are written in Java for portability between Windows and Linux platforms. The Java GUI requires a Java Runtime Environment. A pre-built version of the correct JRE is bundled into a stand-alone package. The JRE package is a trimmed-down set of the full Java JRE (Java Run Time Engine) based on the JRE included with Java 2 Platform Standard Edition Development Kit 5.0 (jdk1.5.0_06). The purpose of providing this separate JRE package is to ensure a standard, controlled Java run-time is available for the demo GUI. The JRE bundle is the exact version the demo GUIs were developed with and tested on. Using this JRE guarantees trouble-free GUI operation.

The user can download and install the JRE 5.0 from the Sun Microsystems website. Newer versions of the Sun Microsystems JRE have not been tested and may or may not work. If another JRE package is used, edit the startup script files located in the demo directory to explicitly invoke the alternate JRE.

You only need to install this package once. All future Lattice PCI Express demos will share this library.

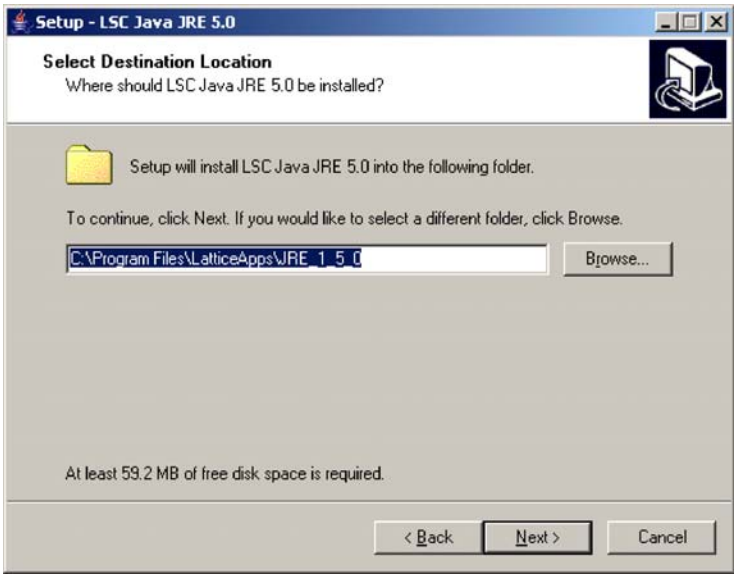
Installing the Lattice JRE package (LSC_JRE) will not affect any current or future installations of Java on the system. The package is placed in the **LatticeApps** directory tree and no environment variables or registry settings are added or affected.

Obtain the **LSC_Win2kXP_JRE_1_5_0.exe** file from the Lattice website and follow the instructions to install the package.

Figure 11. Lattice JRE Installation

The default installation location should be used. All PCI Express demo GUIs will look for the library in this location. If the JRE package is not installed in the default location, the startup scripts for the demos will need to be modified to point to the alternate installation location.

Figure 12. Selecting the Installation Location



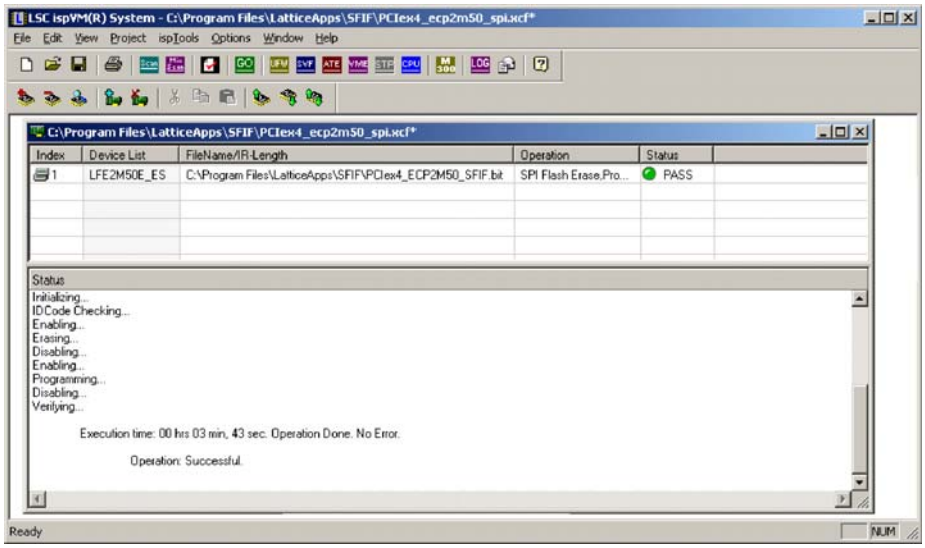
Lattice PCI Express Evaluation Board Installation

The demo requires a Lattice PCI Express evaluation board. The demo will not run in the absence of an evaluation board installed into a PCI Express slot on the motherboard since the driver will not have anything to open, and the demo application will not have anything to communicate with. (Some demos may offer a simulation mode, allowing execution of the GUI without having an evaluation board installed.)

The supported PCI Express Evaluation boards are listed in the Installation Notes screen during the installation process. They are also in the Readme.txt or other documentation files located in the demo installation directory. These boards should be loaded with the appropriate bitstream located in the Bitstream directory of the demo installation directory. The bitstream files are suitably named to identify the specific evaluation board they support. Double-click on the appropriate ispVM® .xcf file to launch ispVM and program the SPI Flash device on the board with the correct bitstream. The board's SPI Flash must be programmed before installing the board in the PC. See the specific evaluation board user's guide for details on programming the board with ispVM.

Note: The ispVM XCF files assume ispVM is installed in the default location. If the ispVM package was installed in another location, you may need to run ispVM and manually select the location of the bitstream file.

Figure 13. Example ispVM Bitstream Programming



Evaluation Board Hardware Installation

After ensuring the proper bitstream is loaded into the SPI Flash, the board can be installed in a PCI Express slot. Take note that you are installing it in a PCI Express slot and that the PC power is off and you are taking anti-static precautions (touch the PC case before handling the board).

IMPORTANT: Shut down the PC and then turn off the power supply. PC power supplies have standby voltages that are present even when the PC power light (and fan) is turned off. Turning off the power supply (if possible) is the safest way to ensure the board will not be "hot-swapped".

Note: The FPGA bitstream must already be loaded into the SPI flash on the evaluation board. The FPGA must be programmed with the PCI Express IP core when the PC powers up so that the endpoint is seen by the North Bridge root complex and the BIOS and OS allocate resources for it.

To install the Lattice PCI Express evaluation board:

1. Shut down Windows and the PC.
2. Turn off power supply or unplug the power cord.
3. Locate an available PCI Express slot. Using ESD precautions, install the Lattice PCI Express Evaluation Board in the PCI Express slot. You may need an adapter board to convert the board to a x1 slot.
4. Power-on the PC and observe that it boots normally to the Windows login screen. Consult the Trouble Shooting section of this document if anything abnormal occurs.
5. Log in as a user with administrator rights. During the login process Windows will detect the new hardware and ask if you want to install it.

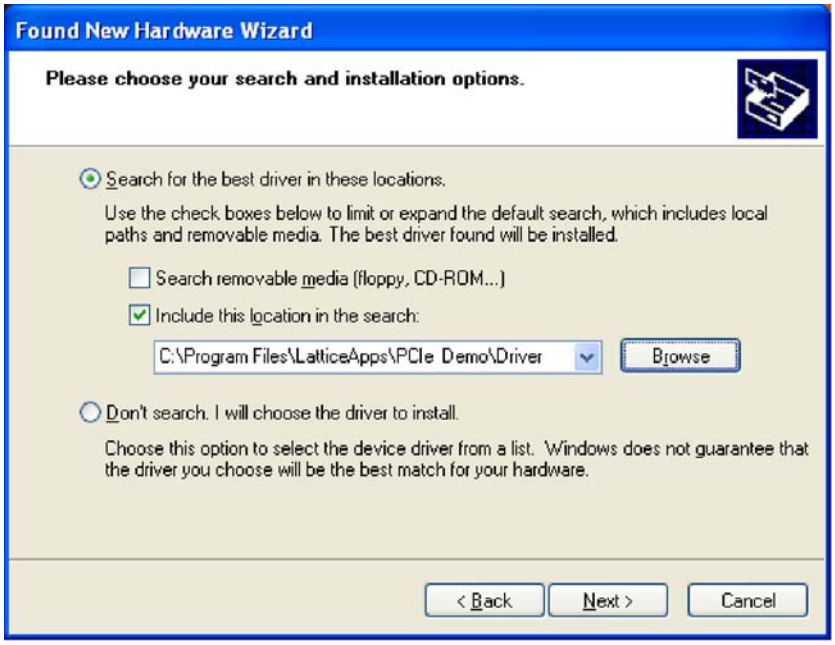
Evaluation Board Driver Installation (Windows XP)

This section describes installation of the evaluation board device driver software on a Windows PC. The screen shots included are from installation on an XP system. The Windows 2000 and Server2003 procedures differ slightly. These two operating systems have slightly different dialog box options, but the process is very similar. The "Found New Hardware" screen will appear when the PC is booted for the first time with the evaluation board installed. If this screen does not appear, the evaluation board was not properly detected by the PC BIOS or Windows. Refer to the Trouble Shooting section of this document for further information.

Figure 14. Found New Hardware Screen

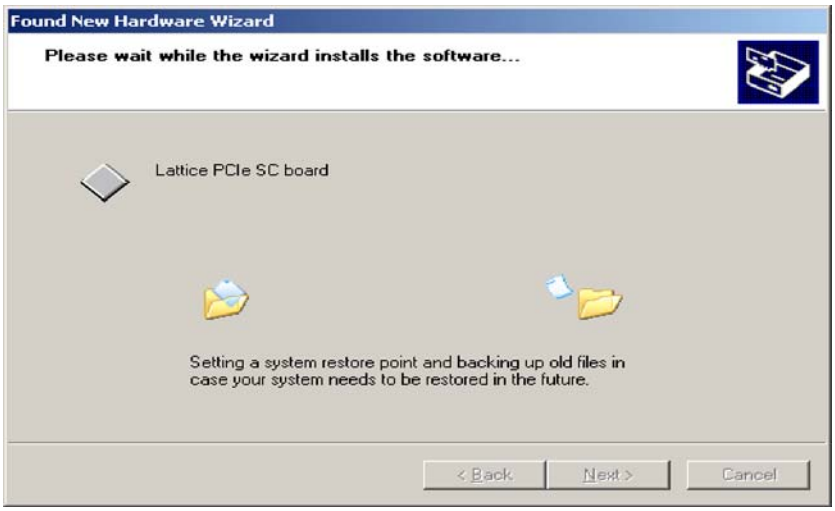
Select the **Install from specific location** option and click **Next**. Browse to where you installed the demo package, locate the **Demo\Driver** directory. The default location of the folder is: **C:\Program Files\LatticeApps\PCIe Demo\Driver**.

Figure 15. Selecting Driver Location



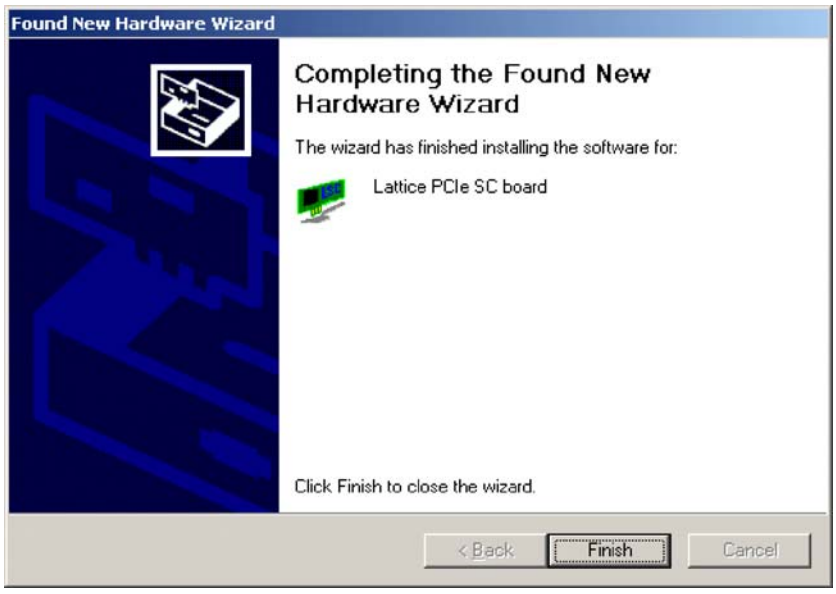
Click **Next** to continue.

Figure 16. Installing Driver



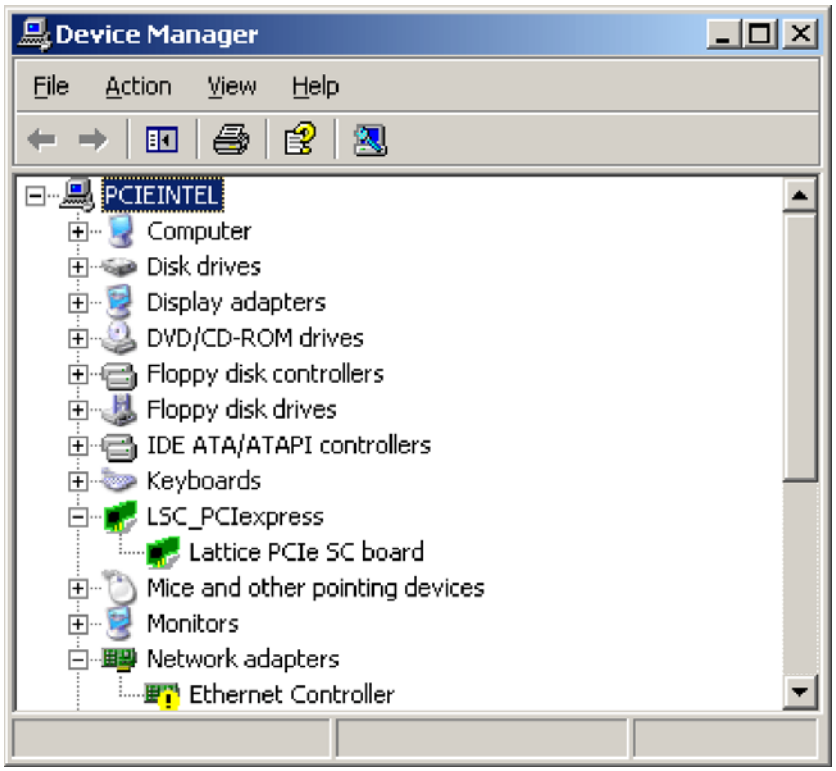
Windows now copies the driver files and will display the following screen when finished.

Figure 17. Driver Installation Complete



To confirm the installation and verify that Windows properly sees the evaluation board hardware, right-click on **My Computer** (on the Desktop) and choose **Properties**. Select the **Hardware** tab and press the **Device Manager** button. The Lattice Evaluation Board (LSC_PCI Express) will appear in the list of hardware devices in your system. If the evaluation board is equipped with a 16-segment display (and a newer driver is being loaded, lscpcie2.sys or lscdma.sys) a capital "I" will be displayed on the 16-segment display. See the Troubleshooting section of this document for more information on 16-segment display codes.

Figure 18. Verifying Hardware is Installed



Right click on the **Lattice Eval Board** icon and select **Properties** to show the resources assigned to the device and the driver information. Memory ranges corresponding to the configured BAR registers will be assigned to the board. If this is all present, then the demo program is able to run and access the hardware on the evaluation board.

Installation in a Different Slot

Windows identifies PCI/PCI Express hardware devices using the bus, slot, vendor ID and device ID fields. If you install the board into a different slot, the slot number will change. This will cause Windows to display the "Found New Hardware" message box when the system powers up. The entire set of preceding steps to install the driver do not need to be taken, since the driver has already been installed. If the board is installed in a new slot, simply choose to let Windows search for the driver ("Install the software automatically (Recommended)" and install automatically. Windows will then associate the newly created device registry tag (bus, slot, vendor and device ID) with the lscpcie.sys driver and the demo GUI will work with the board in the new slot.

This same scenario will occur when installing a LatticeECP2M evaluation board after installing a LatticeSCM evaluation board. The LatticeECP2M has a different PCI device ID, so Windows considers it new hardware and needs to associate it with the lscpcie.sys driver that has already been installed.

Un-Installing the Software

If you want to remove the software from your system (e.g. to perform a clean installation of a new version), the Lattice PCI Express Demo program group includes a remove program option which will remove the application code. To remove the driver code, use the "Uninstall/Unplug a device" option from the Hardware Wizard. Choose to uninstall and select the Lattice PCI Express device.

Running the Demo

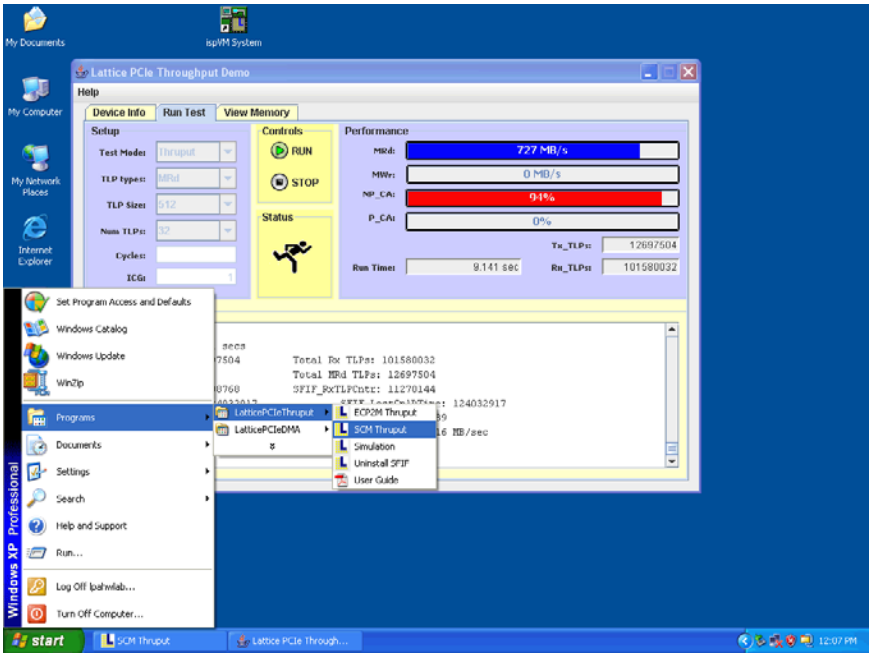
A PCI Express Demo program is launched from the **Windows Start** button:

Start->Programs->LatticePCIe->Program Name

You may also launch the demo using the desktop icons (if selected during installation).

Check the Demo Program Group for any user's guides and available demos to execute. Each demo may have program options specific to the features it demonstrates.

Figure 19. Launching a Demo



Demo Setup

Additional setup is not normally required if the demo programs are run from the **Start->Programs->LatticePCIe** program group. Some demos use a utility program called Scan to discover the evaluation boards installed in the system. If there is more than one evaluation board installed with a compatible bitstream for the demo, a menu will be displayed for the user to choose which board to communicate with. For example, if a LatticeECP2M50 x4 and a LatticeSCM80 x4 are both installed, the first time the demo launch program is run it will recognize both boards and ask which one to use for the demo.

The scan program creates a configuration file. If this file exists, it is used for subsequent runs. If the user installs another board or wishes to connect to a different board, the Scan utility needs to be re-run first to update the configuration file with the new board information. This is only required if boards are being interchanged in the system. See the demo's Program Group for the Scan Boards program.

Troubleshooting

This section outlines some debug procedures to follow when experiencing trouble installing or running the demo.

Tips and Tricks

Driver Codes

Newer Lattice PCI Express device drivers (lscpcie2.sys, lscdma.sys) display codes on the evaluation board's 16-segment LED during driver activity. The codes can be used to determine if communication with the driver and board hardware are functional. The following characters are displayed:

- **I** – (Capital i) displayed during driver initialization time. Occurs during Windows boot. If the "I" is not present, the board was not recognized or the driver did not load.
- **E** – Displayed if an error was detected by the driver, such as memory resource allocation, interrupt connectivity, etc. The driver disables access to the board and no demos will be able to run.
- **O** – Displayed when an application opens the driver and accesses the board. This display is usually quickly overwritten by the application's own usage of the 16-segment display, and is generally not visible for long.
- **C** – Displayed when an application closes access to the board.
- **R** – Displayed when the driver is removed from the system.

Disable/Enable Driver

The driver can be manually removed and installed through the Device Manager screen. Launch Device Manager and right-click on the **Lattice Evaluation Board** icon. Select the **Disable** option to disable the driver and all access to the board. An "R" should be displayed on the 16-segment LEDs. Select the **Enable** and the driver will be re-loaded and initialize the hardware. An "I' will be displayed on the 16-segment LEDs.

This can be useful when a new bitstream has been dynamically re-loaded into the board while the system is running (via ispVM) and the program button has been pressed. This reloads the FPGA with the new design, but in the process loses connection to the PC. The above method will cause the board and driver to be re-loaded and operations can continue without rebooting Windows.

Identifying Installed Boards

Certain demos may contain a Scan Boards program option. This program enumerates all known Lattice PCI Express evaluation boards installed in the system. The demo bitstream code is displayed. This can be used to verify that Windows and the driver see the board and recognize the bitstream. Demos will only work with the demo IP for which they were designed. A code is placed in the PCI SubSystem Vendor ID register to identify the IP version. For example, if the evaluation board has a Throughput Demo bitstream loaded, the PCI Express SG-DMA will not recognize the code and will not run on that board. Scan can be used to detect the board and display the fact that the Throughput Demo IP is actually loaded.

Trouble Installing the Demo Software Package

The most likely issue that can arise is the issue of permissions when installing. Depending on the system security policies, the user my need to have administrator permission to install into the Program Files directory (the default location).

Trouble with the Board

Ensure the board is installed in a PCI Express slot. It can physically fit into a PCI slot. This can damage the board or PC if power is applied when it is in the wrong type of slot.

Ensure the board has a valid PCI Express bitstream loaded in the SPI Flash. The bitstreams are provided in the demo installation directory. Configuration files for ispVM are also present so all you need to do is double-click on the .xcf file and use ispVM to program the boards. See the board manuals for information regarding any special jumper settings and cable connections for the ispVM JTAG programming module.

Ensure the four Status LEDs are on, indicating the board is seen as a PCI Express endpoint. If the two yellow LEDs and two green LEDs are not on, the board will not be recognized by the PC BIOS or Windows. You can try installing in a different PCI Express slot to see if that fixes the link-up problem. You can also try pressing the Evaluation Board's reset button immediately after the PC boots.

Note: Some PCs do not support a x4 link width device in a x16 graphics slot. In this case, the four LEDs on the top (two yellow, two green) will not light when the PC is powered up and/or the board will not be seen by Windows. If this is the case, try another slot (preferably a x4) or another PC.

Ensure the board is seen by Windows. Check **My Computer->Properties->Hardware->Device Manager** and verify the LSC_PCIe driver and evaluation board are shown in the list. If not, shut down the system and try another slot. If the board is present, go to **Properties** and the **Resource** tab to verify that memory was assigned to it. Also verify the Vendor ID and Device ID are valid, as seen be Windows Plug-n-Play. If the values are invalid, perhaps the bitstream is corrupt and needs to be reloaded into SPI Flash.

Trouble with the Driver

The evaluation board must be installed in the PC, and seen by Windows, for the driver to be installed. If you do not see the "Found New Hardware" message when logging in after installing the board, check the board's status LEDs. Try a different PCI Express slot.

Make sure you specify the search location for the driver during installation. Tell Windows to install from the specific demo Driver directory located under the **LatticeApps\DemoName** directory.

You will need administrator permission to install device driver files.

Trouble Running the Demo

The evaluation board must be installed in the PC, and seen by Windows, for the driver to be installed/loaded. The driver must be loaded by Windows in order to run the demo. Verify that Windows sees the board and has loaded a driver for it.

If the test software exits immediately, there are two probable causes:

1. The driver was never loaded (or the evaluation board is not installed)
2. The board failed to be detected by Windows.

Either way, the board needs to be installed and seen by Windows and the LSC_PCIe version 2 (lscpcie2) driver needs to be associated with the hardware.

Windows Debug Tools

Some demos use a utility program called Scan to discover the evaluation boards installed in the system. The Scan program creates a configuration file. If this file exists, it is used for subsequent runs. If another, different board is installed, the Scan utility needs to be re-run first to update the configuration file with the new board information.

See the demo's Program Group for the Scan Boards program and run it.

Windows offers some utilities to interrogate the operation of hardware devices. Use these tools to verify the evaluation board device driver is loaded and running.

My Computer
Right-click on the **My Computer** icon and select **Properties** and then the **Hardware** tab to reach the **Device Manager** button. The Device Manager provides information on the hardware devices and the drivers associated with them. The Hardware Wizard allows the installation and removal of drivers. You need to have administrator rights to run the Hardware Wizard and to install and remove drivers.

Figure 20. Device Manager

The most useful tool is the driver properties to verify that the lscpcie2 driver has been installed and is the correct version. Double-click on the LSC_PCIe board icon and the following window will appear with information on the board and driver. The Driver tab provides version information about the driver.

Figure 21. General Tab

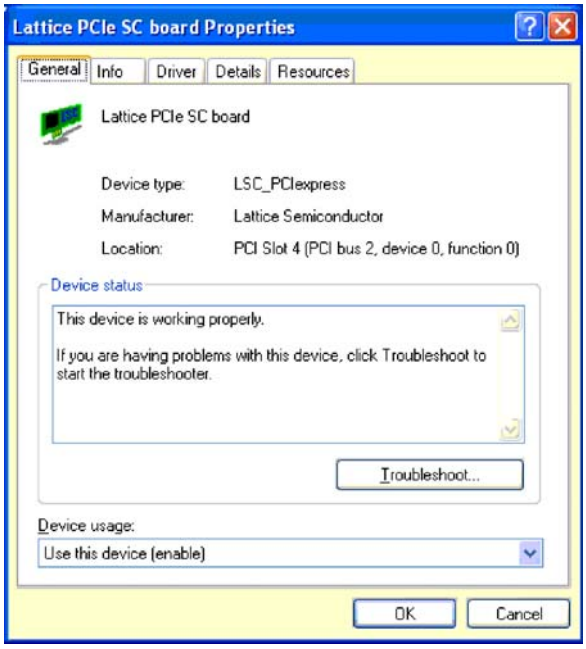
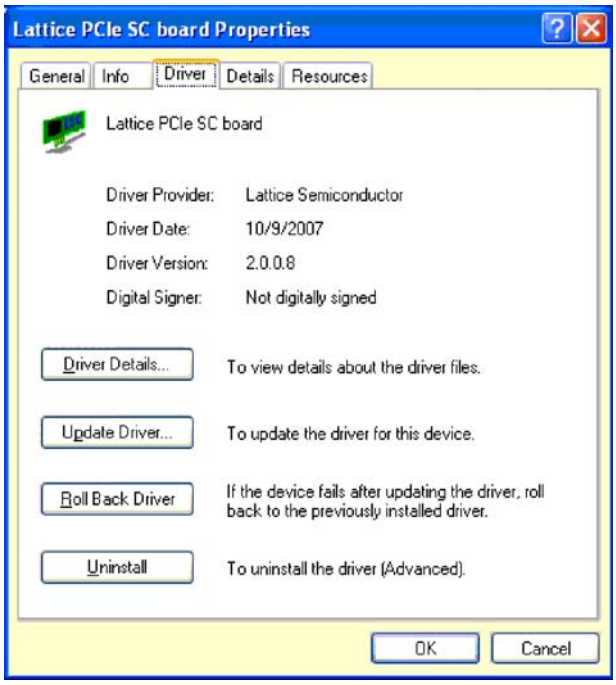


Figure 22. Driver Tab



References

The following documents provide more information on topics discussed throughout this guide.

- PCI Express IP User's Guide
- LatticeSC80 PCI Express x8 Evaluation Board User's Guide
- LatticeSC25 PCI Express x1 Evaluation Board User's Guide
- LatticeECP2M Advanced Evaluation Board User's Guide

These documents are available on the Lattice web site at www.latticesemi.com.

Technical Support Assistance

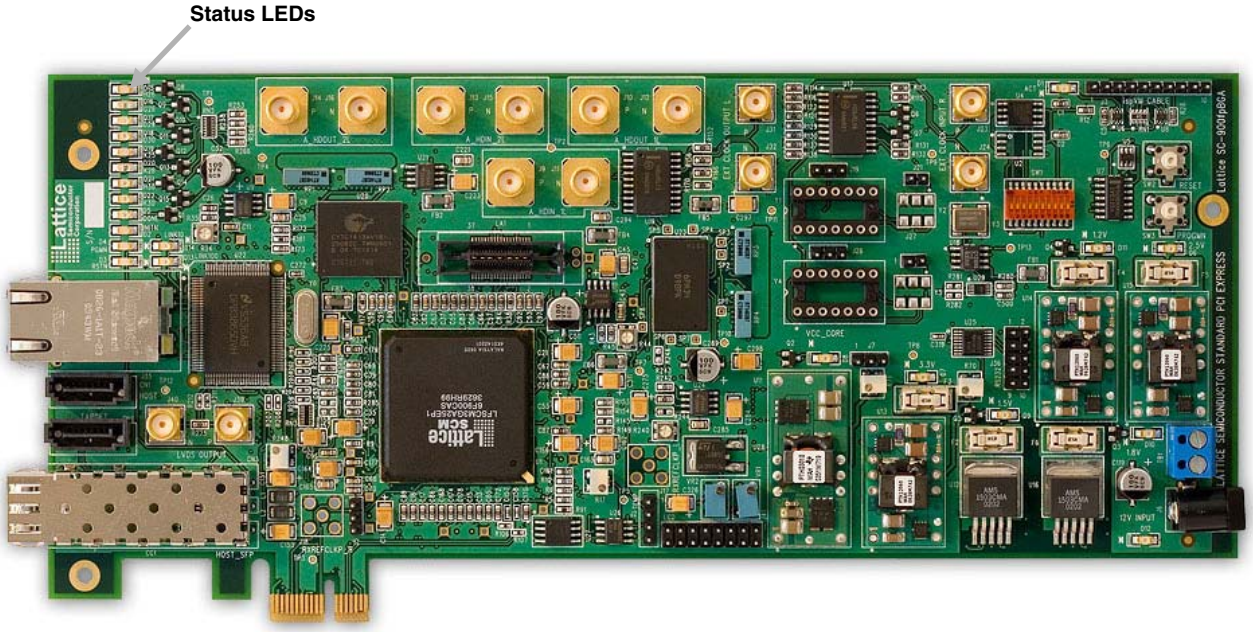
Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
January 2008	01.0	Initial release.
January 2008	01.1	Updated Installation Guide text section.

Appendix A. LatticeSC PCI Express x1 Evaluation Board

Figure 23. LatticeSC25 PCI Express x1 Evaluation Board



The LatticeSC25 PCI Express x1 evaluation board does not have the 16-segment display nor the DIP switches. This board can still be used with the PCI Express demo, but the operations that deal with the 16-segment display or DIP switches will have no affect on the board, since they are not physically present. The EBR memory tests can be used with this board, but the direct, interactive demos will not be of any use.

The LatticeSC25 board has a physical PCI Express x1 connector. Electrically it is wired to one FPGA SERDES. It can only operate in x1 PCI Express mode. The bitstream that is loaded must set the PCI Express IP core as x1 in the LatticeSCM.

The LatticeSC25 board is used without any adapters. It can be installed in any size slot in a PC. All slots must support the ability to fall back to x1 mode. The demo software will work with this board installed in any PCI Express slot

In summary, an adapter is not required when using the LatticeSC25 PCI Express x1 board. It only supports x1 operation.

For more information on the operation of this board, please refer to the *LatticeSC PCI Express x1 Evaluation Board User's Guide*, available at: www.latticesemi.com/boards.

LED Definitions

The Status LEDs on the LatticeSC PCI Express x1 Evaluation Board are located vertically along the left edge of the board (i.e., they are visible through the expansion slot when installed in a PC). The LEDs are in the following order and have the following functions:

Table 2. LED Order and Functionality

LED	Color	Usage
D15 (top)	Red	PCI Express access to IP on wishbone bus (EBR and registers). Negative logic: on=no activity, off=activity.
D16	Orange	Data Link up, ready for packets at Transaction Layer (PCI enumeration of configuration registers).
D17	Green	L0 training sequences completed, PHY layer up and ready for flow control.
D18	Blue	Not used (off).
D19	Red	Segment K of the GUI 16-segment display. Negative logic: on=no activity, off=activity.
D20	Orange	LTSSM has completed electrical Detect state and made it to Polling state (TS1, TS2, etc.).
D21	Green	PLL locked to PCI Express 100MHz clock
D22	Blue	Segment K of the GUI 16-segment display. Negative logic: on: bit=0, off: bit=1.
D5	Green	Done
D2	Red	Init
D4	Red	Program
D3	Red	Reset

Table 3. Normal Operation

D15 (top)	Red/blinking
D16	Orange
D17	Green
D18	off
D19	Red
D20	Orange
D21	Green
D22	Blue
D5	Green
D2	off
D4	off
D3	off

Default Switch Settings

SW1 – Controls SPI flash programming (D=down, U=up).

1	2	3	4	5	6	7	8	9	10
D	D	U	D	U	D	D	D	D	D

SW4 - on back side of board, user-selectable for demo DIP switch reading.

Default Jumper Settings

J5	1-2
J7	2-3
J19	1-2
J21	Jumper Installed
J26	1-2
J27	Jumper Installed

Appendix B. LatticeSC PCI Express x4 or x8 Evaluation Boards

Figure 24. LatticeSC80 PCI Express x8 Evaluation Board

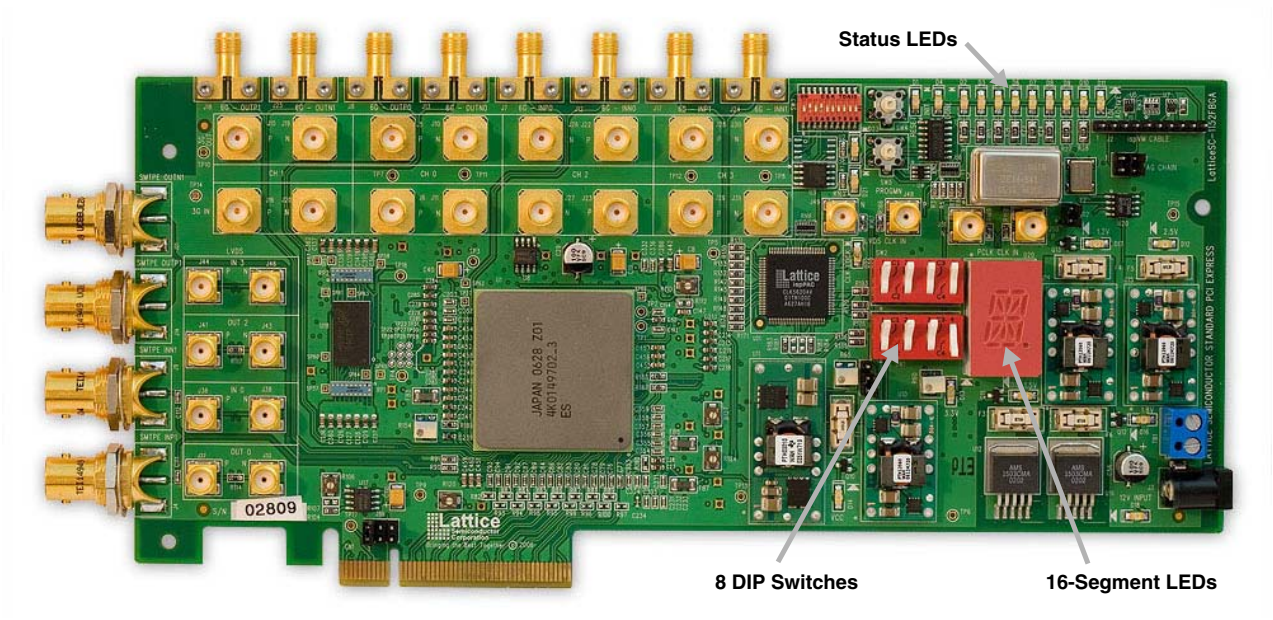
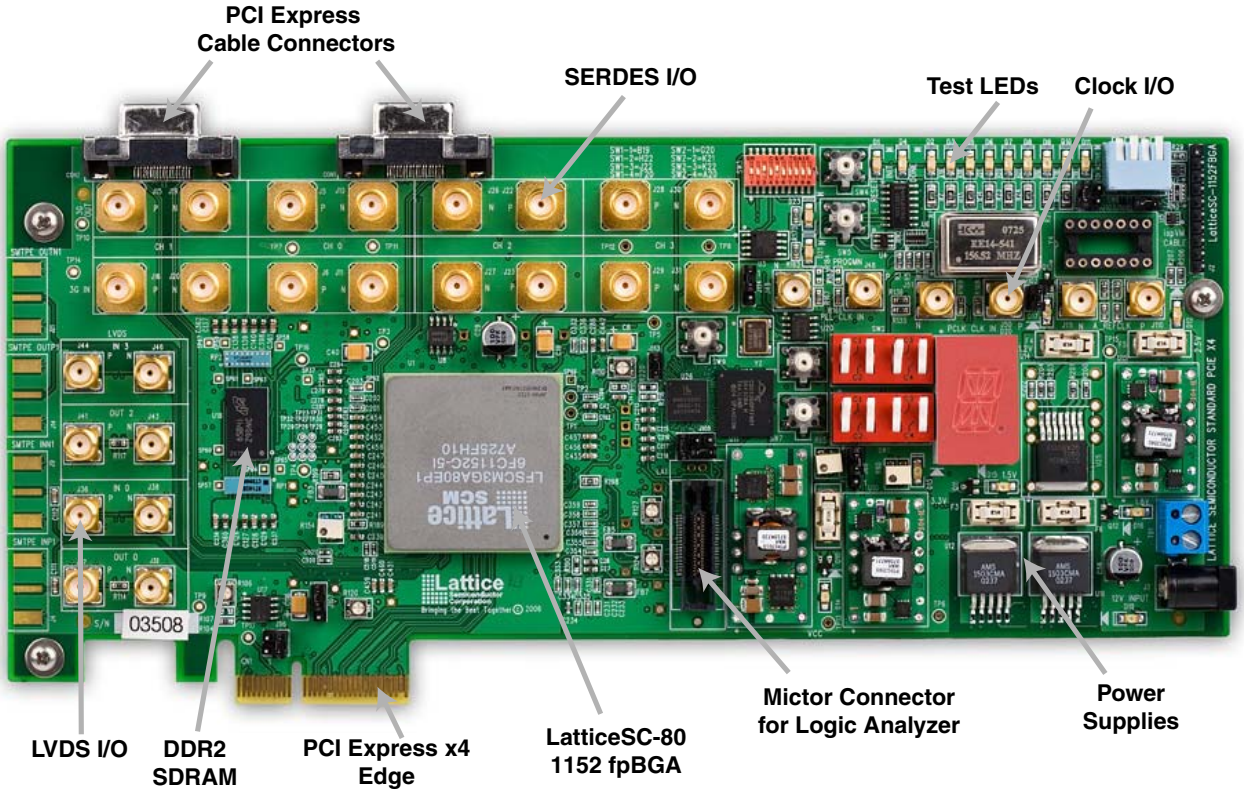


Figure 25. LatticeSC80 PCI Express x4 Evaluation Board



The LatticeSC80 board has a 16-segment LED display that can be written to by the demo application. The board also has eight DIP switches. The states of these DIP switches are read by the PCI Express demo software and dis-

played to the user. The Status LEDs are set by the application IP to indicate the states of the PCI Express IP and link.

The LatticeSC80 x8 board has a physical PCI Express x8 connector. Electrically it is wired to eight FPGA SERDES. It has the potential operate in x1, x4 or x8 PCI Express mode. Currently the LatticeSCM MACO PCI Express IP core only supports x1 and x4 modes. A Presence jumper must be set to x1 or x4 to match the intended the operating link width. Since all eight lanes are physically connected to SERDES, the root complex detects all eight lanes during the detect stage. There is potential for the root complex to become confused by detecting all eight lanes electrically, but the board is loaded with a bitstream that supports only x4 PCI Express operation. To avoid this situation, a x4 adapter is used with the LatticeSC80 board to make it appear electrically as a x4 board. The PC root complex then only detects 4 lanes and operation continues as a x4 link.

The previous discussion does not apply to the LatticeSC80 x4 board, since it already has a x4 connector.

The same situation is true for operation in x1 mode. If a bitstream is loaded that only supports x1 PCI Express mode, then the x1 adapter needs to be installed so the board electrically appears as if it only has one PCI Express lane, and the other lanes are not detected.

When the LatticeSC80 board is used with the x1 adapter, it can be installed in any size slot in a PC. According to the PCI Express specification, all slots must support the ability to fall back to x1 mode. When the LatticeSC80 board is used with the x4 adapter it physically will only fit into x4 or larger slots. There is a potential for a root complex to not support x4 mode in a x8 or x16 slot. The root complex could decide that since the board is not the native size (board links not equal to slot links) it will fall back all the way to x1 and not an intermediate stage (i.e., x4). This potential issue most likely would arise in x16 graphics slots where the PC BIOS expects a x16 (or x8), only sees a x4 and falls back to a x1. In such a case, the demo software will work normally. This shows one of the strong points of PCI Express: the ability to dynamically adapt to lane size without affecting the transport layer.

In summary, for currently available x1 and x4 demonstrations, an adapter is always required when using the LatticeSCM80 PCI Express x8 board. A x4 adapter is required for use with bitstreams that support x4 mode, or a x1 adapter can be used with any bitstream.

For more information on the operation of LatticeSC80 board, please refer to the *LatticeSC PCI Express x8 Evaluation Board User's Guide* for the board, available at: www.latticesemi.com/boards.

LED Definitions

The Status LEDs on the LatticeSC PCI Express x8 Evaluation Board are located horizontally along the top right edge of the board. The LEDs are in the following order and have the following functions:

Table 4. LED Order and Functionality

LED	Color	Usage
D1 (far left)	Red	Init
D4	Green	Done
D2	Red	Not used (off).
D3	Red	Not used (off).
D5	Yellow	PLL locked to PCI Express 100MHz clock.
D6	Yellow	LTSSM has completed electrical Detect state and made it to Polling state (TS1, TS2, etc.).
D7	Green	L0 training sequences completed, PHY layer up and ready for flow control.
D8	Green	Data Link up, ready for packets at Transaction Layer (PCI enumeration of configuration registers).
D9	Blue	Not used (off).
D10	Blue	Not used (off).
D11	Green	JTAG activity.
16-Segment Decimal Point	Red	PCI Express access to IP on wishbone bus (EBR and registers). On=activity, off=bus accesses.

Table 5. Normal Operation

D1	D4	D2	D3	D5	D6	D7	D8	D9	D10	D11
off	GRN	off	off	YLW	YLW	GRN	GRN	off	off	off

Default Switch Settings

SW1 – User-selectable for demo

SW2 – User-selectable for demo

SW3 – Controls SPI flash programming (D=down, U=up)

1	2	3	4	5	6	7	8	9	10
D	D	U	D	U	D	D	D	D	D

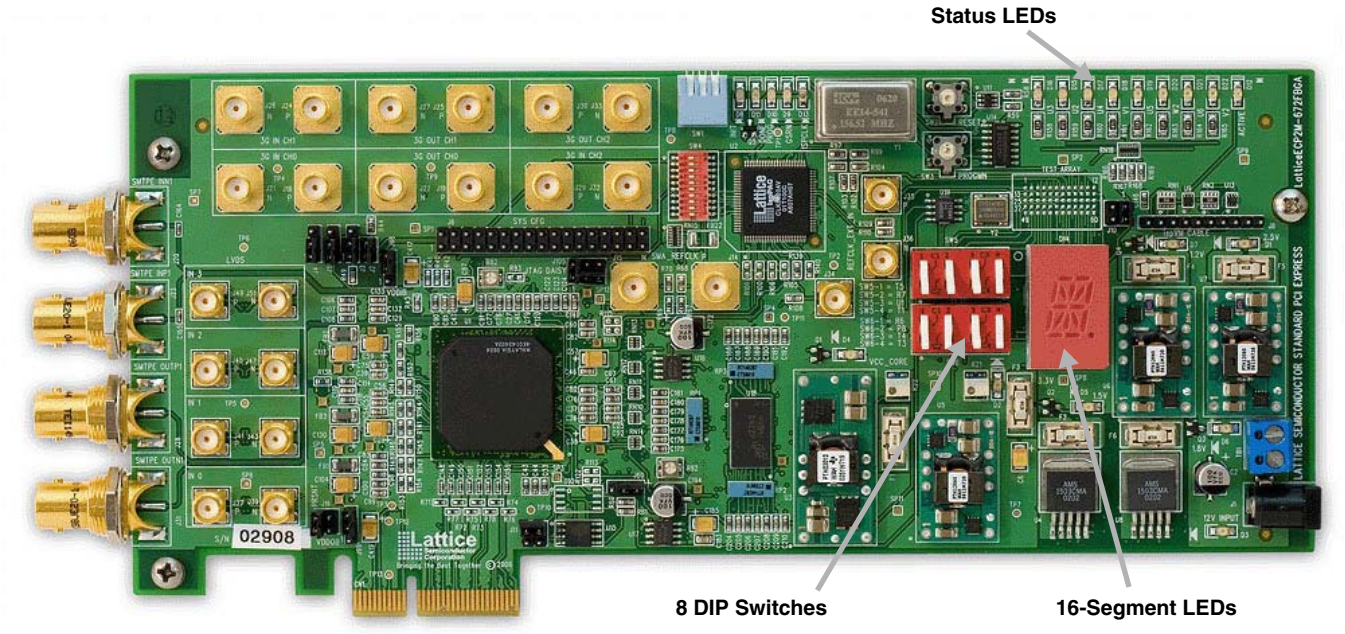
SW8 - On back side of board, all down (off)

Default Jumper Settings

J60	1-2 (down)
J93	3-4 (right)
J96	1-2 for x1 Mode, 3-4 for x4 Mode
J102	Jumper Not Installed

Appendix C. LatticeECP2M PCI Express x4 Evaluation Board

Figure 26. LatticeECP2M PCI Express x4 Evaluation Board



The LatticeECP2M35 and LatticeECP2M50 PCI Express x4 evaluation boards are very similar to the LatticeSC80 PCI Express x8 evaluation board. Both boards include the 16-segment LED display and the DIP switches.

The LatticeECP2M35/50 board has a physical PCI Express x4 connector. Electrically it is wired to four FPGA SERDES. It has the potential to operate in x1 or x4 PCI Express mode. The Lattice ECP2M PCI Express IP can support both x1 or x4 mode. A Presence jumper must be set to x1 or x4 to match the intended the operating link width. Since all four lanes are physically connected to SERDES, the root complex detects all four lanes during the detect stage. There is potential for the root complex to become confused when it sees four electrical lanes, but the board is loaded with a bitstream that supports only x1 PCI Express operation. To avoid this situation, a x1 adapter is used with the LatticeECP2M to make it appear electrically as a x1 board. The PC root complex then only detects 1 lane and operation continues as a x1.

If a bitstream is loaded that support x4 operation, a x1 adapter can also be used to force the board to operate as a x1.

When the LatticeECP2M board is used with the x1 adapter, it can be installed in any size slot in a PC. All slots must support the ability to fall back to x1 mode. When the LatticeECP2M board is used without the x1 adapter it physically will only fit into x4 or larger slots. There is a potential for a root complex to not support x4 mode in a x8 or x16 slot. The root complex could decide that since the board is not the native size (board links not equal to slot links) it will fall back all the way to x1 and not an intermediate stage (i.e., x4). This potential issue most likely would arise in x16 graphics slots where the PC BIOS expects a x16 (or x8), only sees a x4 and falls back to a x1. In such a case, the demo software will work normally. This shows one of the strong points of PCI Express: the ability to dynamically adapt to lane size without affecting the transport layer.

In summary, for currently available x1 and x4 demonstrations, a x1 adapter is always required when using the LatticeECP2M PCI Express board for x1 operation.

For more information on the operation of this board, please refer to the *LatticeECP2M PCI Express x4 Evaluation Board User's Guide,* available at: www.latticesemi.com/boards.

LED Definitions

The Status LEDs on the LatticeECP2M PCI Express x4 Evaluation Board are located horizontally along the top right edge of the board. The LEDs are in the following order and have the following functions:

Table 6. LED Order and Functionality

LED	Color	Usage
D16 (far left)	Red	CDR lock
D15	Red	RxValid status
D17	Yellow	PLL locked to PCI Express 100MHz clock.
D18	Yellow	Not used (off).
D19	Green	L0 training sequences completed, PHY Layer up and ready for flow control.
D20	Green	Data Link up, ready for packets at Transaction Layer (PCI enumeration of config registers).
D21	Blue	X4 Link
D22	Blue	Not used (off).
D12	Green	JTAG activity (negative logic - off when JTAG access).
16-Segment Decimal Point	Red	PCI Express access to IP on wishbone bus (EBR and registers). On=activity, off=bus accesses.

Table 7. Normal x4 Operation

D16	D15	D17	D18	D19	D20	D21	D22	D12
RED	RED	YLW	off	GRN	GRN	BLUE	off	GRN

Table 8. Normal x1 Operation

D16	D15	D17	D18	D19	D20	D21	D22	D12
RED	RED	YLW	off	GRN	GRN	off	off	GRN

Default Switch Settings

SW1 – All ON, (in towards circuit board).

SW4 – All OFF, (towards left side).

SW5 – All down to boot, once running user selectable for demo.

SW6 – All down to boot, once running user selectable for demo.

Default Jumper Settings

J2	1-2
J3	1-2
J4	1-2
J5	1-2
J10	1-2 (Right Pair)
J11	Top Pair
J16	1-2 (Top, Across); Presence x1 Mode
J60	2-3 (Right)
J98	2-3
J99	2-3
J105	1-2, 4-6