



SMPTE SDI Demo

User's Guide

Introduction

Video and television technology has been migrating from analog to digital over the past two decades. The technology used for transmitting data between digital systems has also been migrating from parallel to high-speed serial over the past decade. The SDI video standard is an uncompressed digital video standard that transmits high speed serial video stream through a coaxial cable.

Once video is captured by a professional video camera, no matter if it is pre-stored in a media or not, it must go through a few broadcasting systems before reaching consumers. SD-SDI and HD-SDI are common video standards used in these professional/broadcasting systems. With SDI, the high resolution video stream can be transmitted through a 75 Ohm coaxial cable for as long as several hundreds meters.

This user's guide shows the capability of LatticeECP2M's SERDES with an SD/HD-SDI design example. The design is implemented using the LatticeECP2M™ SMPTE video evaluation board. It includes a pattern generator and a pattern checker along with the Lattice's Multi-Rate SDI PHY IP core. The IP core supports automatic detection between the 270 Mbps SD-SDI video standards and the 1.485 Gbps HD-SDI video standards.

Features

- Supports two SD-SDI formats and eight HD-SDI formats
- Support video standards with M (1.001) factor that allows the frame rate to be 59.94 Hz, 29.97 Hz, and 23.98 Hz for upwards compatible with existing NTSC system
- Automatic detection between different video formats with the multi-rate feature of the IP core
- Color adjustment function for tuning Contrast/Brightness/Hue/Saturation in Pass-Through mode
- Color bars generation supports three types of color bars: SMPTE color bars, 75% color bars and 100% color bars
- Pathological signal analysis with three different test patterns: Matrix SDI check-field, EQU SDI check-field and PLL SDI check-field
- 16-segment LED for displaying which pathological patterns the generator and the checker is currently using
- Built-in pattern checker for tests with color bar patterns or pathological signal patterns using single or multiple boards
- Detailed pattern-checking errors reported through a UART port for capturing overnight test results (RS-232 port set to 115200, 8, 1, N)
- Character LCD module for displaying Rx/Tx status, video standards, current operational mode, Contrast/Brightness/Hue/Saturation values and control settings
- Seamless switching between video standards that guarantees the switching is between frame boundaries

Functional Description

This design supports two operational modes, Pass-Through mode and Pattern-Generation mode. The mode switching and the controls of these two modes are done by the on-board switch and push-buttons.

When in Pass-Through mode, the serial video stream is received, descrambled and word-aligned by the IP core receiver. Then, the Contrast/Brightness/Hue/Saturation adjustment module can optionally process the received parallel video data. Finally, the parallel video data is sent to the IP core transmitter for data scrambling, line number insertion and CRC insertion before being sent out.

When in Pattern-Generation mode, an internal pattern generator will generate patterns for the IP core transmitter to send out color bars or pathological signals. The receiver can also be enabled in this mode for comparing the received video data with an internal pattern checker. The comparison errors will be sent out through a UART/RS-232 port and captured into a PC text file.

The video standards supported by the Multi-Rate SDI PHY IP core are all implemented in this design which include the two SD standards and the eight HD standards listed in Table 1.

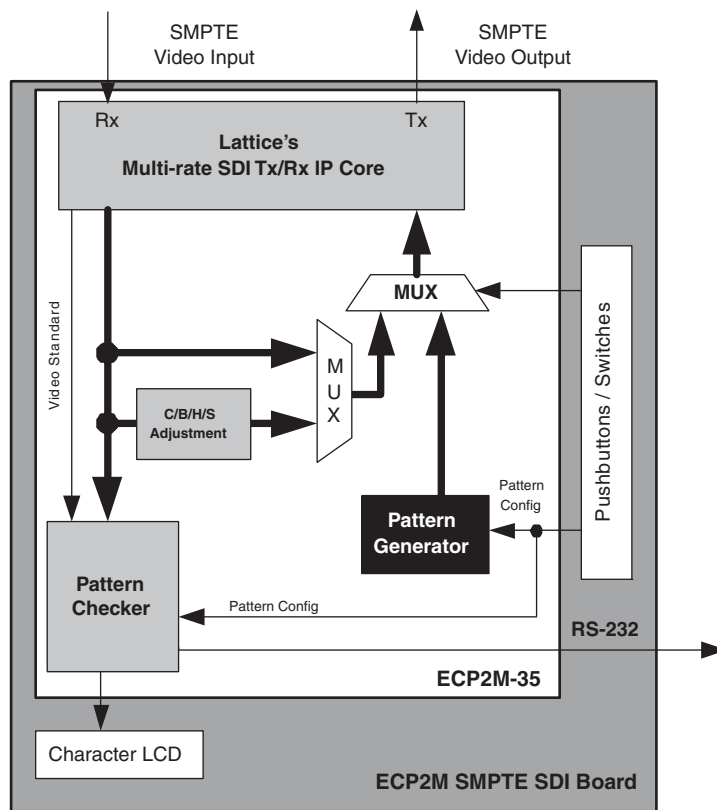
Table 1. Supported Video Formats and Corresponding Switch Settings

Standard	SD-SDI		HD-SDI												
Bit Rate	270Mbps		1.485Gbps												
Serial SMPTE Standard	259M		292M												
Parallel SMPTE Standard	125M		260M		295M	274M								296M	
SW6-[1:4]	0xx0	0xx1	1000	1000	1001	1010	1010	1011	1011	1100	1101	1110	1110	1111	1111
Total words per line	1716	1728	2200	2200	2376	2200	2200	2200	2200	2640	2640	2750	2750	1650	1650
Total lines per frame	525	625	1125	1125	1250	1125	1125	1125	1125	1125	1125	1125	1125	750	750
Active words per active line	720	720	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920	1280	1280
Active lines per frame	487i	576i	1035i	1035i	1080i	1080p	1080p	1080i	1080i	1080p	1080i	1080p	1080p	720p	720p
Frame rate (Hz)	30/M	25	30	30/M	25	30	30/M	30	30/M	25	25	24	24/M	60	60/M
Fields per frame	2	2	2	2	2	1	1	2	2	1	2	1	1	1	1
Bits per word	10	10	20	20	20	20	20	20	20	20	20	20	20	20	20
Word rate (MHz)	27	27	74.25	74.25/M	74.25	74.25	74.25/M	74.25	74.25/M	74.25	74.25	74.25	74.25/M	74.25	74.25/M
Pixel sample rate (MHz)	13.5	13.5	74.25	74.25/M	74.25	74.25	74.25/M	74.25	74.25/M	74.25	74.25	74.25	74.25/M	74.25	74.25/M

Note: When in Pattern-Generation mode, the video format is selected by SW6-1, SW6-2, SW6-3 and SW6-4. The video standard with factor M (equal to 1.001) is selected by SW5-2.

The functional block diagram of the demo is shown in Figure 1. The IP core has a feature to include the SERDES in the core. This reduces the effort of connecting signals between SERDES and the design logic and is used in this demo design.

Figure 1. Functional Block Diagram of the Design



The pattern generator shown in Figure 1 can generate different test patterns for all the 10 video formats. As shown in Figure 2, there is another instance of this pattern generator in the pattern checker module. The pattern generator

shown in Figure 1 is controlled by the on-board switches. However, depending on the operational mode, the pattern generator in the checker module may be controlled either by the on-board switches or the output signals of the IP core.

The block diagram of the pattern checker is shown in Figure 2. The Sync Control module monitors the parallel video data received by the IP core and releases the reset of the pattern generator at the exact right time so that the pattern generator can generate the data that is synchronized with the data received by the IP core. With that, the CMP comparator can compare the two data buses and registers the results in the Timer/FCNT module. The Timer/FCNT is a module that includes a 100-hour timer and a frame counter. The timer provides the timestamp for the tests. This timestamp can not be reset after power on. The frame counter counts the number of successfully passed frames before hitting a comparison error. When an error occurs, the time and the location of the mismatch in the video format will be reported. The LatticeMico8™ microprocessor in this design is used for sending out the design status onto the 20 characters x 2 lines LCD module. It also sends the test results through the UART to an external terminal. A personal computer with serial RS-232 port can be used to run the HyperTerminal application. By using the HyperTerminal's text capturing feature, the overnight or over-the-weekend test results can be stored in a text file.

Figure 2. Functional Block Diagram of the Pattern Checker

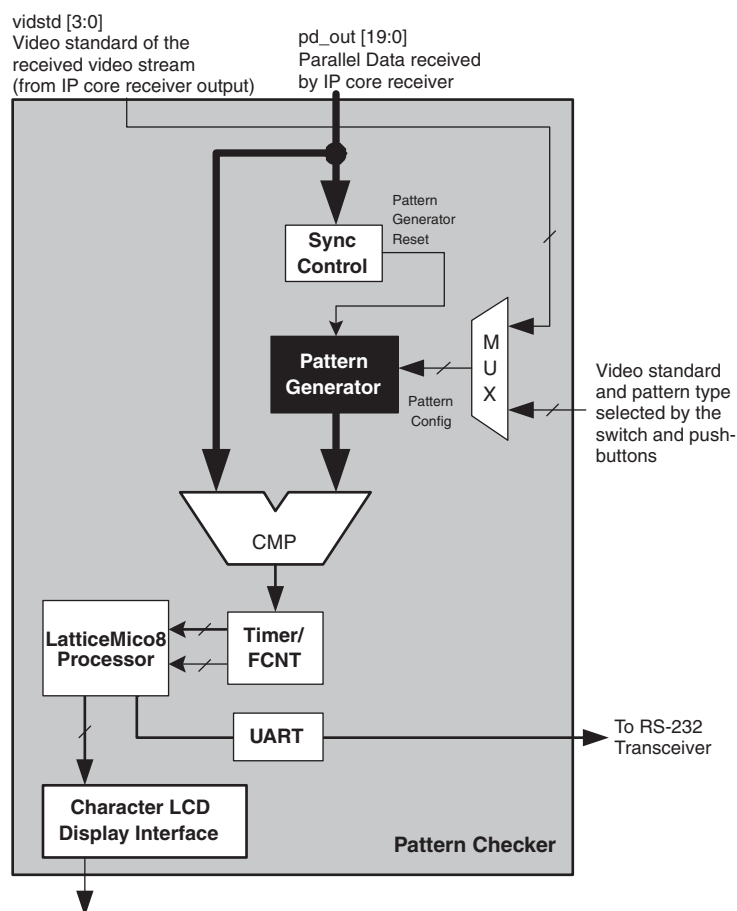


Figure 3 shows the basic data structure of a SDI video frame. It is similar to the timing format of the analog system. As seen in Figure 3, the progressive standard and the interlaced standard have different numbers of fields per frame. Other than that, the total lines per frame, the total words per line, and the sizes of the vertical/horizontal blanking periods are also different from one video format to another. Please refer to Table 1 for the actual numbers.

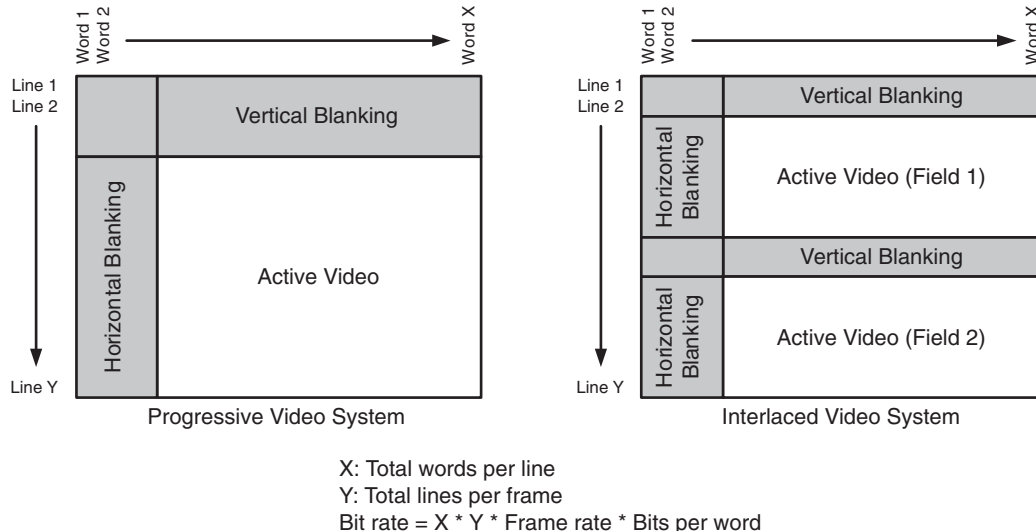
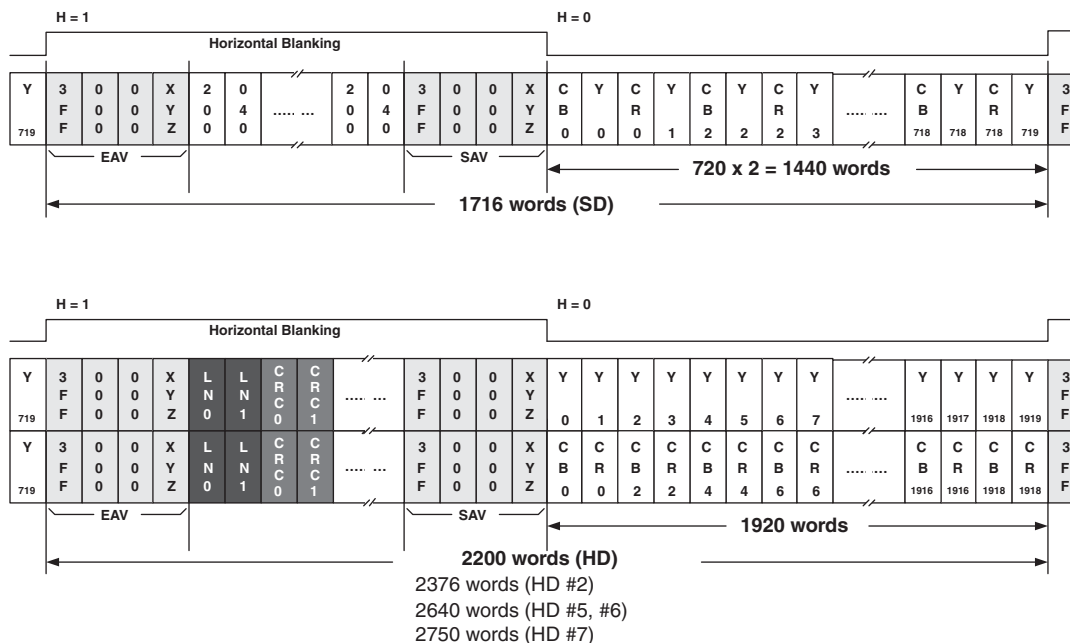
Figure 3. Basic Data Structure of the SDI Systems

Figure 4 shows some examples of the words in a line of the SD-SDI and the HD-SDI systems.

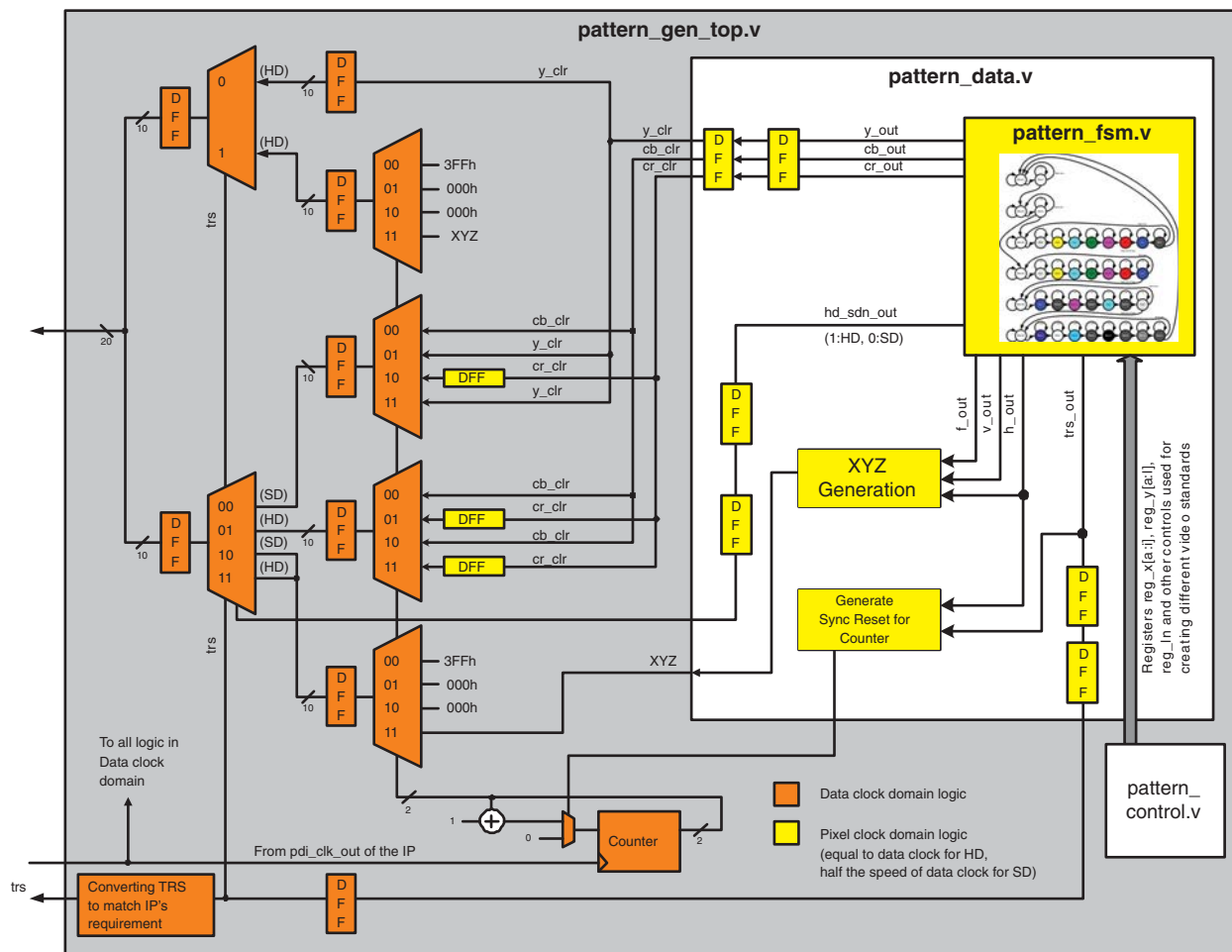
For the HD system, these data words are generated at the same clock frequency as the pixel clock. However, for the SD system, they are running at only half of the pixel clock frequency.

Figure 4. Examples of the Data Streams of the SDI Systems

Instead of using lookup tables for supporting the six different patterns of the ten different video standards, the pattern generators employ a finite state machine so that they can be easily configured from one to another. Figure 5 shows the block diagram of the pattern generator. The finite state machine is controlled by parameters stored in configuration registers, which can be updated with different values based on the standards and patterns selected by the switches. This is completed by the Pattern_Control module shown in the block diagram. The outputs of the finite state machine are the Y, Cb, Cr video pixel data and the field, vertical blank and horizontal blank information.

The field, vertical blank and horizontal blank are used for creating the XYZ word in the Color_Bar module. The Y, Cb and Cr outputs of the finite state machine are in YCbCr 4:4:4 format. Since the SDI video uses the YCbCr 4:2:2 format, the words will be converted to the YCbCr 4:2:2 format and restructured in the Color_Bar_Gen_top module before being sent out.

Figure 5. Block Diagram of the Pattern Generator



Video Clocking Scheme

This section describes the reference clocks used in the Rx side and Tx side SERDES. The SERDES reference clock can be sourced from either the external dedicated package pins or the internal FPGA fabric. The external dedicated refclk pins are shared for the SERDES within the same quadrant. Hence, if Rx and Tx need to use different reference clocks, they must come from different sources.

Since SD and HD are running at different bit rates, the reference clock for the IP core receiver will need to be adjusted accordingly for locking to either SD or HD bit rate. The IP core sends out the rx_hd_sdn output signal to inform the external logic which reference clock frequency is required for locking the incoming serial data. The design uses this output to generate the controls of the Gennum GS4911 clock generator. Whenever the GS4911 is set to its Free Run mode, its output frequency can be controlled through its VID_STD[5:0] inputs so that either 27MHz or 1.485MHz can be generated for SD and HD standards. That is equal to one-tenth and one-twentieth of the received SD and HD video stream bit rate respectively.

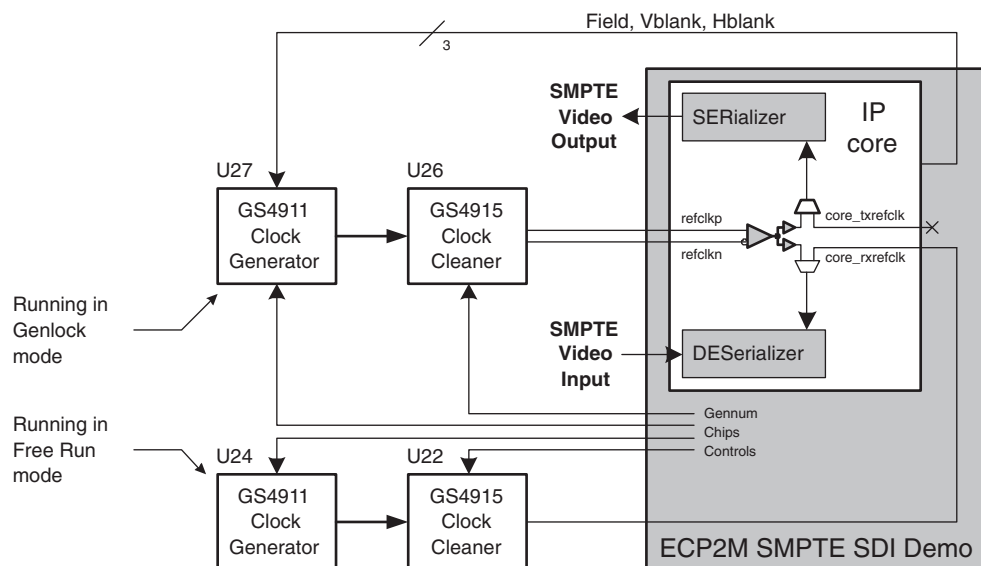
For Pass-Through mode, the Rx reference clock is used by the DESerializer for reference only and its frequency is okay to be slightly different from the DESerializer's recovered clock by a few PPM. This is because the DESerial-

izer's recovered clock is actually the clock used to recover the serial data. On the Tx side, however, the reference clock used by the SERIALIZER must be able to create a transmit clock that is exactly (0 PPM difference) the same frequency as the DESERIALIZER's recovered clock. Otherwise, a video frame buffer must be used for dropping or duplicating a frame when it is needed so that the Tx frame rate can still be slightly different from the Rx frame rate.

In order to provide a Tx reference clock that is GENLOCKed to the input video stream, the LatticeECP2M SMPTE SDI board uses GS4911's GENLOCK feature. When GS4911 is set to Genlock mode, it will generate a clock that is GENLOCKed to the Field, Vblank and Hblank reference signals provided to it. The IP core receiver will generate these signals when it is locked to the supported video standards. After genlocked to the input video stream, the GS4911's clock output will then be fed into Gennum's GS4915 clock cleaner to reduce the jitter. If not controlled, the jitter will migrate from the reference clock to the serial data output. A low jitter reference clock ensures the jitter on the SERIALIZER output to be controlled within the SDI's specification.

As seen in Figure 6, there are two instances of the Gennum's GS4911 and GS4915 chips on the board. The Rx side GS4911 and GS4915 are used for generating the Rx reference clock. This clock is connected to a general purpose I/O of the LatticeECP2M, then routed to the DESERIALIZER through the FPGA fabric. After the DESERIALIZER recovers the data of the video input stream and locks to a supported video standard, the IP core receiver will create the Field, Vblank and Hblank output signals based on the data it received. These signals are used by the Tx side GS4911 to generate a precise clock that is GENLOCKed to the video input stream. After this clock is cleaned by the Tx side GS4915, the GS4915's differential clock output will be connected to the SERDES's differential reference clock inputs and used by the transmitter.

Figure 6. Reference Clock in Pass-Through Mode



For Pattern-Generation mode, both the Rx side and Tx side Gennum chips are controlled by the design to generate the desired frequency. Both the Rx and Tx GS4911 are set to Free Run mode. The Genlock mode is not used. Since SD and HD are running at different bit rates, it is possible for the receiver, if not disabled, to use a different reference clock frequency than the one used for the transmitter. In this case, the Rx and Tx is locking to different bit rate. Figure 7 shows the clocking of the design when the Pattern-Generation mode is selected.

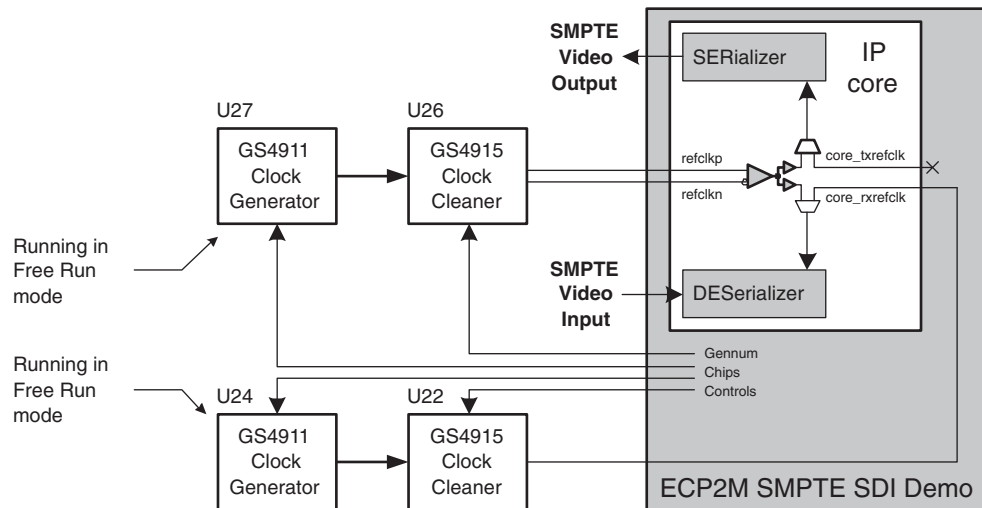
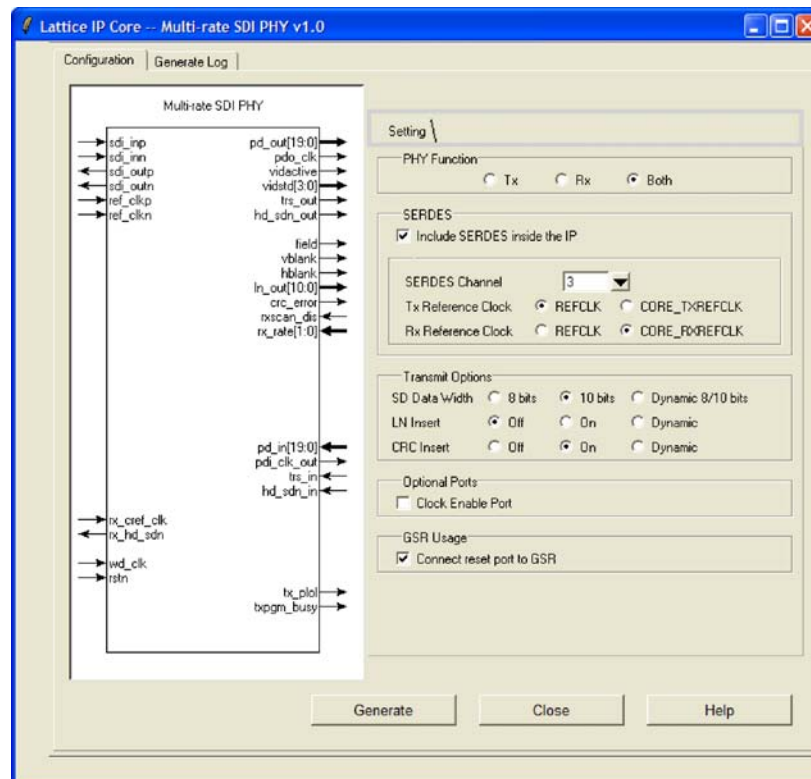
Figure 7. Reference Clock in Pattern-Generation Mode

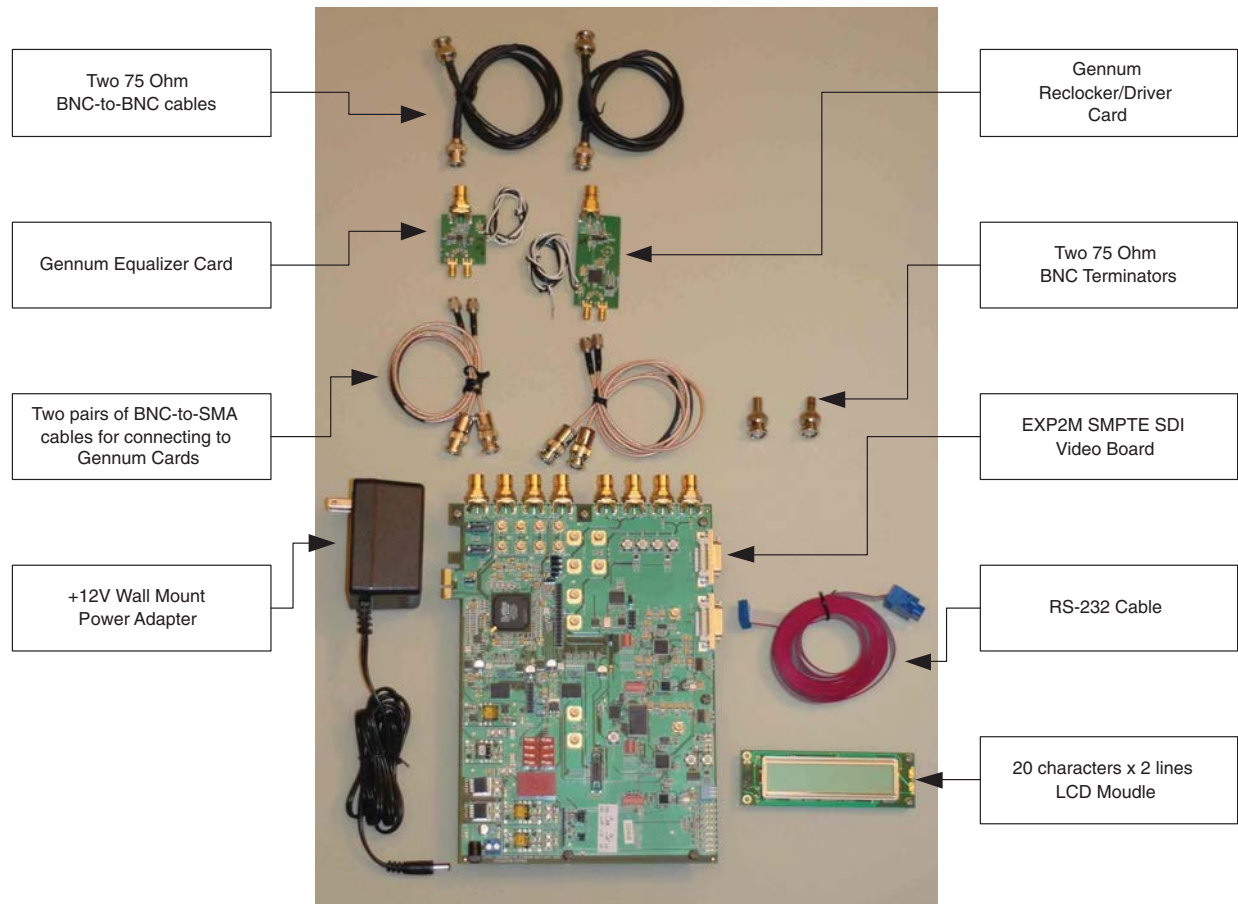
Figure 8 shows how the Rx reference clock is generated by CORE_RXREFCLK (from FPGA fabric) and the Tx reference clock is generated by the REFCLK (from external pins).

Figure 8. Multi-rate SDI PHY IP Core Generation

Demo Kit

This design uses Lattice SMPTE SDI Demo Kit which includes the items shown in Figure 9. To run the pathological signal test you will also need a computer equipped with a RS-232 serial communication port.

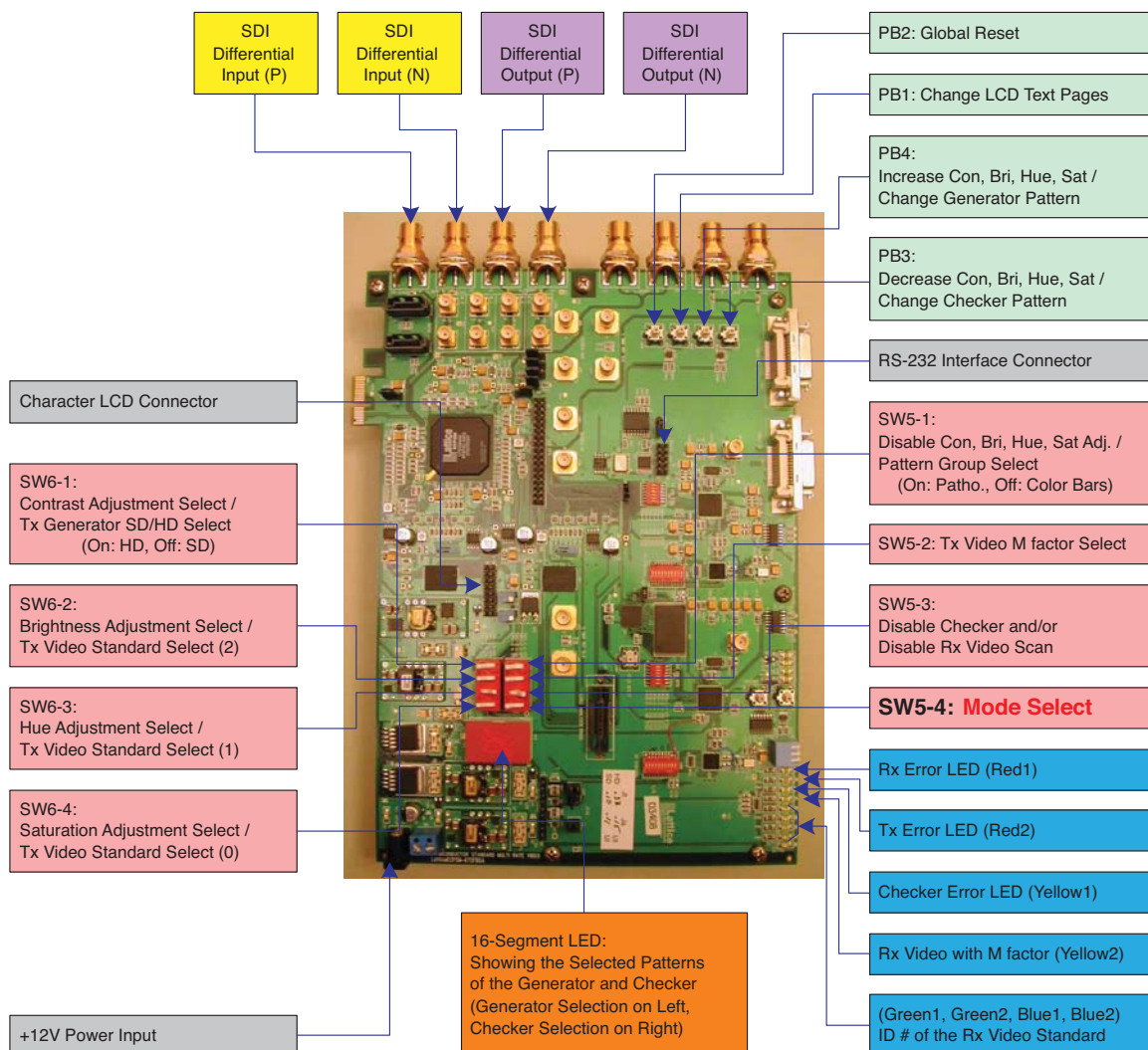
Figure 9. Items Included in the Demo Kit



Demo Settings

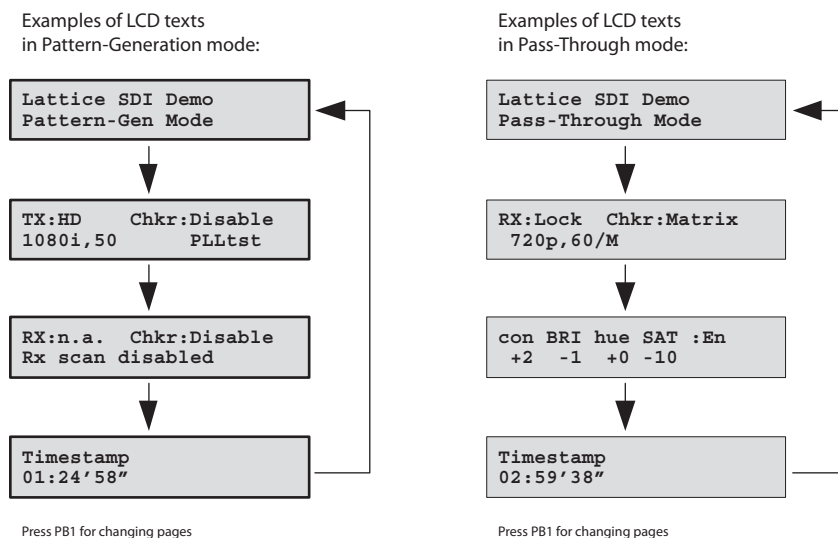
To run this demo, you will need to connect cables, adjust switches, press push-buttons and monitor the LEDs. Figure 10 lists the functions of the connectors, switches, push-buttons and LEDs that are used in the demo. Since the demo design is controlled by the limited number of switches and push-buttons, many of these switches and push-buttons have dual functions depending on the mode of operation.

There are two 4-position SPST switches, SW5 and SW6, on this board used for the demo controls. The most important one is in position #4 of SW5, which is designed as SW5-4 in this document. SW5-4 is used to select the mode of operation of this demo. The setting of SW5-4 determines the functions of the other switch positions and the push-buttons. The demo settings are controlled by push-buttons PB1, PB2, PB3 and PB4 and switches SW5 and SW6. The following sections include detailed descriptions of these switches, push-buttons and LEDs in the two operational modes.

Figure 10. Functions of the Connectors, Push-buttons, Switches and LEDs

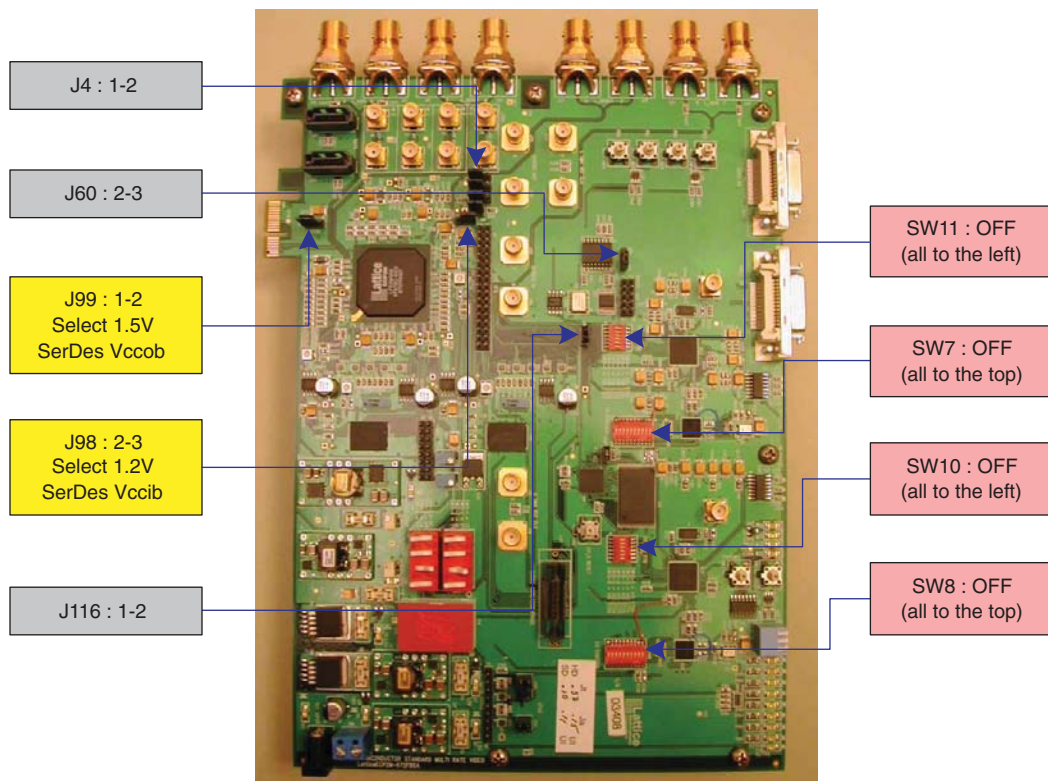
There is a 20 characters by 2 lines LCD module provided with this demo kit. It needs to be installed on J126. If it is not installed, please refer to the photos in this document for the installation. The LCD can display four different pages of contents. The texts of these pages are different for Pass-Through Mode and Pattern-Generation Mode. Whenever the SW5, SW6 switches or the push-buttons are adjusted, the LatticeMico8 processor will sense the adjustment and then turn the page to the related page.

When in Pattern-Generation Mode, these pages are (1) Current Mode, (2) Tx Status (3) Rx Status and (4) Timestamp After Power On. When in Pass-Through Mode, these pages are (1) Current Mode, (2) Rx Status (3) Contrast/Brightness/Hue/Saturation Values and (4) Timestamp After Power On. Figure 11 shows the examples of these pages. You can also change the displayed pages by pressing the push-button PB1.

Figure 11. Examples of LCD Texts in Different Operational Mode

Default Settings of Other Switches and Jumpers

Other than SW5 and SW6, there are other mini switches and several jumpers on the board that will affect the demo. These mini switches and jumpers need to be set to their default state to run this demo properly. The mini switches are on SW7, SW8, SW10 and SW11. These switches are connected to the controls of the on-board Gennum clock chips. They all need to be set to the OFF state, i.e. the side with the numbers. These controls will be done by the logic inside the FPGA instead. The locations of these mini switches and jumpers, along with their default settings, are shown in Figure 12. Please refer to the User's Guide of the board for the functions of these mini switches and jumpers.

Figure 12. Default Settings of Mini Switches and Jumpers

Using the Gennum Equalizer and Reclocker/Driver Cards

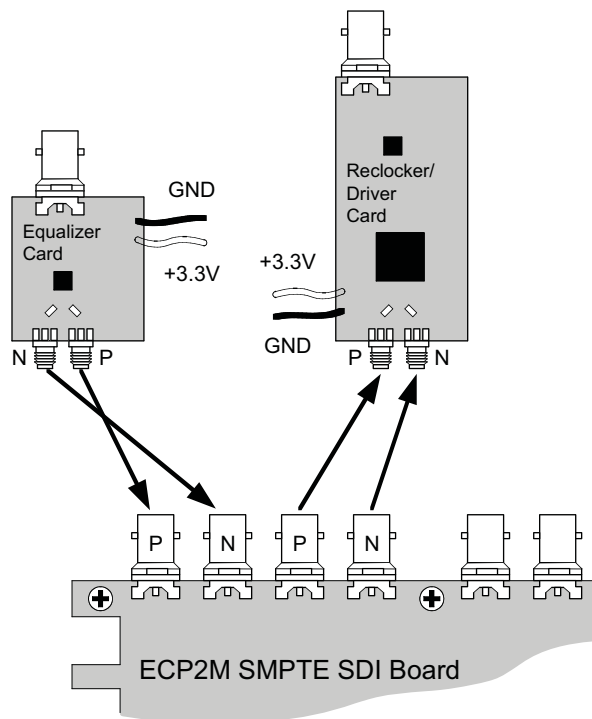
This kit comes with two Gennum cards. When it is necessary to connect the SDI through the very long 75 Ohm SDI cable, the use of a SDI equalizer and SDI driver is recommended. The equalizer card is used on the receiver side and the driver card is used on the transmitter side. The Gennum driver card also includes a Gennum reclocker chip, which can optionally be bypassed.

Both Gennum cards are soldered with two wires. These wires are used for providing 3.3V power to the cards. The voltages of these wires should be:

- White wire: +3.3V
- Black wire: Ground

Both Gennum cards have two SMA connectors and one BNC connector. The BNC connector is the connector for the single-ended SDI signal. The SMA connectors are for the differential signals that need to be connected to the LatticeECP2M SMPTE SDI board. Figure 13 shows the locations of the SMA connectors and which connectors they need to be connected to on the LatticeECP2M SMPTE SDI board. The two pairs of BNC-to-SMA cables are used for the connections.

Figure 13. Connections Between Gennum Cards and LatticeECP2M SMPTE SDI Board



Running the Demo in Pattern-Generation Mode

When in Pattern-Generation mode, the design can create data patterns for color bars as well as the pathological signal tests.

The patterns generated by the pattern generator are divided into two groups. The color bars group supports three different color bars types - SMPTE, 75% and 100% color bars. The pathological test group supports Matrix check-field, EQU check-field and the PLL check-field. As seen in Table 2, push-buttons PB3, PB4 and SW5-1 are used to select the color bars types or the pathological test patterns.

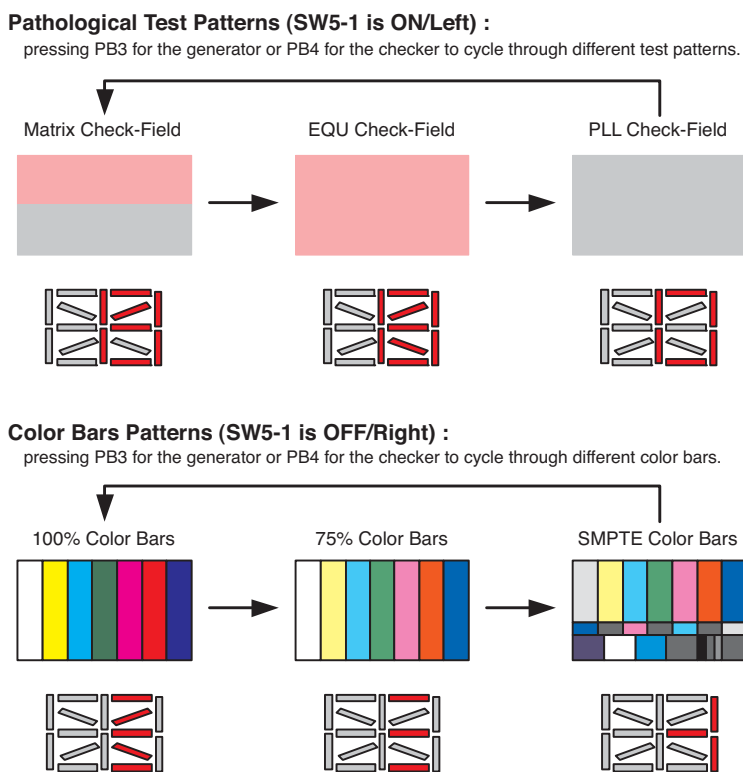
For video mode selection, SW6-1 is used to select either SD or HD standards; SW6-2, SW6-3 and SW6-4 are used to select the specific format of the SD/HD standard; while SW5-2 is used to select the M factor if applicable. The settings and the corresponding video formats are shown in both Table 1 and Figure 15.

When in the Pattern-Generation Mode, both the pattern generator and the pattern checker are available. The pattern checker is used for checking the received video pattern in the loopback test. It can be disabled by SW5-3. When in Pattern-Generation mode, the checker pattern can be set to either color bars or the pathological test patterns. Figure 14 shows how the screen will look like when these patterns are selected. The 16-segment LED is used to display what pattern is currently selected. The corresponding 16-segment LED patterns are also shown in Figure 14. If the board is rotated to the orientation shown in this document, the left side of the 16-segment LED is used for displaying the pattern currently selected for the pattern checker, while the right side is for displaying the pattern currently selected for the pattern generator. If the checker is disabled by SW5-3, the left side of the 16-segment LED will be off.

Table 2. Switches for Color Bars Generation

SW5-1	Selected Pattern Group	Changing Pattern by Pushing PB3 (for Generator) or PB4 (for Checker)
OFF(Right)	Pathological Test	Matrix --> EQU --> PLL
ON(Left)	Color Bars	100% --> 75% --> SMPTE

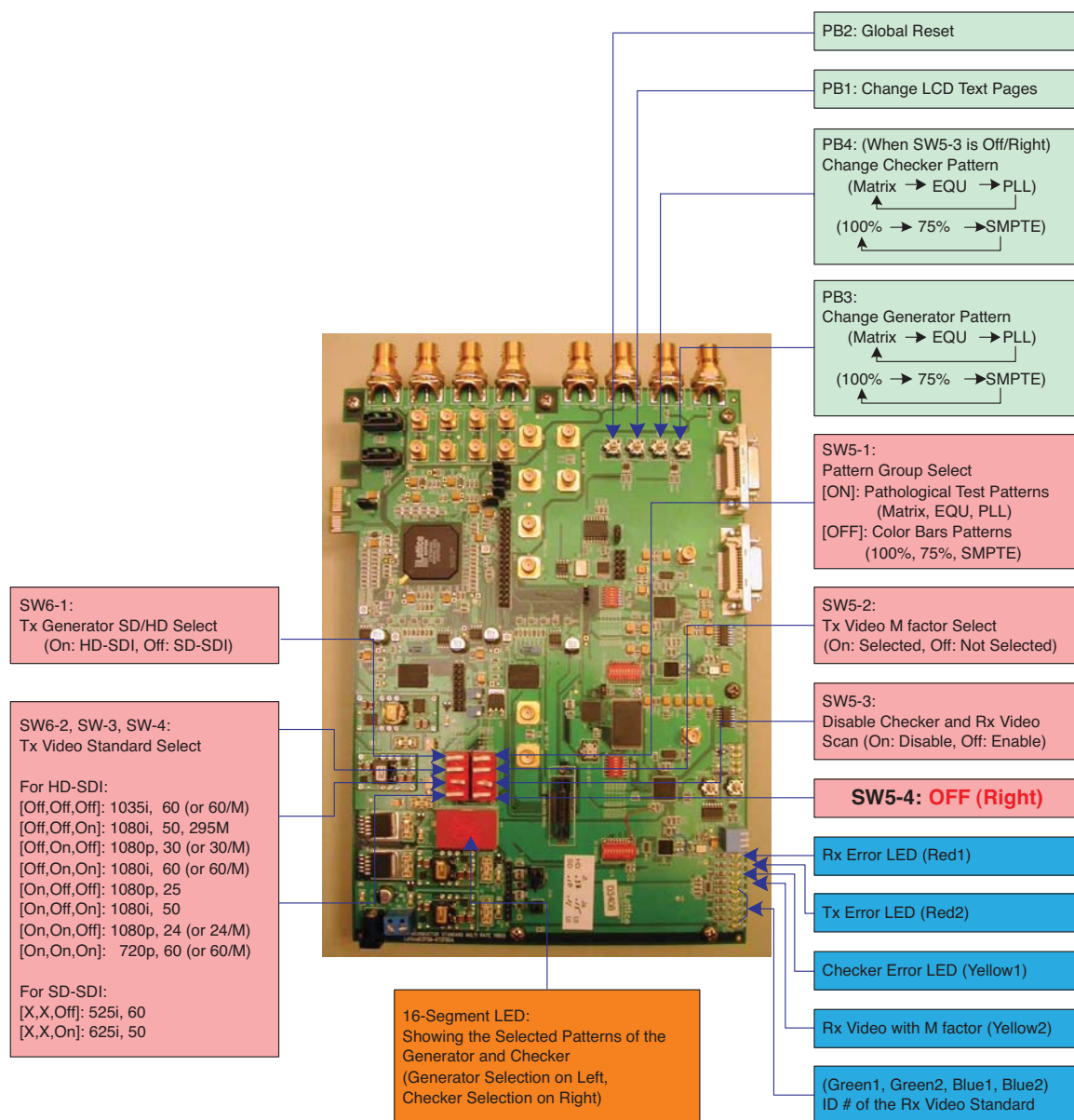
Figure 14. Pathological Signal Test Patterns on Screen



Note:
The 16-segment LED showing above are for the status of the pattern generator. The left side of the 16-segment LED is used for displaying the pattern currently selected for the pattern checker. When the checker is disabled by turning SW5-3 is ON (left), the left side of the 16-segment LED is off as shown above.

The push-button and switch controls as well as the LEDs function in Pattern-Generation Mode are shown in Figure 15. The pattern generator and the pattern checker can be enabled simultaneously in the Pattern-Generation mode. SW5-3 is used to turn the pattern checker off. When it is turned off, Rx scanning is also disabled. When Rx scanning is disabled, no video stream will be received by the receiver.

Figure 15. Pattern-Generation Mode Settings



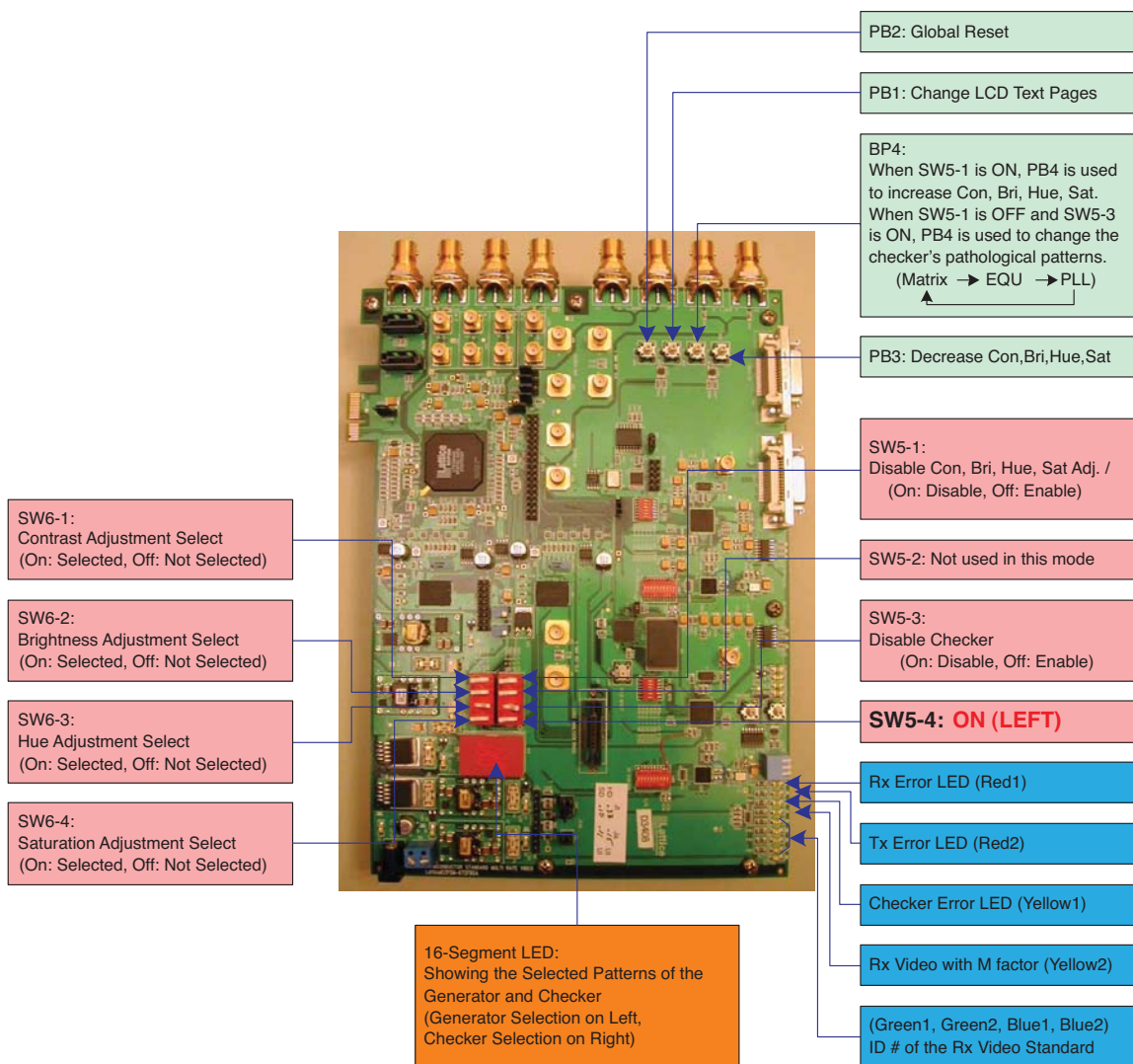
Running the Demo in Pass-Through Mode

For running the demo in Pass-Through Mode, SW5-4 needs to be turn on (left). When in this mode, the Contrast/Brightness/Hue/Saturation adjustment video processing module can be used to adjust the received video before passing it through the Tx. The SW5-1 control the MUX that provides the parallel video data stream to the IP core transmitter. When SW5-1 is ON, the C/B/H/S adjustment module is bypassed and the original parallel video data stream received by the Rx is selected. When SW5-1 is OFF, the video data stream after the C/B/H/S adjustment is selected. This Contrast/Brightness/Hue/Saturation adjustment module, which includes 20 steps of adjustment from -10 to 0 to +10, is modified from the one used in RD1030, *LatticeXP2* and *LatticeECP2/M 7:1 LVDS Video Interface* reference design. The modification is required to address the sampling format difference between the SMPTE's YCbCr 4:2:2 and the YCbCr 4:4:4 in the 7:1 LVDS ChannelLink design. For more information about the design of this module, please refer to the RD1030 document.

When running in Pass-Through Mode, the pattern generator will be forced to disable by the design. However, the pattern checker is still available for checking the incoming pattern and report errors if it finds any differences. The SW5-3 is used to disable the pattern checker if it is not required. In Pass-Through Mode, the pattern checker can check the incoming pattern with pathological test patterns only. They can only be either Matrix check-field, EQU check-field or PLL check-field, but cannot be the color bars as in Pattern-Generator mode. Push-button PB4 is used to select these test patterns. When using PB4 to select these test patterns, the SW5-1 must be turned ON to disable the C/B/H/S adjustment. Otherwise, pushing PB4 will increase the C/B/H/S selected by the SW6-1, SW6-2, SW6-3 and SW6-4 instead.

The push-button and switch controls as well as the LEDs in Pass-Through Mode are shown in Figure 16.

Figure 16. Pass-Through Mode Settings



Cable Connections

The demo kit includes two different types of cables, the 75 Ohm BNC-to-BNC cable and the 50 Ohm BNC-to-SMA cable. The SDI is a standard using the 75 Ohm single-ended cable. Therefore, you should use the 75 Ohm cable for connecting to other SDI devices. However, since the SDI input and output on the ECP2M SMPTE SDI board are differential signals with 75 Ohm impedance, when you are connecting the single-ended SDI signal from other SDI device to this board, you need to connect the 75 Ohm terminator to the N input (J21) or N output (J22). The 50 Ohm BNC-to-SMA cables are used for connecting the board's SDI output to the Gennum Reclocker/Driver Card or connecting the Gennum Equalizer Card to the board's SDI input.

Figure 17 shows the connections that uses a waveform generator to generate SDI signal and a waveform monitor to capture the video. The Gennum Cards are also used in the setup so that very long cable can be used. The design is set to Pass-Through Mode. The data path is also showing in Figure 17. The CBHS adjustment is optional in this mode. The pattern checker can also be turned on if the waveform generator is generating Matrix check-field, EQU check-field, or PLL check-field test patterns.

Figure 17. Connections Using External Video Source/Sink and Gennum Cards

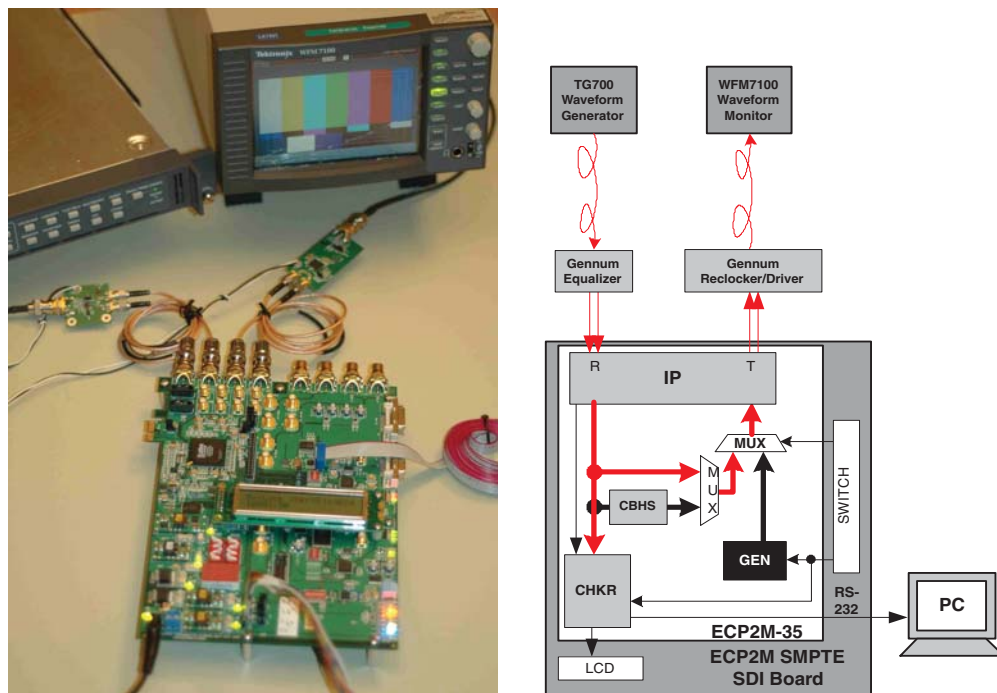


Figure 18 shows the connections that also uses a waveform generator to generate SDI signal and a waveform monitor to capture the video, but the Gennum Cards are not used. The design is set to Pass-Through Mode. Since Gennum Cards are not used, the 75 Ohm terminators need to be connected to the N connectors of the input and output.

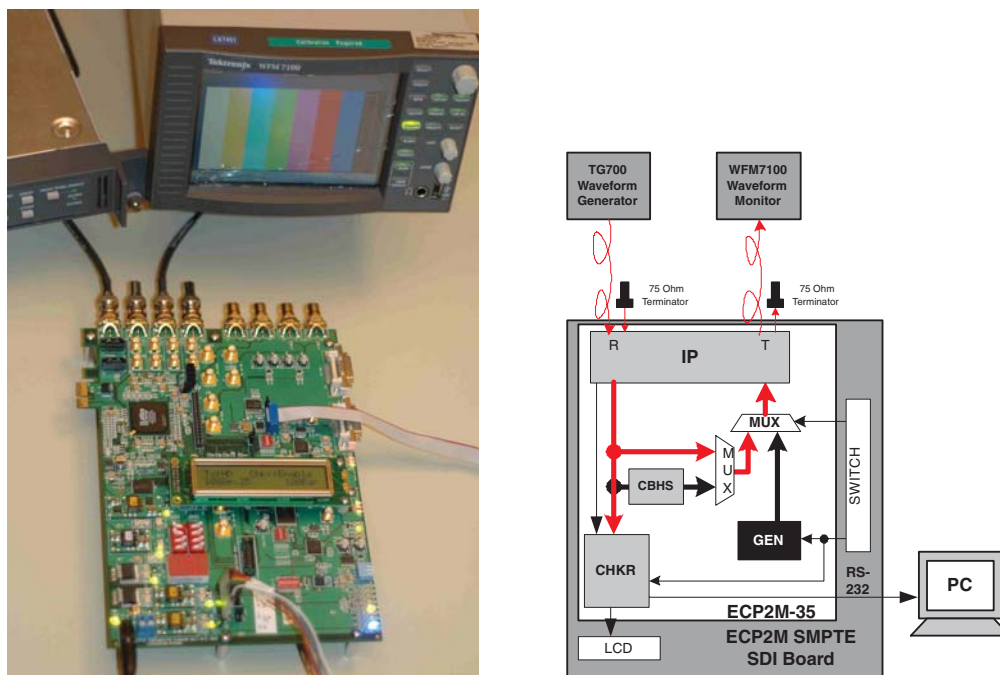
Figure 18. Connections Using External Video Source/Sink without Gennum Cards

Figure 20 shows the connections of a loopback pathological signal test that uses the Gennum Cards. The design is set to Pattern-Generation Mode with Pattern Checker turned on. The data path is also shown in Figure 20. Since the Pattern Generator and the Pattern Checker can be set to different pathological check-field test patterns, please make sure they are set to the same test patterns, otherwise you will see the orange pattern-checking error LED flashing and the detailed error reported through the UART/RS-232 port. To monitor the detailed test results, set the RS-232 port to 115200 bps, 8 data bits, 1 stop bit, no parity bit and no flow control. Figure 19 shows an example of the test results captured by the HyperTerminal application. When the test is running without errors, the DP (Decimal Point) of the 16-segment LED will be flashing. This DP-segment is connected to one of the bits of the FCNT frame counter. The FCNT is used to count how many frames are compared without errors. The flashing of DP-segment indicates the testing is running good. In the Pattern-Generation Mode, the color bars patterns can also be used as test patterns. When the color bars patterns are selected for the loopback test, the 16 strip shape segments of the 16-segment LED will all be turned off. Since the YCbCr data of the color bars may be slightly different from test equipment to test equipment, you may see errors if you use an external waveform generator to generate the color bars and use the Pattern Checker to compare with whatever was received by the IP core receiver.

Figure 19. Example of the Test Results Captured by HyperTerminal

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Lattice SMPTE SD/HD-SDI Demo -- designed by J. Hsin 11/16/2007
Matrix 720p,60 00:00'01"03->08:07'19"29 Fram=01754242 ErrPLL Elaps=08:07'18"26
Matrix 720p,60 08:07'20"10->08:07'20"14 Fram=00000000 ErrTRS Elaps=00:00'00"00
Matrix 720p,60 08:07'20"94->15:10'09"94 Fram=01522092 Passed Elaps=07:02'49"00
Pattern Checker Disabled !!!
Matrix 720p,60 15:10'13"61->
Received Video Format or Pattern Changed !!!
Matrix 1080i,50 15:10'16"15->
Received Video Format or Pattern Changed !!!
EQUtst 1080i,50 15:10'22"69->
```

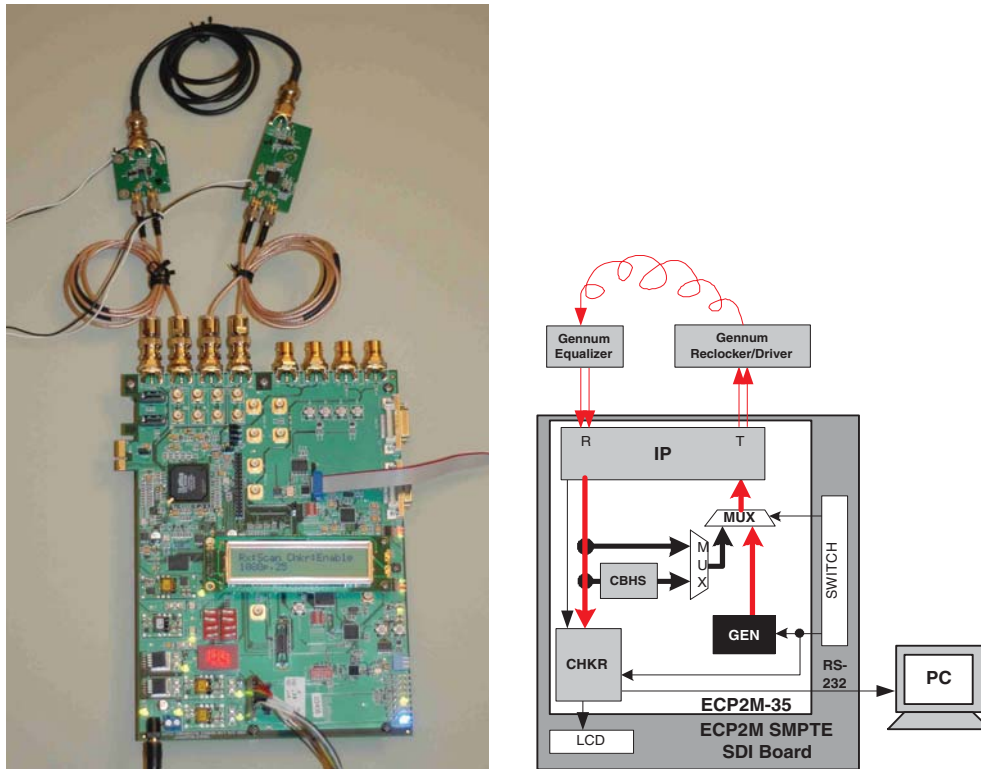
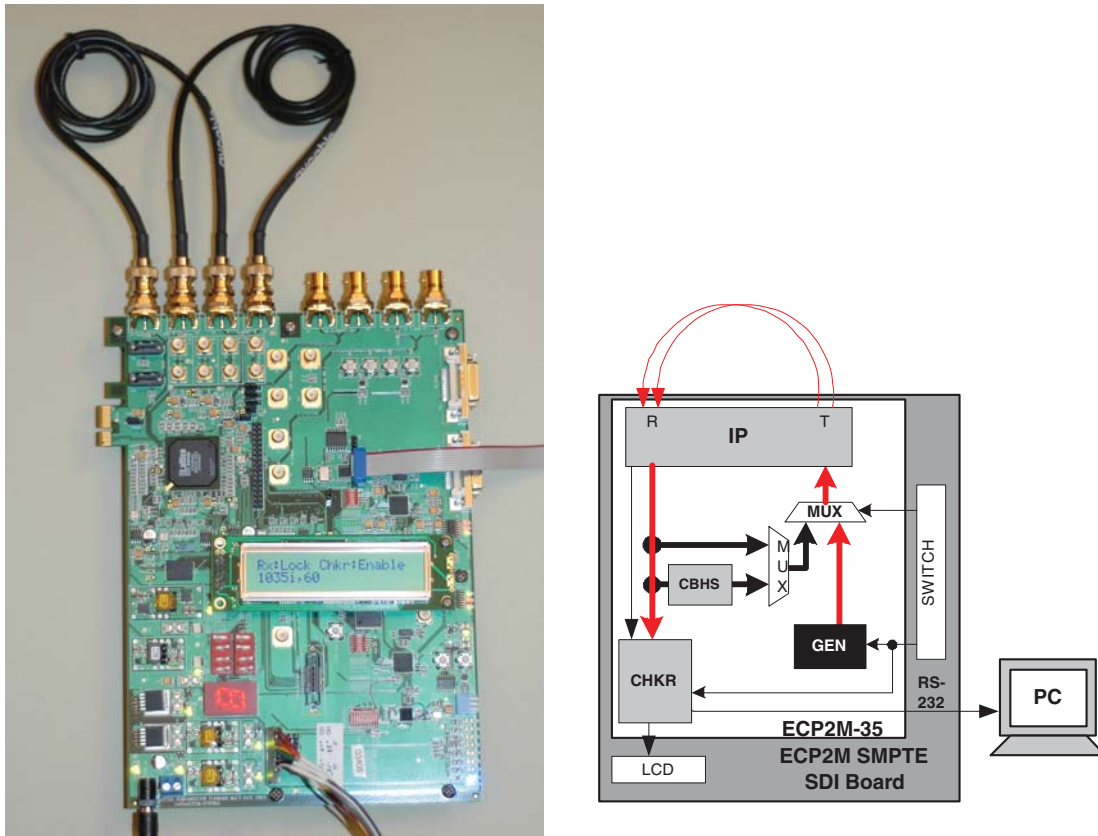
Figure 20. Connections of Loopback Pathological Test Using Gennum Cards

Figure 21 shows the connections of a loopback pathological signal test that does not use the Gennum Cards. The design is set to Pattern-Generation Mode with Pattern Checker turned on. The data path is also shown in Figure 21. Since the Gennum Cards are not used, the best connection will be using two 75 Ohm BNC-to-BNC cables to connect both the P and N connectors of the input and output. It will also work if using only one cable with the N connector terminated by the 75 Ohm terminator, but using two cables will get the best results.

Figure 21. Connections of Loopback Pathological Test Without Using Gennum Cards



This demo design can be flexibly configured. The figures below show the possible connections using two of the ECP2M SMPTE SDI boards. When two boards are chained together and running a loopback test, at least one board needs to be set to the Pattern-Generation mode. You may turn the pattern checkers of both boards on. If set it up this way, you will see the two boards trying for a few seconds to lock to the video stream created by the pattern generator, then both boards will lock and the DP segment on the 16-segment LED will start flashing.

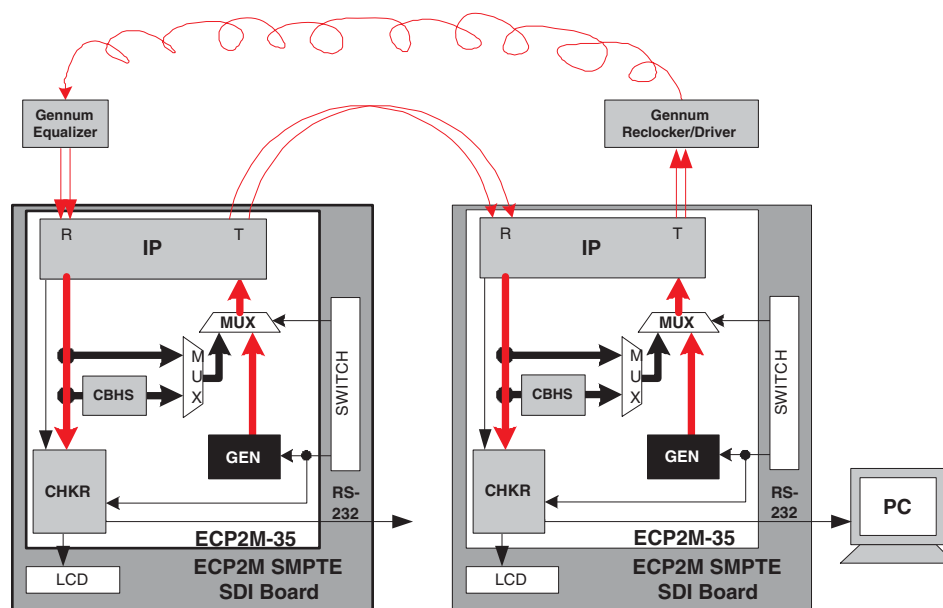
Figure 22. Connection Example 1 Using Two SMPTE SDI Boards

Figure 23. Connection Example 2 Using Two SMPTE SDI Boards

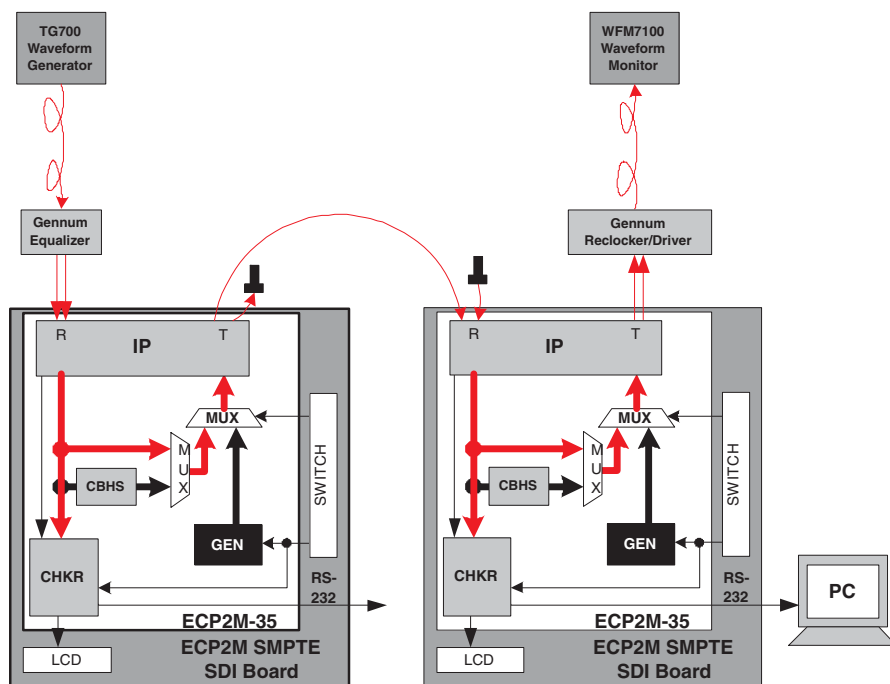
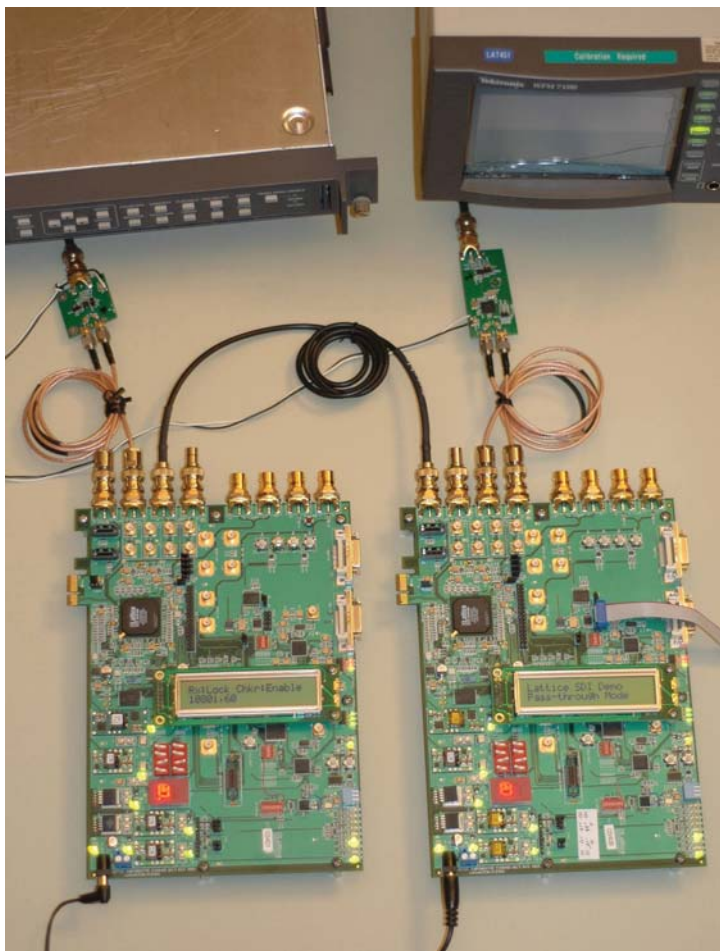
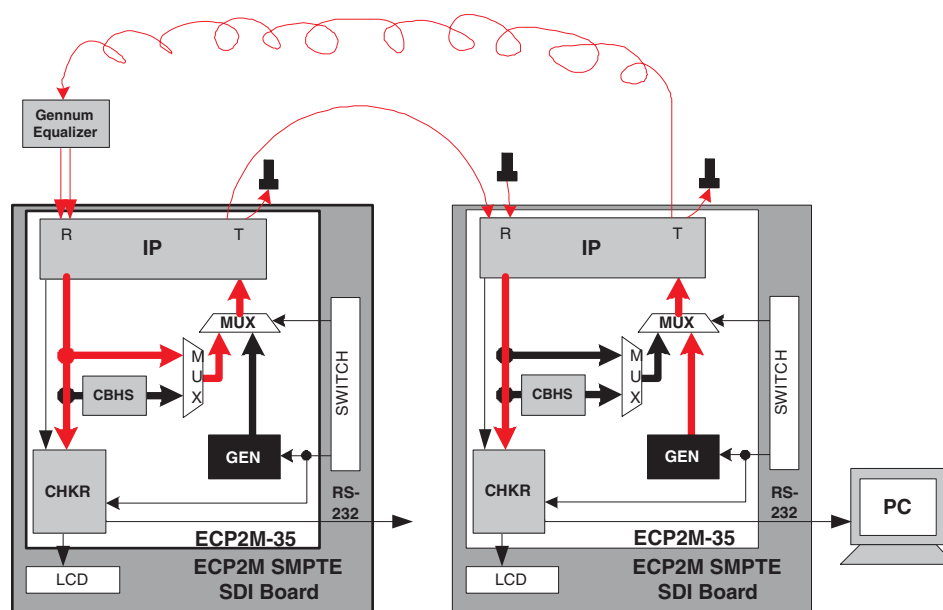
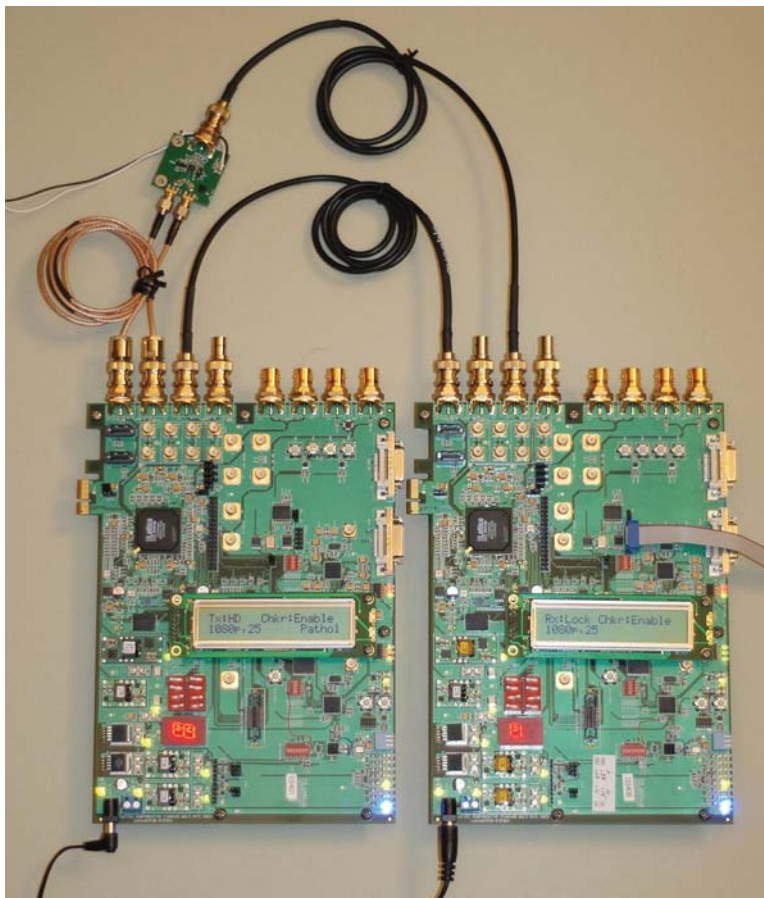


Figure 24. Connection Example 3 Using Two SMPTE SDI Boards



CML Output Connection Considerations

Lattice CML drivers are constructed with an open-drain differential pair and a voltage-controlled current source. The outputs (Output+ and Output-) include pullup resistors to VCCOB (typically 1.2 to 1.5V DC) because the outputs drive only falling edges efficiently and need the pullups to help drive rising edges.

This CML output structure is important to understand when connecting the Lattice SERDES CML outputs directly to test equipment. Most test equipment inputs are terminated to ground. This is true with oscilloscopes, waveform analyzers, and similar testers. Since the CML output is terminated to VCC and test equipment is terminated to ground, AC coupling, also known as DC blocks, should be used. The capacitor removes the DC component of the signal (common-mode voltage), while the AC (voltage swing) is passed on to the test equipment. This approach provides a method to insure compatibility between the test equipment and the CML output and conveys an accurate representation of the signal to the test equipment.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
November 2007	01.0	Initial release.
July 2008	01.1	Added CML Output Connection Considerations text section.