LatticeECP2M™ SMPTE SDI Evaluation Board

User's Guide

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Introduction

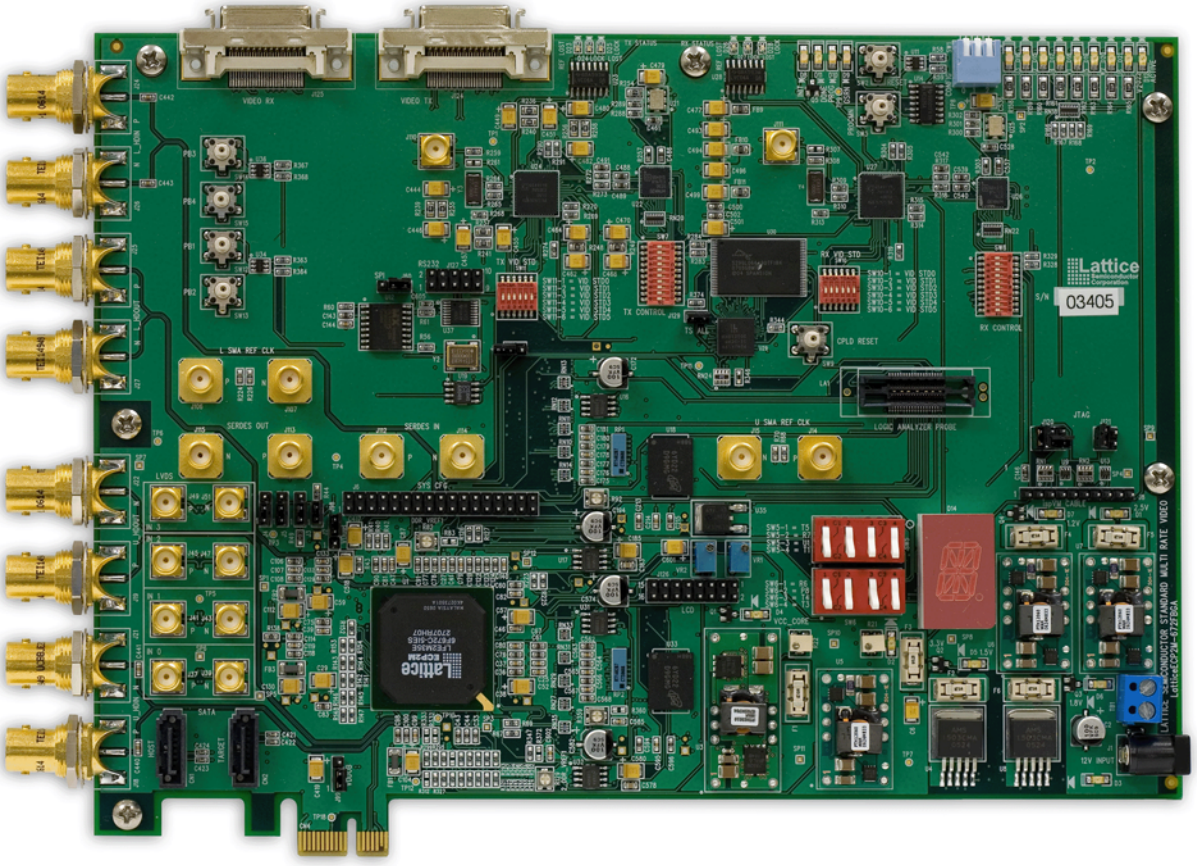
The key circuits inside the LatticeECP2M devices and the features of the SMPTE SDI Evaluation Board help audio and video engineers with prototyping and testing their specific designs. For example, the integration of multi-gigabit serial transceivers and advanced I/O features has enabled the support of many more networking standards than previously possible. This now includes HD-SDI (SMPTE292M), SDI (SMPTE259M), and DVB-ASI, as well as others.

This user's guide describes the LatticeECP2M SMPTE SDI Evaluation Board featuring the LatticeECP2M LFE2M35-FF672 FPGA device. The stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces to demonstrate SMPTE 259 and 292 capabilities The board demonstrates that it is now viable to integrate HD-SDI, SDI and DVB-ASI encoders and decoders into an FPGA.

The evaluation board includes provisioning to connect SERDES channels via standard video BNC connectors to test and measurement equipment. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 75-ohm for differential traces SERDES connected to video channels. The PCB can be equipped with any LatticeECP2M device offered in the 672-ball fpBGA package. The board limitations are based on the FPGA array included on the board.

The board has several debugging and analyzing features for complete customer evaluations of the LatticeECP2M device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP2M FPGA.

Figure 1. LatticeECP2M SMPTE SDI Evaluation Board



Features

- For LatticeECP2M-35 and LatticeECP2M-50 Devices:
  - Video interface for interconnection to video standard equipment
  - Provide SATA interfaces to SERDES channels
  - Allow demonstration of PCI Express (x1) interfaces
  - Allow the demonstration of LVDS I/O signal integrity performance for rates up to 1Gbps
  - Allow control of SERDES PCS registers using the Serial Client Interface (ORCAstra)
  - On-board Boot Flash; both Serial SPI Flash and Parallel Flash via MachXO™ programming bridge
  - Show interoperation with high performance DDR2 memory components
  - Have a driver based "run-time" device configuration capability via a ORCAstra or RS232 interface
  - SMAs for external high-speed clock / PLL inputs
  - Switches, LEDs, displays for demo purposes
  - Input connection for lab-power supply
  - Power connections and power sources
  - ispVM® programming support
  - On-board and external reference clock sources
  - ORCAstra Demonstration Software interface via standard ispVM JTAG connection
  - Various high-speed layout structures
  - User-defined input and output points
  - SMA connectors included (10) for high-speed clock or data interfacing
  - Performance monitoring via test headers, LEDs and switches
- For LatticeECP2M-50 Only:
  - Additional SERDES connection for video channel allowing loop timing recovery using dual quad approach
  - On-board, inter-channel loop back between two SERDES channels
  - SERDES channel connection to DC coupled SMAs for SERDES performance monitoring and testing

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 1 shows the functional partitioning of the board.

Figure 2. LatticeECP2M SMPTE SDI Evaluation Board Outline Drawing

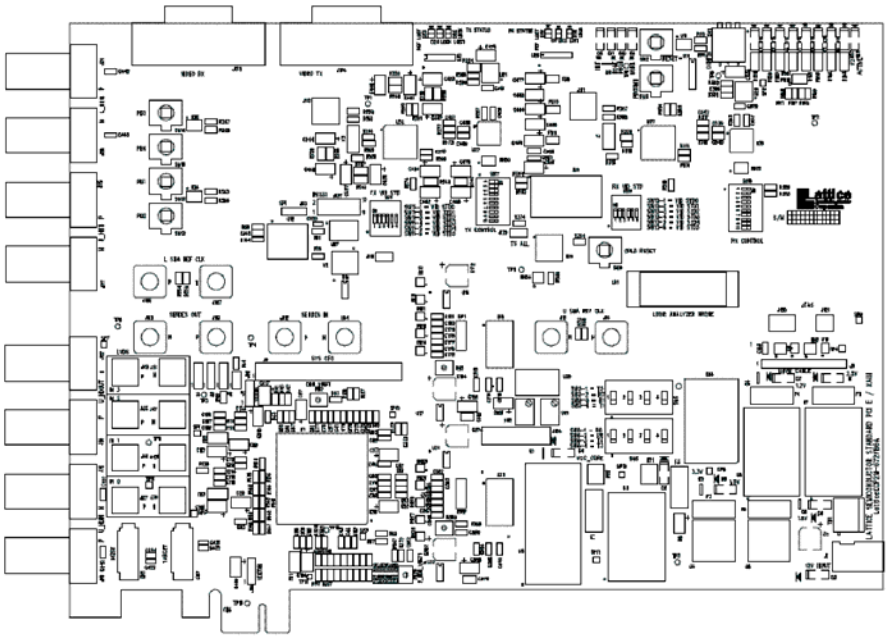
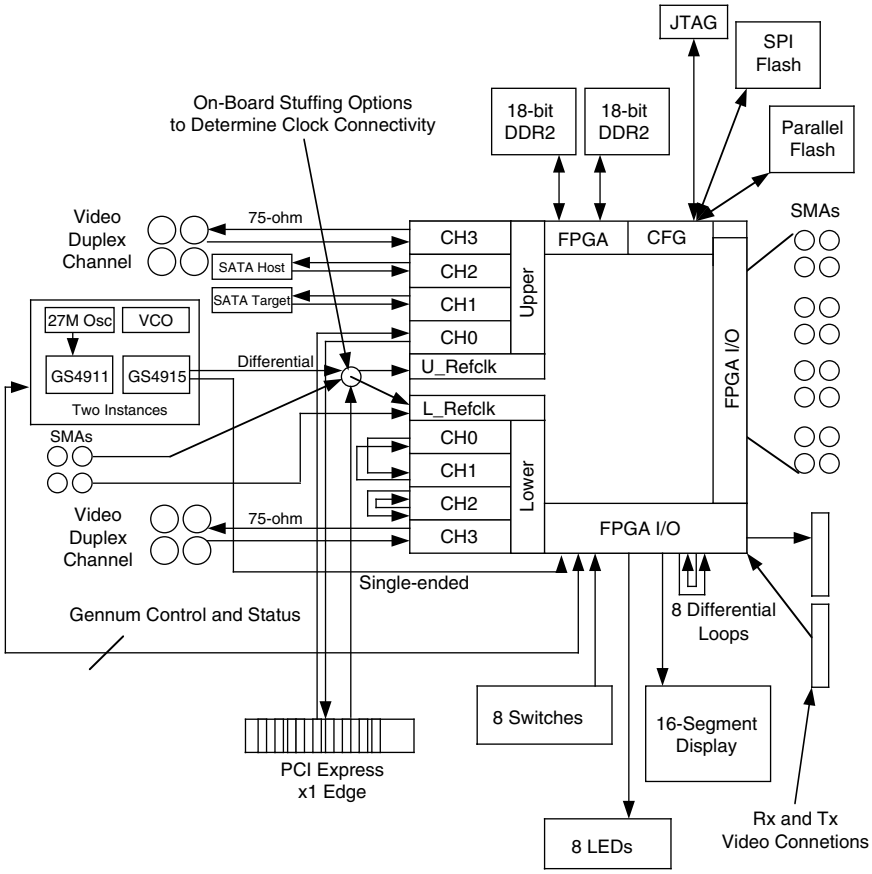


Figure 3. LatticeECP2M SMPTE SDI Evaluation Board



LatticeECP2M Device

This board features a LatticeECP2M FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP2M devices in the 672-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP2M Family Data Sheet on the Lattice website at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFE2M35E-FF672 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family. However, only the LFE2M50E-FF672 device allows full use of the high-speed SERDES test SMAs and SMPTE BNC connections.

Applying Power to the Board

The LatticeECP2M PCI Express Evaluation Board is ready to power on. The Evaluation Board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a bench top supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory supplied wall transformer, simply connect the output connection of the power cord to J1 and plug wall-transformer into an AC wall outlet.

Power Supplies

(see Appendix A, Figure 9)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a bench top supply adjusted to provide a nominal 12V DC.

All input power sources and on-board power supplies are fused with surface mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 1. Board Power Supply Fuses (see Appendix A, Figure 9)

F1	1.2V Core Fuse
F2	1.5V Fuse
F3	3.3V Fuse
F4	1.2V Fuse
F5	2.5V Fuse
F6	1.8V Fuse

Table 2. Board Power Supply Indicators (see Appendix A, Figure 9)

D1	2.5V Source Good Indicator
D2	3.3V Source Good Indicator
D3	12V Input Good Indicator
D4	1.2V VCC Core Source Good Indicator
D5	1.5V Source Good Indicator
D6	1.8V Source Good Indicator
D7	1.2V Source Good Indicator

External power can be alternatively connected rather than the wall transformer power pack

Table 3. Board Supply Disconnects (see Appendix A, Figure 9)

TB1	Screw terminal for 12V DC Pin1 (square PCB pad) → 12V DC Pin2 → Ground

PCI Express Power Interface

Power can be sourced to the board via the PCB edge-finger (CN1). This interface allows the user to provide power from a PCI Express host board.

Programming/FPGA Configuration

(see Appendix A, Figure 11)

A programming header is provided on the evaluation board, providing access to the LatticeECP2M JTAG port.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2M FPGA device and render the board inoperable.*

An ispDOWNLOAD® cable is included with each ispLEVER® design tool shipment. Cables may also be purchased separately from Lattice.

ispVM Download Interface

J8 is an 10-pin JTAG connector used in conjunction with the ispVM USB download cable to program and control the device.

Table 4. ispVM JTAG Connector (see Appendix A, Figure 9)

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN
Pin 5	NC
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE
Pin 10	INITN

Programming Daisy Chain

This board includes two Lattice Semiconductor programmable (U1 = LatticeECP2M, U29 = LCMXO1200) devices that can be programmed in a daisy chain. A jumper setting of J120 controls the chain. Both devices are in the programming chain from the JTAG header J8 with jumpers on J120 across Pins {1-2}, Pins {3-4}, and Pins {5-6}. Also a jumpers on J121 across Pins {1-2}, Pins {3-4} are also required for both devices to be in the chain.

If the user desires to only program U1, J120 requires jumpers across Pins {1-2} and Pins{3-5}, J10 requires only a jumper should be across Pins {1-2}.

Download Procedures

Requirements:

- PC with ispVM System v.16.0 (or later) programming management software, installed with appropriate drivers (USB driver for USB cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download

The LatticeECP2M device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

1. Connect the ispDOWNLOAD cable to the appropriate header. J8 is used for the 1x10 cable.

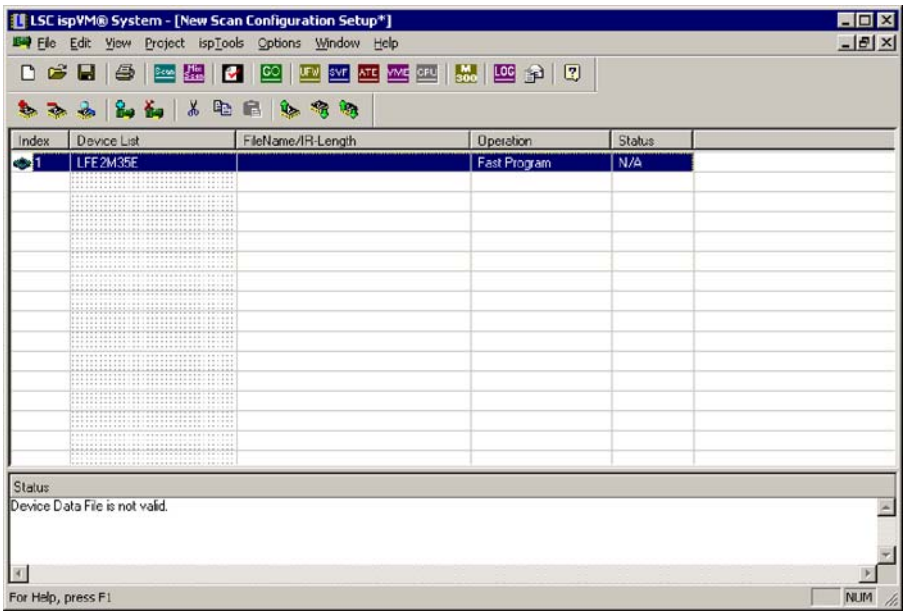
   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2M FPGA device and render the board inoperable.*

2. Connect the LatticeECP2M Evaluation Board to the appropriate power sources and power-up the board.

3. Start the ispVM System software.

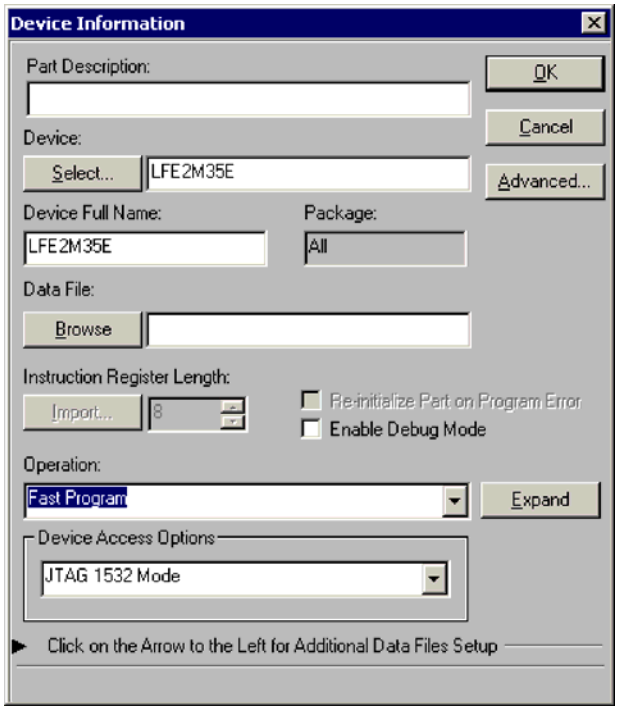
4. Press the **SCAN** button located in the toolbar. The LatticeECP2M device should be automatically detected.

Figure 4. ispVM Programming Window



5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.

Figure 5. ispVM Device Information Window



6. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Configuration Status Indicators

(see Appendix A, Figure 11)

These LEDs indicate the status of configuration to the FPGA.

- D8 (RED) illuminated, this indicates that the programming was aborted or reinitialized driving the INITN output low.
- D11 (GREEN) is illuminated, this indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D12 (GREEN) will flash indicating TDI activity.
- D10 (RED) illuminated, this indicates that PROGRAMN is low.
- D9 (RED) illuminated, this indicates that GSRN is low.

PROGRAMN & GSRN

(see Appendix A, Figure 11)

These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and GSRN (SW2). Depressing the button drives a logic level "0" to the device.

The GSRN push-button is connected to a general purpose FPGA pin (BGA AA20). It must be specifically included by the user in the FPGA design, if needed.

CFG [2:0]

(see Appendix A, Figure 11)

The FPGA CFG pins are set on the board for a particular programming mode via the SW1 DIP switch. JTAG programming is independent of the MODE pins and is always available to the user. Pushing in (depressing) the switch is ON and sets the value to 0.

Table 5. CFG Mode Selections

CFG2	CFG1	CFG0	Configuration Mode
0 (ON)	0 (ON)	0 (ON)	SPI Flash Mode (available on-board)
0 (ON)	1 (OFF)	0 (ON)	SPIm
1 (OFF)	0 (ON)	0 (ON)	Master Serial
1 (OFF)	0 (ON)	1 (OFF)	Slave Serial
1 (OFF)	1 (OFF)	0 (ON)	Master Parallel
1 (OFF)	1 (OFF)	1 (OFF)	Slave Parallel
X (don't care)	X (don't care)	X (don't care)	ispJTAG

On-Board Flash Memory

(see Appendix A, Figure 11)

One SPI (16-pin TSSOP 64M) Flash memory devices (U12) is on board for non-volatile configuration memory storage. The CFG [2:0] need to be [000] all depressed and J60 jumper installed on pins 2-3.

A 16-bit parallel Flash device is also available. This board uses a Lattice MachXO CPLD device to act as a programming bridge from the Flash device. The CFG [2:0] needs to be [111] all up and J60 jumper installed on pins 1-2.

Video Clock Management

(see Appendix A, Figures 16 and 17)

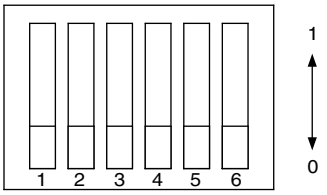
Industry standard video clocks are generated and managed via Gennum chipsets. These chipsets are used to generate both transmit and receive clocks. The GS4911 clock generator device produces multiple video standard reference clocks from an on-board 27MHz oscillator. This device can also receive input clock from an external clock source via a SMA. The GS4915 clock cleaner is used to reduce clock jitter to produce a clean clock for video signal quality using a high performance VCO. Both the GS4911 and GS4915 are controlled by on-board switches and connections to the FPGA. Device status is also observed from LED indicators.

Table 6. Gennum Clock Device Control and Status Components

	GS4911 Clock Gen	GS4915 Clock Cleaner	Video Clock Selection Switch	Control Switch	Ref Clk Lost	Lock Lost	Lock
TX Clock	U24	U22	SW11	SW7	D23	D24	D25
RX Clock	U27	U26	SW10	SW8	D26	D27	D28

Both GS4911 clock generator devices use a DIP switch (SW10 and SW11) to control the desired frequency generated by the devices. These switches control the VID[0:5] as outlined in Table 20 of the GS4911B/GS4910B data sheet.

Figure 6. VID Switch Position (SW10 and SW11)



The control signals to the Gennum Clock chipsets can also be controlled via the FPGA. Table 7 outlines the connections between the Gennum Clocking devices and the FPGA.

Table 7. Gennum Clock Devices to FPGA Interconnections

GS4911B- Schematic Designator U27		
Signal	**Clock Pin Name**	**FPGA Pin**
rx_gs4911_ctrl_0	RESETn	F7
rx_gs4911_ctrl_1	GENLOCKn	G9
rx_gs4911_ctrl_2	VID_STD5	C4
rx_gs4911_ctrl_3	VID_STD4	B2
rx_gs4911_ctrl_4	VID_STD3	C5
rx_gs4911_ctrl_5	VID_STD2	B3
rx_gs4911_ctrl_6	VID_STD1	E7
rx_gs4911_ctrl_7	VID_STD0	H10
rx_gs4911_out_1	TIMING_OUT1	E10
rx_gs4911_out_2	TIMING_OUT2	F12
rx_gs4911_out_3	TIMING_OUT3	A8
rx_gs4911_out_4	TIMING_OUT4	B9
rx_gs4911_out_5	TIMING_OUT5	E8
rx_gs4911_out_6	TIMING_OUT6	A9
rx_gs4911_out_7	TIMING_OUT7	H14
rx_gs4911_pclk	PCLK2	F14
rx_hsync	HSYNC	H16
rx_se_refclkGS4515	SE_CLKOUT	G15
rx_vsync	VSYNC	D12
fsync	FSYNC	H18

GS4911B- Schematic Designator U24		
Signal	**Clock Pin Name**	**FPGA Pin**
tx_gs4911_ctrl_0	RESETn	C8
tx_gs4911_ctrl_1	GENLOCKn	G12
tx_gs4911_ctrl_2	VID_STD5	D8
tx_gs4911_ctrl_3	VID_STD4	H12
tx_gs4911_ctrl_4	VID_STD3	A6
tx_gs4911_ctrl_5	VID_STD2	A5
tx_gs4911_ctrl_6	VID_STD1	A4
tx_gs4911_ctrl_7	VID_STD0	A3
tx_gs4911_out_1	TIMING_OUT1	D10
tx_gs4911_out_2	TIMING_OUT2	F13
tx_gs4911_out_3	TIMING_OUT3	E11
tx_gs4911_out_4	TIMING_OUT4	G14
tx_gs4911_out_5	TIMING_OUT5	B10
tx_gs4911_out_6	TIMING_OUT6	A10
tx_gs4911_out_7	TIMING_OUT7	H15
tx_gs4911_pclk	PCLK2	C11
tx_hsync	HSYNC	A11
tx_se_refclk	SE_CLKOUT	C12
tx_vsync	VSYNC	A12

A control interface to the clock devices is connected to the FPGA to dynamically control the video clocking modes. This control bus GSPI uses a simple 3-pin interface to control the GS4911 clock generators. A chip select is used to pick which clock device is being controlled.

Table 8. Gennum Serial Peripheral Interface

GSPI Bus	FPGA Pin
RX GSPI CSn	G7
TX GSPI CSn	G8
GSPI CLK	F8
GSPI DI	J10
GSPI DO	D4

SW7 and SW8 DIP switches can be used to set the control signals to the Gennum clock devices. SW7 controls the TX chipsets and SW8 controls the RX chipsets.

Figure 7. Gennum Clocking Control Switches

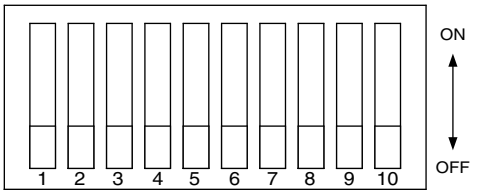


Table 9. Gennum Clock Control Switch Connections

SW7 Control Switches	
1	TX RESET GS4911
2	TX RESET GS4915
3	TX SKEW EN
4	TX DOUBLE
5	TX FCRTL1
6	TX FCTRL0
7	TX AUTOBYPASS
8	TX BYPASS
9	TX IPSEL
10	TX GENLOCKN

SW8 Control Switches	
1	RX RESET GS4911
2	RX RESET GS4915
3	RX SKEW EN
4	RX DOUBLE
5	RX FCRTL1
6	RX FCTRL0
7	RX AUTOBYPASS
8	RX BYPASS
9	RX IPSEL
10	RX GENLOCKN

Clock Status Indicators

The board includes several LED indicators that are used to monitor the status of the Gennum clock devices.

Table 10. Gennum Clock Device Status Indicators

Indicator	LED Designation	Description
TX REF LOST	D23	Will light GREEN when TX GS4911(U24) REF_LOST pin is high. This indicates no reference signal applied to device or other conditions. Refer to GS4911 data sheet. Otherwise, it will be RED.
TX LOCK LOST	D24	Will light GREEN if the GS4911(U24) LOCK_LOST is high indicating the output is not Genlocked to the input. Otherwise. it will be RED.
TX LOCK	D25	RED indicates the TX GS4915(U22) LOCK pin is high which indicates the output clock is locked to the selected input. Otherwise it will be GREEN.
RX REF LOST	D26	Will light GREEN when TX GS4911(U27) REF_LOST pin is high. This indicates no reference signal applied to device or other conditions. Refer to GS4911 data sheet. Otherwise it will be RED.
RX LOCK LOST	D27	Will light GREEN if the GS4911(U27) LOCK_LOST is high indicating the output is not Genlocked to the input. Otherwise, it will be RED.
RX LOCK	D28	RED indicates the TX GS4915(U26) LOCK pin is high which indicates the output clock is locked to the selected input. Otherwise, it will be GREEN.

SERDES

(see Appendix A, Figure 13)

SERDES Reference Clocks

Note: This board supports many application specific SERDES capabilities. The board has to be provisioned correctly comply with the appropriate clock rate required for the particular application.

The 50-ohm terminated SMA connectors are provided the supply reference clocks directly to the LatticeECP2M device. These SMAs are board provisioned by resistor shunt connections that can be optionally removed.

Table 11. SERDES Reference Clocks

Connector	SERDES Signal	FPGA Pin	Resistor Shunt
J14	U_REFCLKP	D19	R67
J15	U_REFCLKN	E19	R69
J106	L_REFCLKP	AC19[1]	R223
J107	L_REFCLKN	AB19[1]	R225

1. Pins only available with LatticeECP2M-50 device.

The user must provision the board correctly to select the proper clocking for the application. This is done by removal or shunting of SMT resistor pads. For PCI Express the clock is sourced from the PCI Express edge connection. For SMPTE the clocks are generated from the Gennum Video Clock sources. Table 12 outlines the different clock provisioning per application.

Table 12. Reference Clock Source Selection

	R79	R80	R262	R263	R334	R335
SMPTE	open	open	shunt	shunt	shunt	shunt
PCI Express	shunt	shunt	open	open	open	open
SATA	open	open	open	open	open	open

Note: SATA must be clocked via an external clock source from the SMA clock inputs.

SERDES Channels

Video Interface Connections

The 75-ohm terminated BNC edge launch connectors provide the video signals directly to the LatticeECP2M device.

Table 13. SERDES Video Interconnections

Connector	SERDES Signal	FPGA Pin
J18	U_HDINP3	A14
J21	U_HDINN3	B14
J19	U_HDOUTP3	A17
J22	U_HDOUTN3	B17
J24	L_HDINP3	AF17[1]
J26	L_HDINN3	AE17[1]
J25	L_HDOUTP3	AF14[1]
J27	L_HDOUTN3	AE14[1]

1. Pins only available with LatticeECP2M-50 device.

Surface Mounted SMA Connections

(see Appendix A, Figure 12)

DC coupled top-mounted SMA connectors connect to the four SERDES Tx and Rx channels. These pins are directly coupled to the designated SMA connector creating a path for both input and output differential data.

Table 14. SERDES Connectors (see Appendix A, Figure 12)

SMA	Channel Name	FPGA Pin
J112	L_HDINP2	AF15
J114	L_HDINN2	AE15

SMA	Channel Name	FPGA Pin
J113	L_HDOUTP3	AF18
J115	L_HDOUTN3	AE18

Note: Only available with the LatticeECP2M-50 device.

SERDES SATA Channels

(see Appendix A, Figure 12)

The board contains two SATA host connectors that can be connected to a SATA device (such as a hard disk) using a standard SATA cable. The SATA connectors are connections that are included to attach SATA type cables to SERDES channels for board-to-board or loopback purposes. The connectors are configured using the 7-pin SATA specifications.

The SATA physical interface can carry SERDES signals up to 1.5 Gbps for general-purpose usage.

The board ships with a SATA cable that is used as a loopback connection between the two SATA connectors for loopback testing and bit error rate testing (BERT). The SATA crossover cable can also be used to connect between two boards.

Table 15. SERDES SATA Interconnections

Host			Target		
Pin Name	**SERDES Pin**	**FPGA Pin**	**Pin Name**	**SERDES Pin**	**FPGA Pin**
OUT_HOST+	U_HDOUTP1	A20	OUT_TARGET+	U_HDOUTP2	A18
OUT_HOST-	U_HDOUTN1	B20	OUT_TARGET-	U_HDOUTN2	B18
IN_HOST+	U_HDINP1	A23	IN_TARGET+	U_HDINP2	A15
IN_HOST-	U_HDINN1	B23	IN_TARGET-	U_HDINN2	B15

SERDES PCI Express Channels

(see Appendix A, Figure 12)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1) to fit directly into an x1 host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

Table 16. SERDES PCI Express Interconnections

Pin Name	FPGA Pin	PCI Express Edge	Description
U_HDOUTP_0	A21	A16	Integrated Endpoint block transmit pair
U_HDOUTN_0	B21	A17	
U_HDINP_0	A24	B14	Integrated Endpoint block receive pair
U_HDINN_0	B24	B15	
U_REFCLKP	D19	A13	Integrated Endpoint block differential clock pair
U_REFCLKN	E19	A14	
PCIE_PERSETN	AA20	A11	Fundamental PCI Express Reset

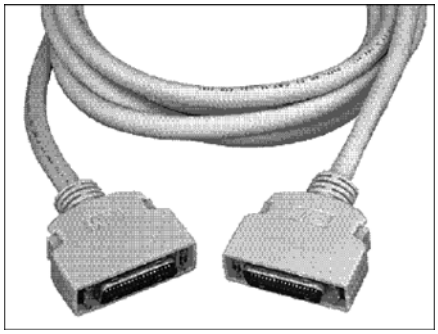
Low Speed Video Connections

(see Appendix A, Figure 20, J124 and J125)

3M™ Mini D Ribbon (MDR) Cables are used in conjunction with the on-board MDR-26(p/n 10226-1210VE) Tx and Rx connectors. These connections include five LVDS pairs (four data pairs and one clock pair). All five Tx pairs are assigned to the pins using the same edge clock. It's the same for the five Rx pairs. The Rx clock input pair is assigned to the dedicated PLL clock input.

Table 17. MDR Connector to FPGA I/O

Video TX- J124	FPGA Pin	Video RX J125	FPGA Pin
TX OUT0+	F21	RX IN0+	M24
TX OUT0-	H20	RX IN0-	M22
TX OUT1+	F22	RX IN1+	L24
TX OUT1-	J18	RX IN1-	L22
TX OUT2+	K19	RX IN2+	L26
TX OUT2-	G22	RX IN2-	M26
TX OUT3+	H24	RX IN3+	N25
TX OUT3-	H23	RX IN3-	N24
TX CLKOUT+	E23	RX CLKIN+	K26
TX CLKOUT-	E24	RX CLKIN-	K25



FPGA Test Pins

(see Appendix A, Figure 20)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to switches and LEDS designated according to Table 18. Push-button switches are available for connection to general purpose FPGA pins. The switches are debounced and can be used for user designs.

Table 18. FPGA Test pins (see Appendix A, Figure 14)

Switch	BGA	Netname
SW6D	T3	Switch1
SW6C	T4	Switch2
SW6B	P8	Switch3
SW6A	R6	Switch4
SW5D	T1	Switch5
SW5C	U1	Switch6
SW5B	R7	Switch7
SW5A	T5	Switch8
SW12	AD26	PB1
SW13	AC23	PB2
SW14	AC25	PB3
SW15	W20	PB4

LED	BGA	NetName
D16	U3	RED1
D17	U4	YELLOW1
D19	U5	GREEN1
D21	U6	BLUE1
D15	U2	RED2
D18	V1	YELLOW2
D20	W2	GREEN2
D22	V2	BLUE2

Note: LEDs will illuminate if connected to an unprogrammed FPGA pin. It is recommended that a pull-down be programmed on FPGA output pins.

LCD Interface

(see Appendix A, Figure 19)

A 2x8 Header (J126) provides a connection to 16-character x 2 line LCD modules such as Varitronix VDM16265. A ribbon cable connection will allow attachment to the connector. The board includes two variable resistors for LCD adjustments. VR1 adjusts the backlight and VR2 provides contrast adjustment. A user design must be included in the FPGA to drive this feature. This header can also be used for probe points for observing FPGA pins.

Table 19. Header J26 Pin Connections

NetName	672-Ball BGA	Header Pin Number
LCD0	AA3	7
LCD1	Y21	9
LCD2	Y5	11
LCD3	AB2	13
LCD4	AA4	15
LCD5	Y6	6
LCD6	U9	8
LCD7	AA5	10
LCD8	AA6	12
LCD9	Y7	14
LCD10	V9	16

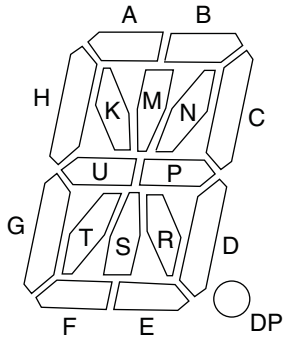
17-Segment LED Display

(see Appendix A, Figure 17)

General-purpose FPGA pins are connected to a 17-segment display according to Table 20. These pins can be driven low to illuminate the display segments.

Table 20. 17-Segment LED Display

Segment	BGA
A	W16
B	AC20
C	AB20
D	AB17
E	W15
F	AC17
G	Y15
H	AA15
K	AB16
M	AC16
N	AB15
P	AC15
R	AA14
S	AB14
T	AC14
U	Y14
DP	AC13



Test SMA Connections

General-purpose FPGA pins are available via SMA test connections. These connections are designed to permit evaluations of several types of FPGA I/O buffers. The use of several termination schemes permits easy interfaces for the type of buffer.

Table 21. FPGA I/O Test SMA Connectors (see Appendix A, Figure 16)

SMA Designation	Name	LFE2M35E Signal	672-Ball fpBGA	Termination Description	Termination Resistor(s)
J37	LVDS_INP0	PR37A	N23	100-ohm Differential	R130
J39	LVDS_INN0	PR37B	M21		
J41	LVDS_INP1	PR41A	P24	100-ohm Differential	R132
J43	LVDS_INN1	PR41B	P23		
J45	LVDS_INP2	PR51A	T24	100-ohm Differential	R134
J47	LVDS_INN2	PR51B	U24		
J49*	LVDS_INP3	PR57A	V24	100-ohm Differential	R136
J51*	LVDS_INN3	PR57B	W24		
J38	LVDS_OUTP0	PR50A	T23	100-ohm Differential	R131
J40	LVDS_OUTN0	PR50B	T22		
J42	LVDS_OUTP1	PR53A	V26	100-ohm Differential	R133
J44	LVDS_OUTN1	PR53B	V25		
J46	LVDS_OUTP2	PR55A	W26	100-ohm Differential	R135
J48	LVDS_OUTN2	PR55B	W25		
J50	LVDS_OUTP3	PR59A	Y26	100-ohm Differential	R137
J52	LVDS_OUTN3	PR59A	AA26		

High Speed Test Point

DP1

(see Appendix A, Figure 16)

General-purpose FPGA pins are available to a differential test pad. These connections allow a high-impedance probe to measure the performance of a coupled-differential output buffer pair.

Logic Analyzer Probe

(see Appendix A, Figure 19)

An AMP/TYCO 767004 38 position 0.025 VERT SMD logic analyzer probe connection is provided for the user to utilize for test points. This connection provides 34 general I/O signals to be observed on a Logic Analyzer probes using Mictor connections such as the Agilent 5346A.

General Purpose I/O/sysCONFIG Header

(see Appendix A, Figure 19)

Header J6 is available to access configuration and dual purpose FPGA pins. This header provides probe points to the specific pins.

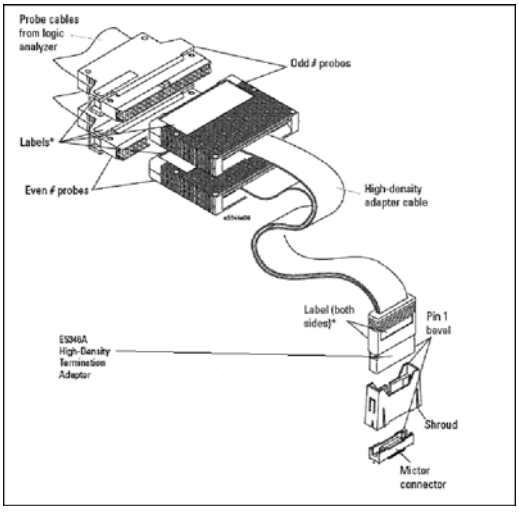
Table 22. J6 Header Pinout Crossover

Net Name	672-Ball BGA	Header Pin	Net Name	672-Ball BGA	Header Pin
CCLK	AB24[1]	1	GND		2
SISPI	Y24	3	N/C		4
CSSPI0N	V20	5	3.3V		6
CSSP1N	W23	7	INITN	AA23[1]	8
DONE	AB25[1]	9	PROGRAMN	AC26[1]	10
D7	W21	11	GND		12
D6	AA24	13	GND		14
D5	Y23	15	GND		16
D4	W18	17	GND		18
D3	W22	19	GND		20
D2	Y20	21	GND		22
D1	W19	23	GND		24
D0	Y22	25	GND		26
CSN	AB26	27	WRITE	Y19	28
CS1	Y21	29	CFG0	AB23[1]	30
3.3V		31	CFG1	AA22[1]	32
GND		33	CFG2	AA21[1]	34

1. This pin cannot be used for any other purpose.

Table 23. Logic Analyzer To FPGA Pin Reference

Signal	FPGA Pin	Signal	FPGA Pin
LA1	AA17	LA2	AA18
LA3	Y17	LA4	AC21
LA5	W17	LA6	AA19
LA7	Y18	LA8	AC22
LA9	P3	LA10	P2
LA11	P5	LA12	N6
LA13	P4	LA14	R3
LA15	P6	LA16	N7
LA17	E13	LA18	H17
LA19	E12	LA20	F15
LA21	D13	LA22	D14
LA23	E14	LA24	G17
LA25	E15	LA26	G18
LA27	D15	LA28	E16
LA29	F18	LA30	F19
LA31	D16	LA32	F17
LA33	D17	LA34	E17



DDR2 Memory Devices

U18 and U133

(see Appendix A, Figure 15)

The LatticeECP2M Evaluation Board is equipped with two 84-ball BGA DDR2 SDRAM memory devices such as a Micron MT47H16M16BG-3 device. The two independent DDR2 memory interfaces includes a 16-bit wide device. The evaluation board includes termination of address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP2M device.

Board Jumpers

The board is equipped with several 0.1 headers. These headers are used to field provision specific features.

Table 24. Default PCB Jumper Settings

Header Designation	Description	Factory Default[1]
J2	Selects SPIFASTN. If low, the LatticeECP2/M will use SPI Serial Flash fast read op-code 0B (hex). The fast read op-code 0B (hex) accommodates higher frequency read clocks.	1-2
J3	CSN: Driving both CSN and CS1N high causes the LatticeECP2/M to exit Bypass or Flow-Through mode and resets the Bypass register.	1-2
J4	CS1N: See description above (J3) for more information.	1-2
J5	Selects the connection of theCSSPI0N between using it as DI (Data Input) for Serial configurations In SPI or SPIm mode the CSSPI0N becomes a low true Chip Select output that drives the SPI Serial Flash Chip Select. The board connects this pin the the sysCONFIG™ header.	1-2
J60	Selects the connection from the FPGA CCLK to either a SPI Flash device or the parallel Flash device.	2-3
J98	Selects the VDDIB for the CML between 1.2V or 1.5V. Default 1.2V.	2-3
J99	Selects the VDDOB for the CML between 1.2V or 1.5V. Default 1.5V.	1.2
J116	Connects D7 to SPI Flash Q.	1-2
J120	Selects the JTAG path from the ispVM download cable.	1-2, 3-5
J121	Selects the device TMS pins for JTAG.	1-2
J129	Tristates the MachXO device when not being used for parallel loading.	1-2

1. Indicates which pins on header are connected with a jumper.

References

- GS4911B/GS4915B Device Data Sheet 36655-3, August 2006, Gennum Corporation
- GS4915 Preliminary Device Data Sheet 39145-0, November 2006, Gennum Corporation

Additional Resources

The use of the LatticeECP2M device in a SMPTE video system requires following quality PCB design practices. Lattice provides several technical notes regarding PCB design that assist users in building a reliable SERDES system. These documents address topics such as power supply selection, routing practices, and other component selections. Please refer to these documents when adopting the Lattice SMPTE design to your PCB system.

- TN1033 - High-Speed PCB Design Considerations
- TN1114 - Electrical Recommendations for Lattice SERDES
- TN1162 - LatticeECP2/M Hardware Checklist

These technical notes can be found by visiting the Lattice website at www.latticesemi.com, and typing the reference number of the document (e.g., TN1033) in the search box.

Known Issues

The initial PCB design has higher than desired clock jitter due to the proximity of the clock circuitry to the FPGA. A significant improvement in clock jitter can be made by locating clock circuitry as close as possible to the FPGA. This will be considered in future revisions of this PCB.

Technical Support Assistance

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
June 2007	01.0	Initial release.
October 2007	01.1	Product name changed from LatticeECPM SMPTE Video Evaluation Board to LatticeECPM SMPTE SDI Evaluation Board.
		Miscellaneous changes to Gennum Clock Device Status Indicators table.
		Miscellaneous changes to Default PCB Jumper Settings table.
		Updated Appendix A schematics.
November 2007	01.2	Added "Additional Resources" and "Known Issues" text sections.
December 2007	01.3	Added Header J26 Pin Connections table.
		Added General Purpose I/O/sysCONFIG text section and J6 Header Pinout Crossover table.
December 2007	01.4	Updated Configuration/Testpoints and FPGA Test schematics in Appendix A.

Appendix A. Schematic

Figure 8. Cover Page

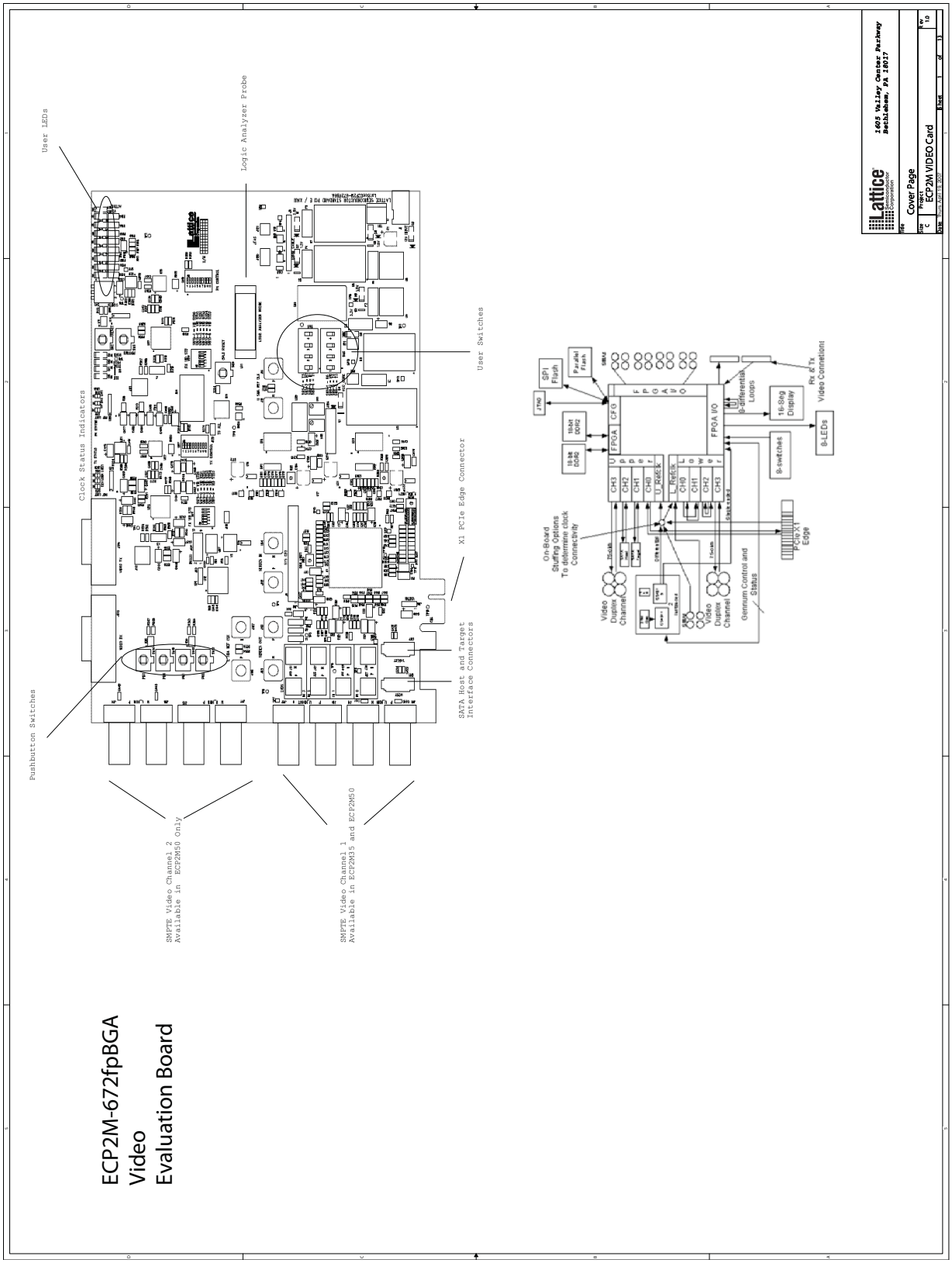


Figure 9. DC/DC Conversion

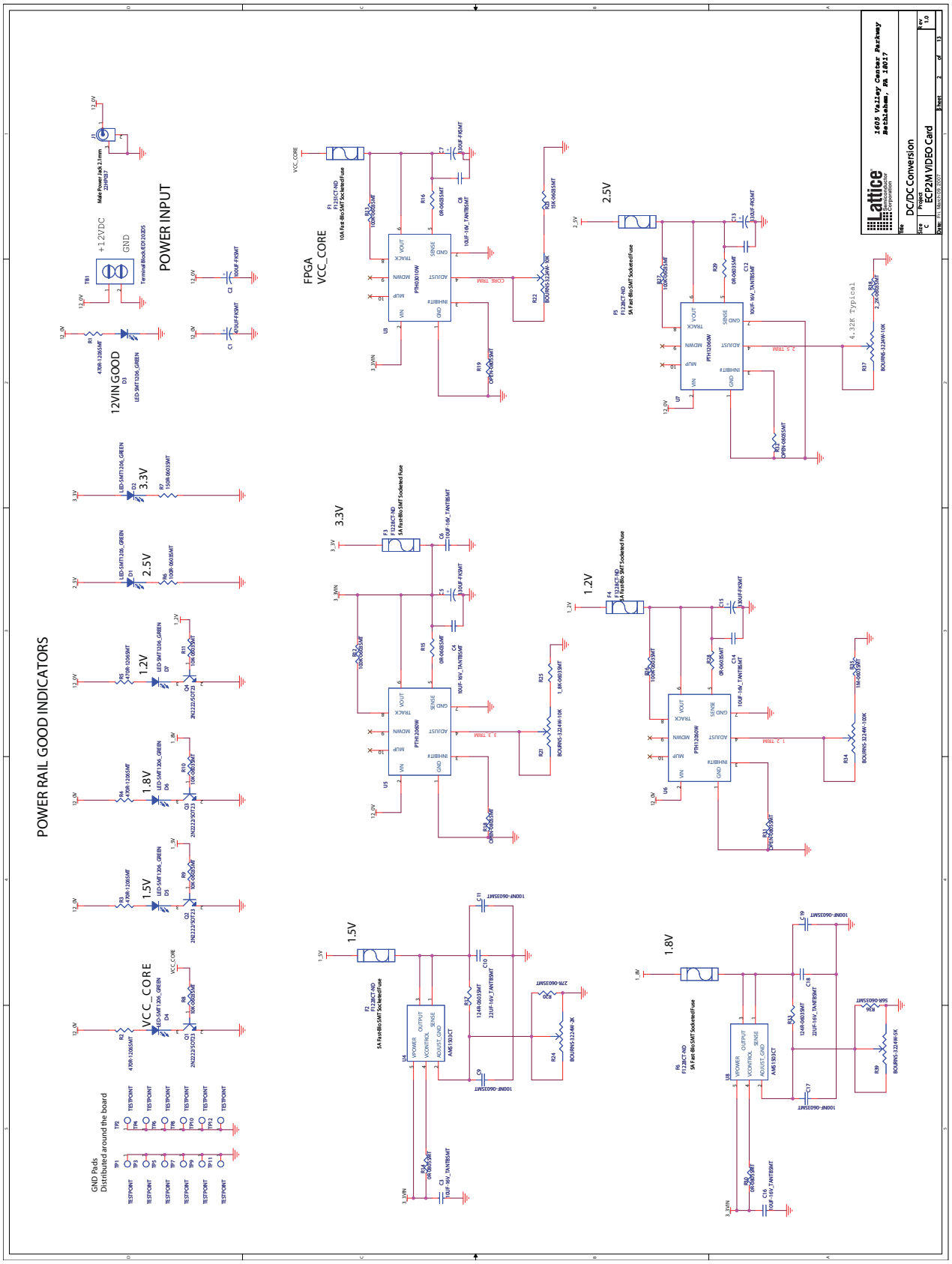


Figure 10. Power Supplies

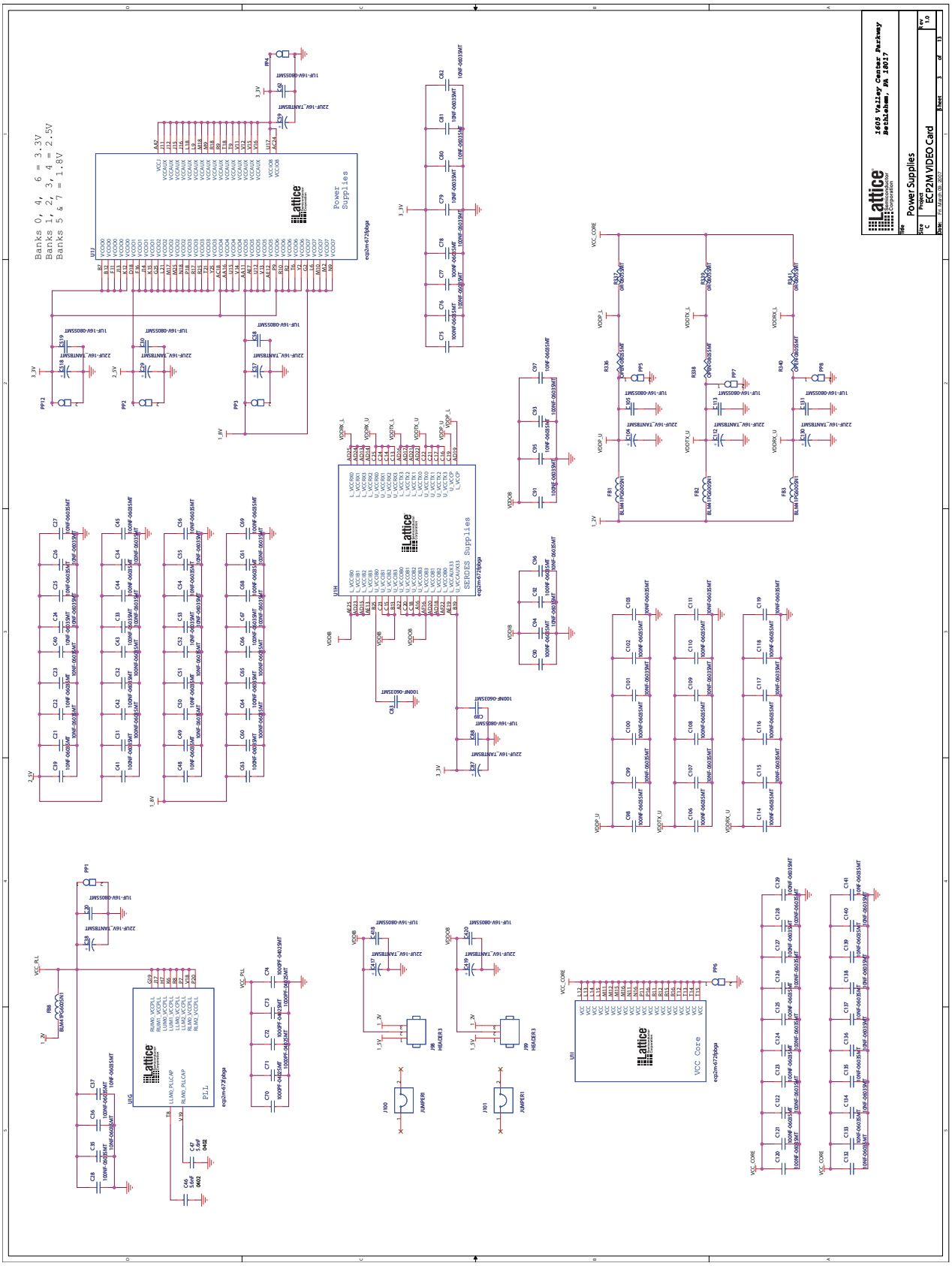
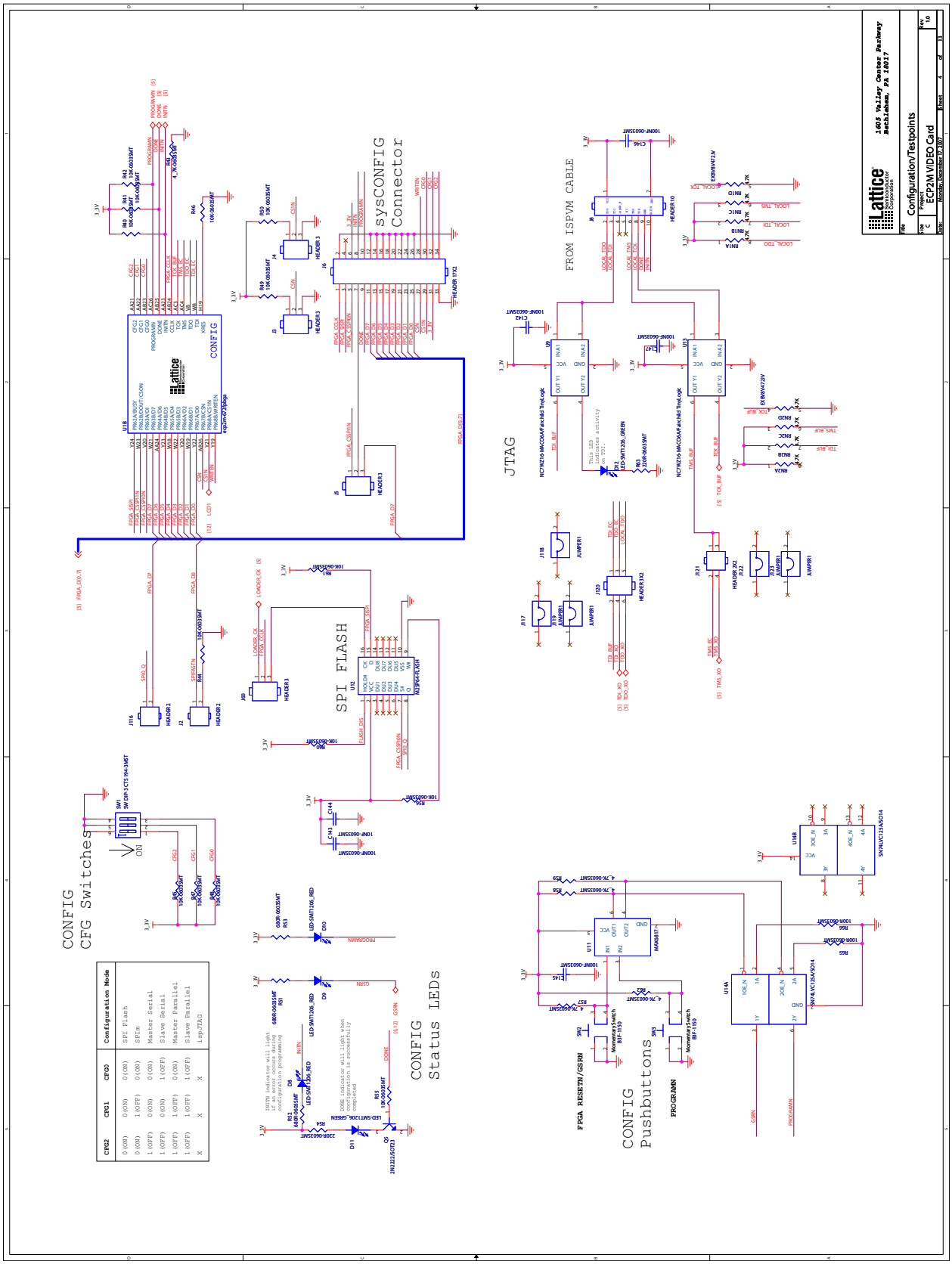


Figure 11. Configuration/Testpoints



CFG2	CFG1	CFG0	Configuration Mode
0 (ON)	0 (ON)	0 (ON)	SPI Flash
0 (ON)	1 (OFF)	0 (ON)	sPrm
1 (OFF)	0 (ON)	0 (ON)	Master Serial
1 (OFF)	0 (ON)	1 (OFF)	Slave Serial
1 (OFF)	1 (OFF)	0 (ON)	Master Parallel
1 (OFF)	1 (OFF)	1 (OFF)	Slave Parallel
X	X	X	Jtg-JTAG

Figure 12. Parallel FPGA Loader

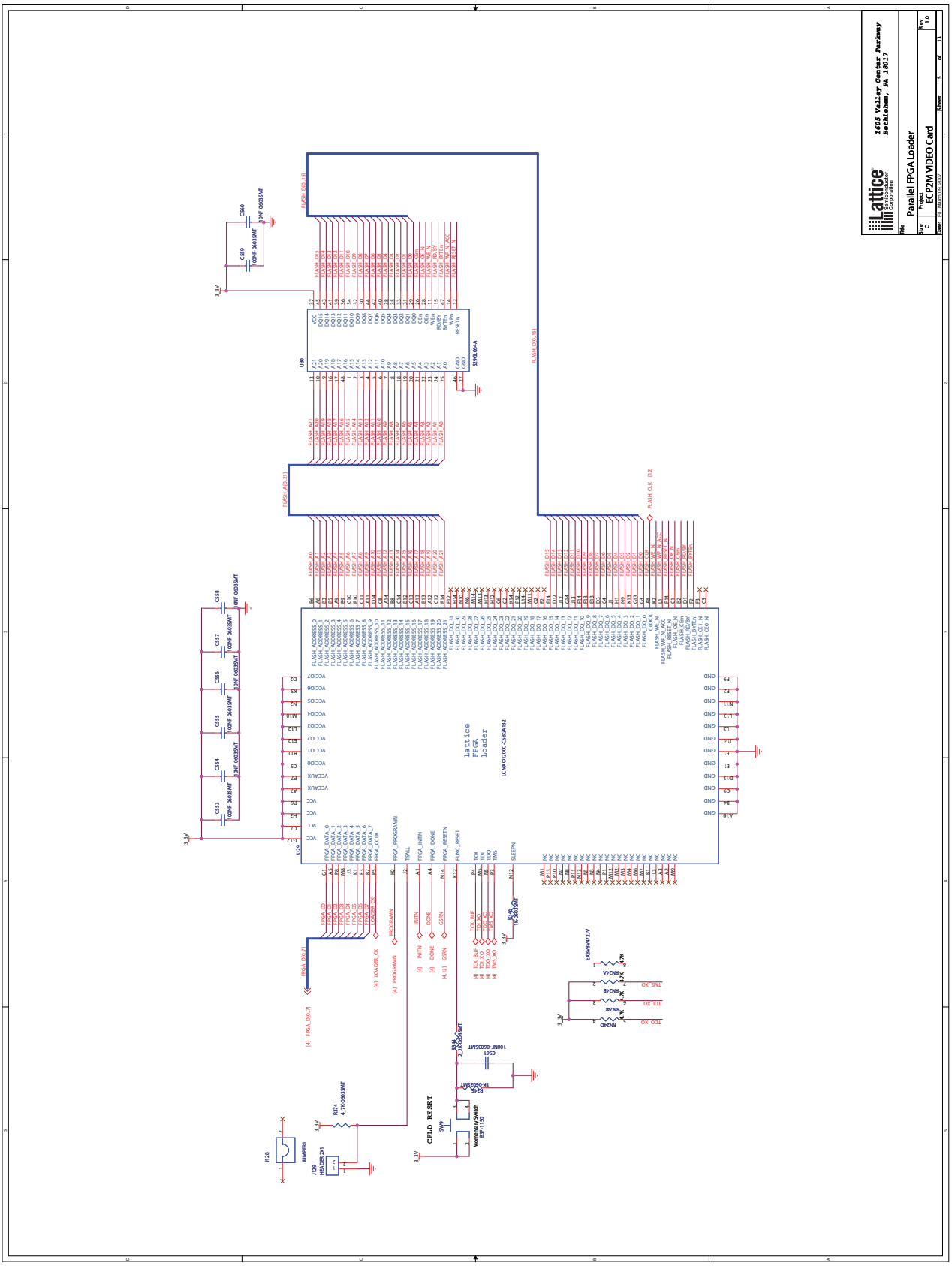


Figure 13. SERDES

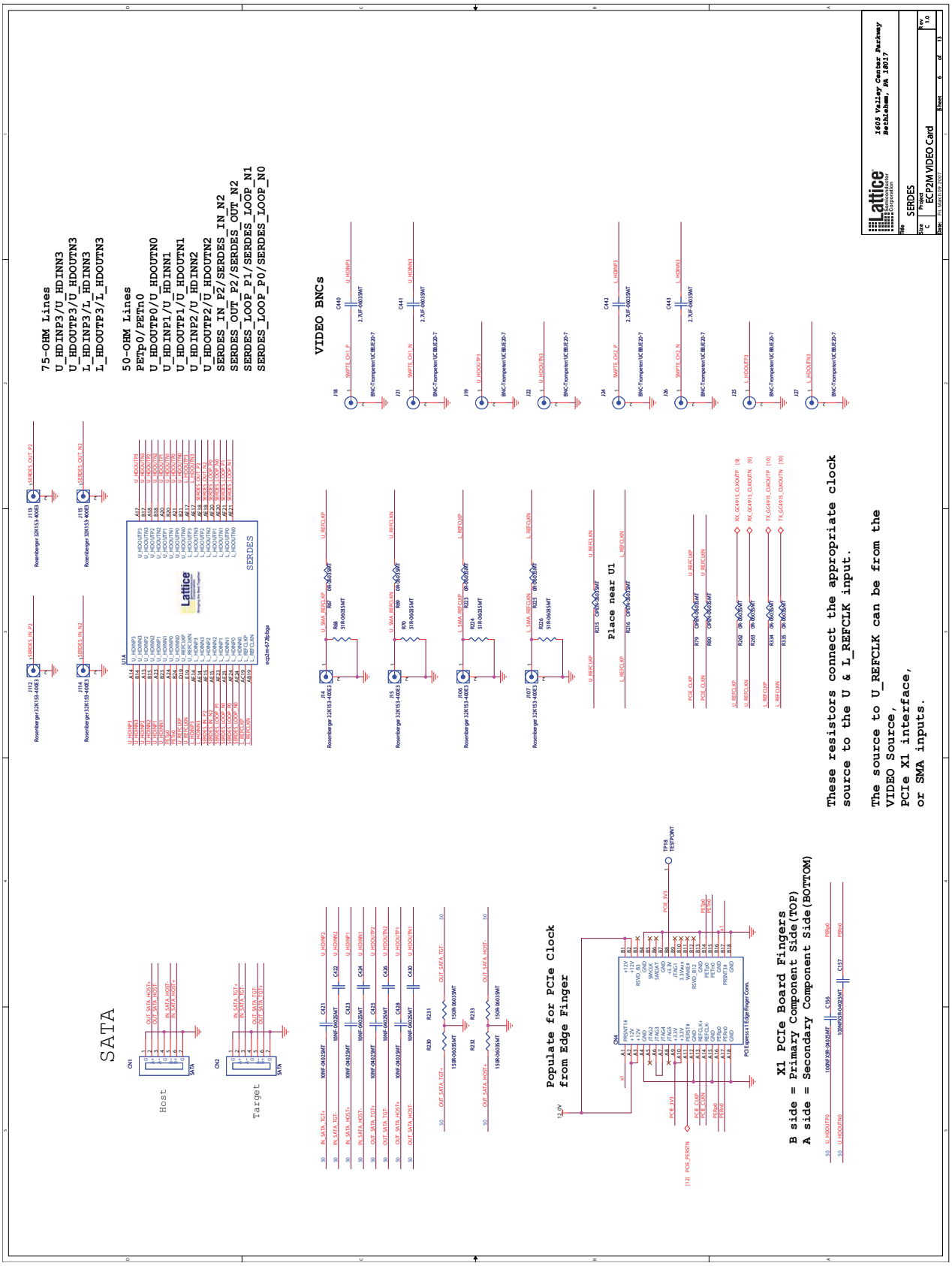


Figure 14. DDR2 FPGA Controller

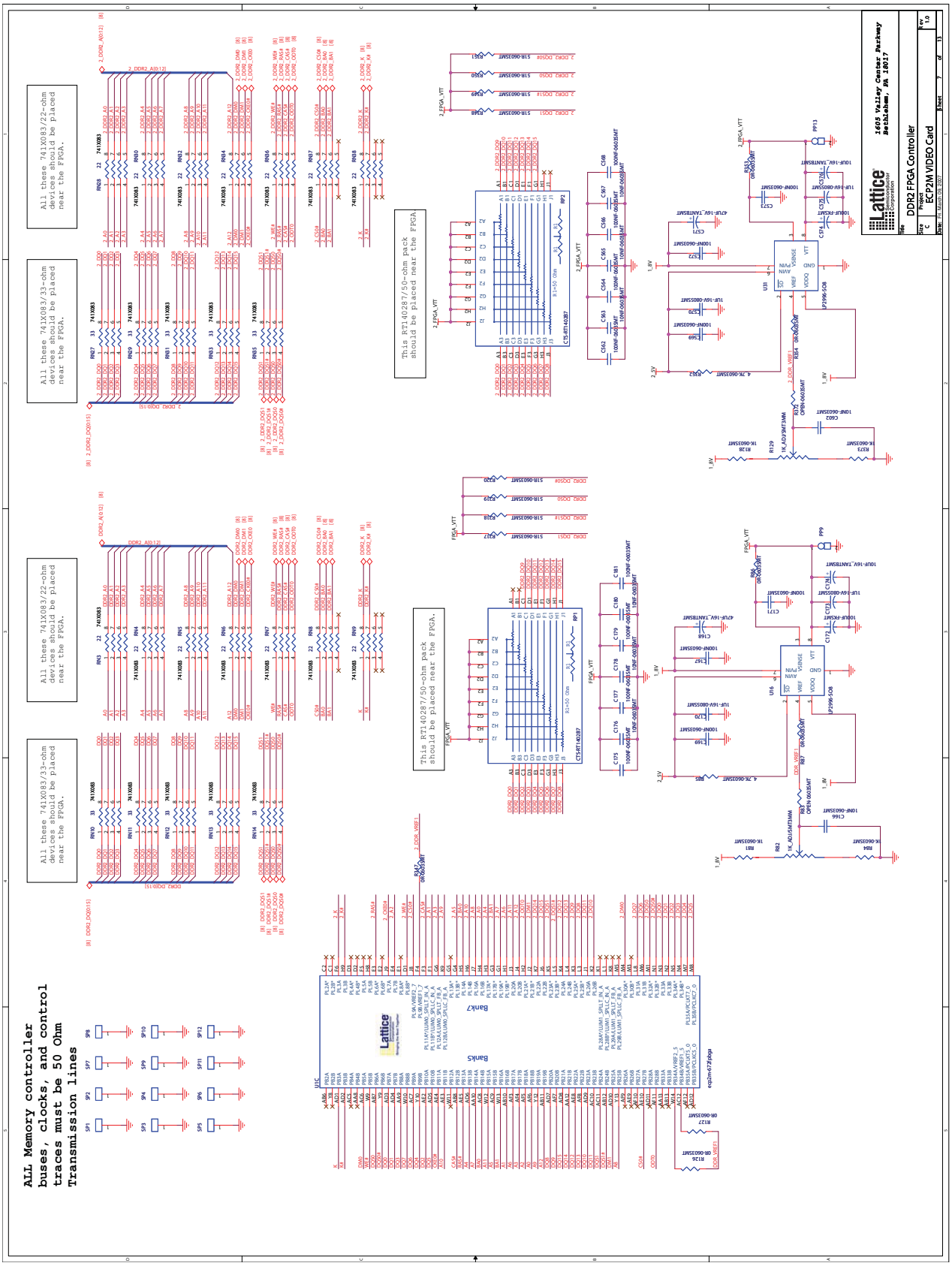


Figure 15. DDR2 Device/Termination

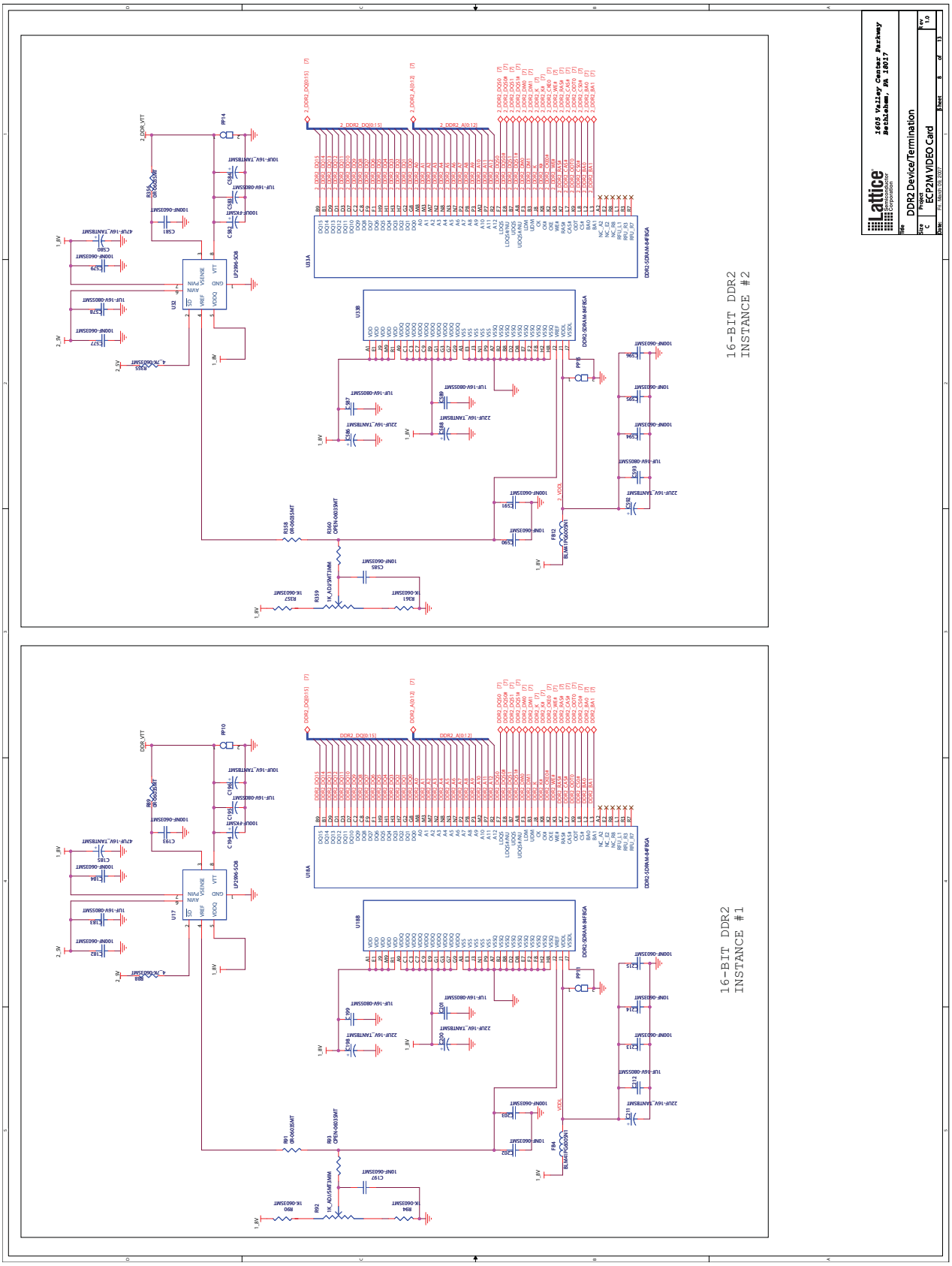


Figure 16. Tx Video Clocks

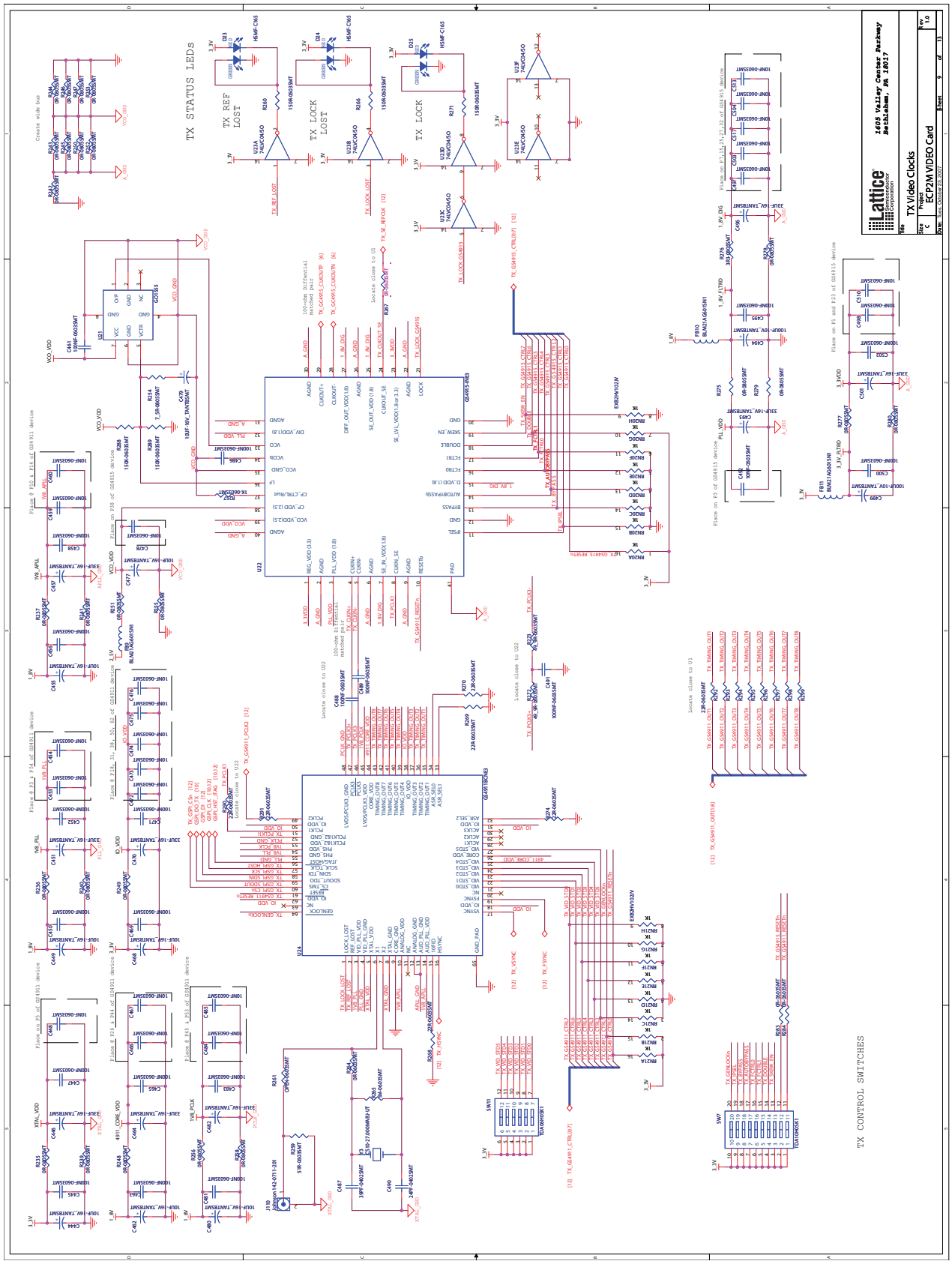


Figure 17. Rx Video Clocks

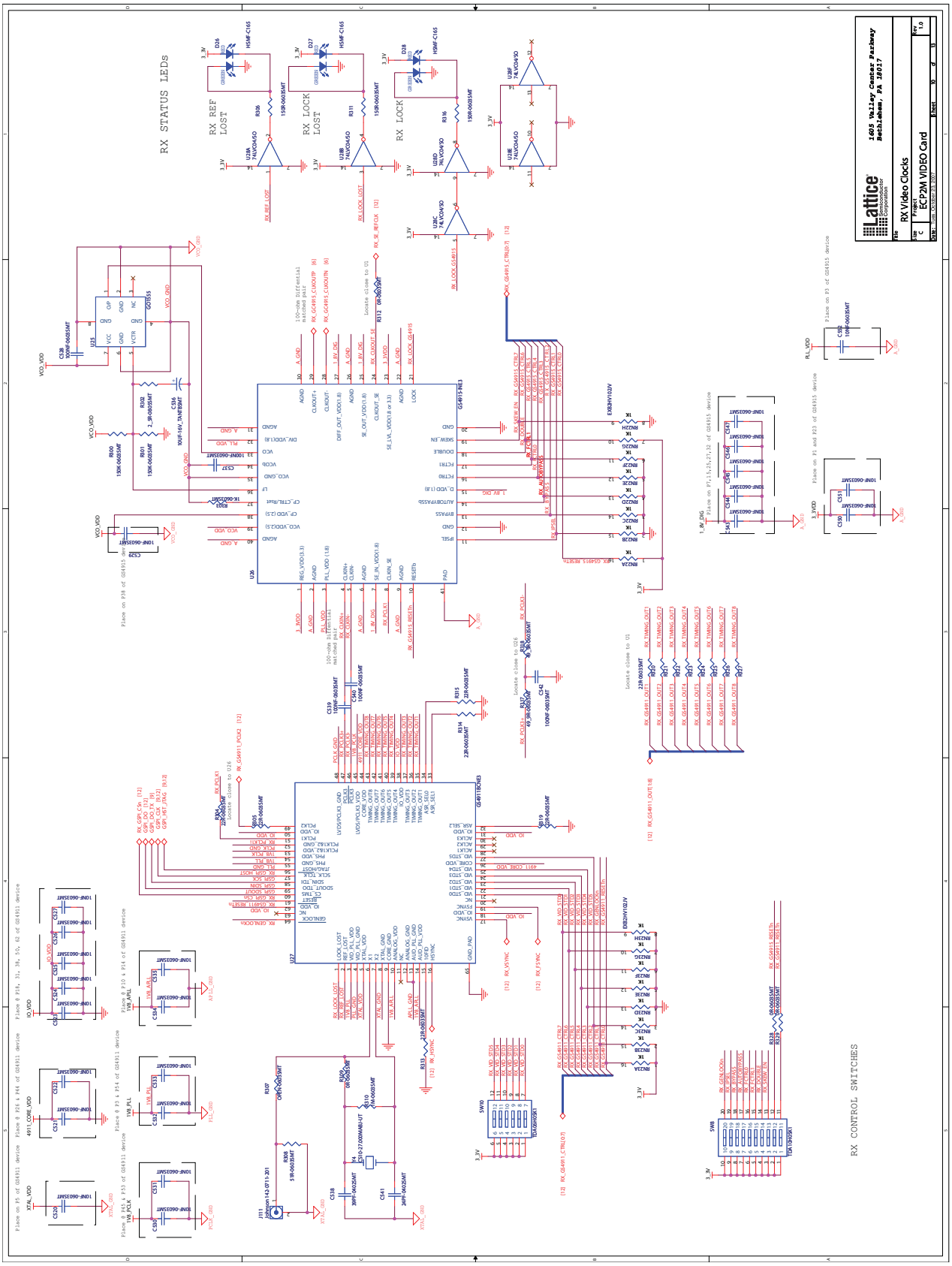


Figure 18. Differential I/O

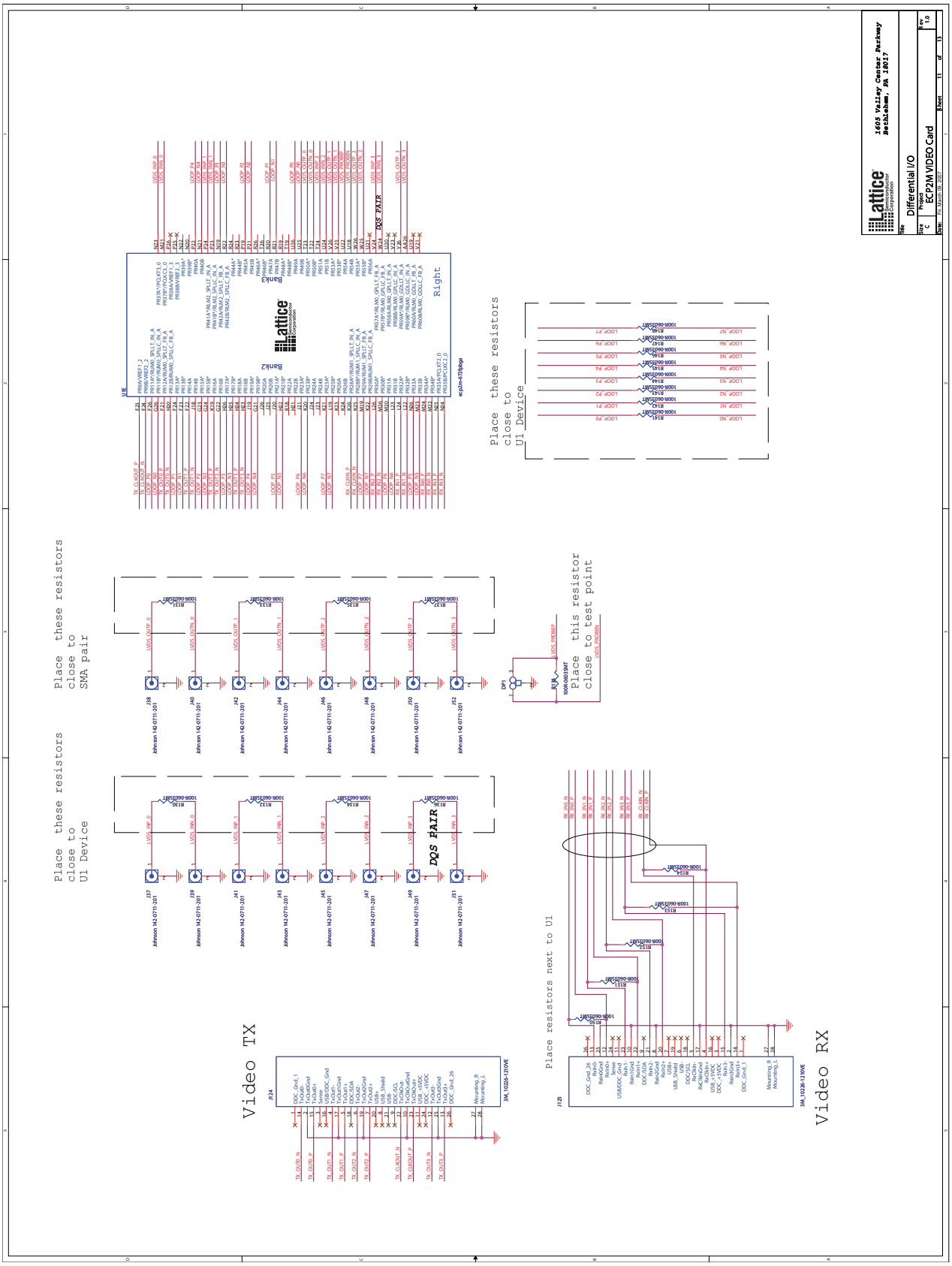


Figure 19. FPGA Test

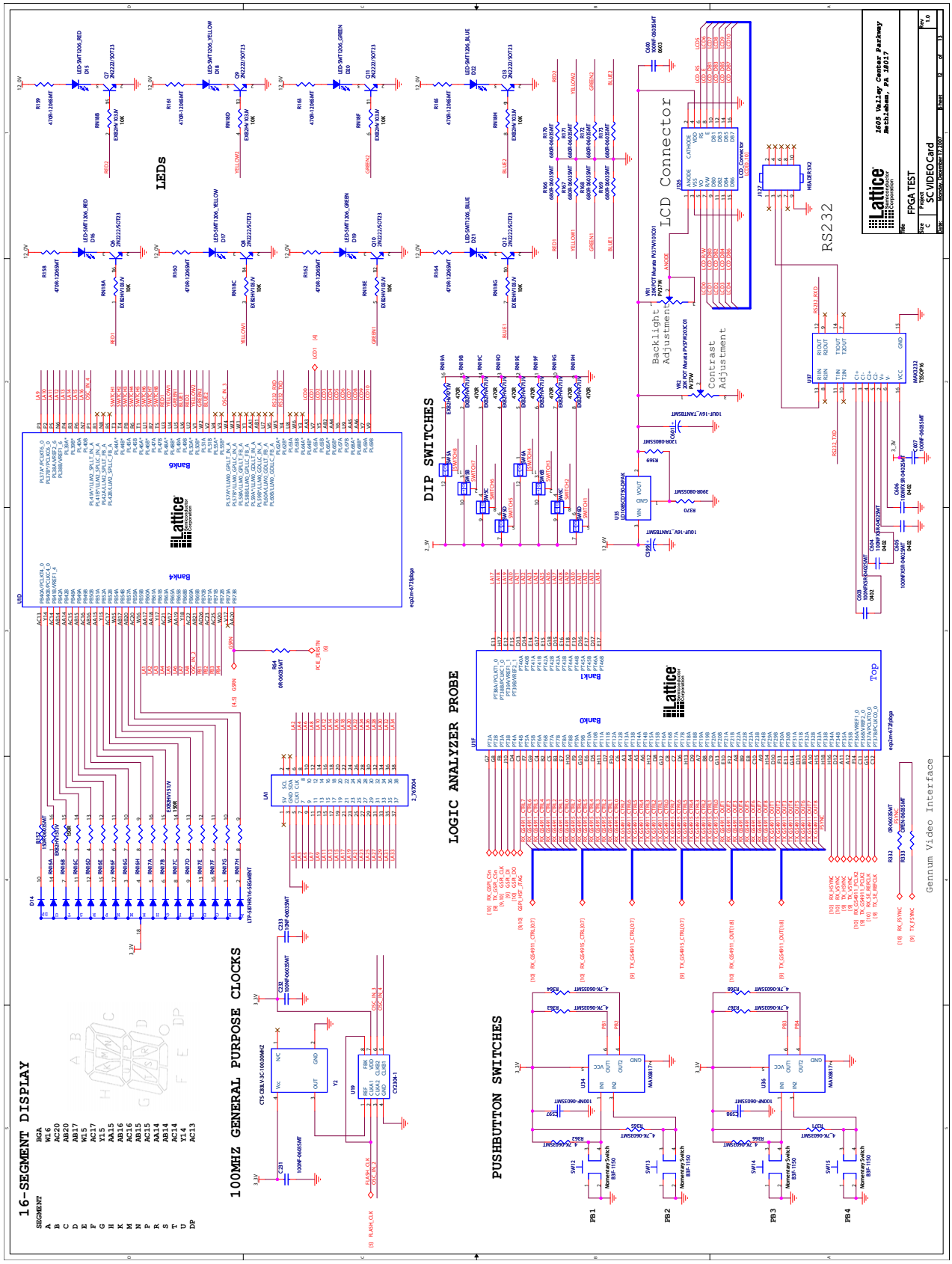


Figure 20. VSS/Decoupling