

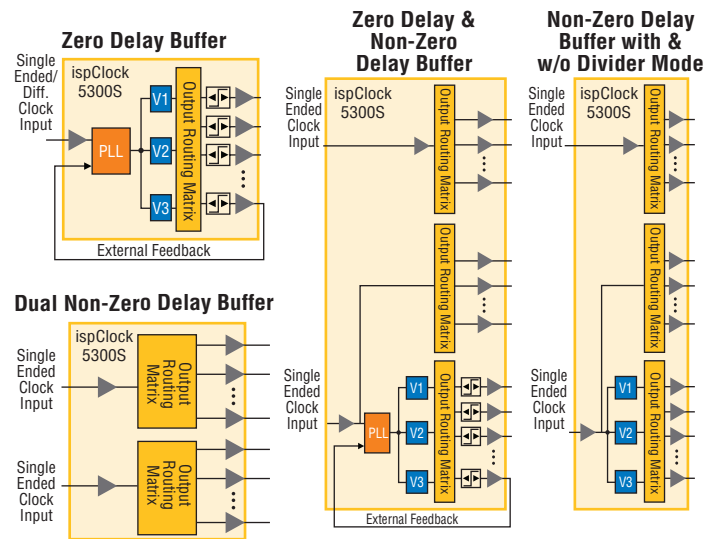
# ispClock5300S

## Integrates Zero Delay Buffers and Fan-out Buffers and Provides Multi-voltage Logic Interface

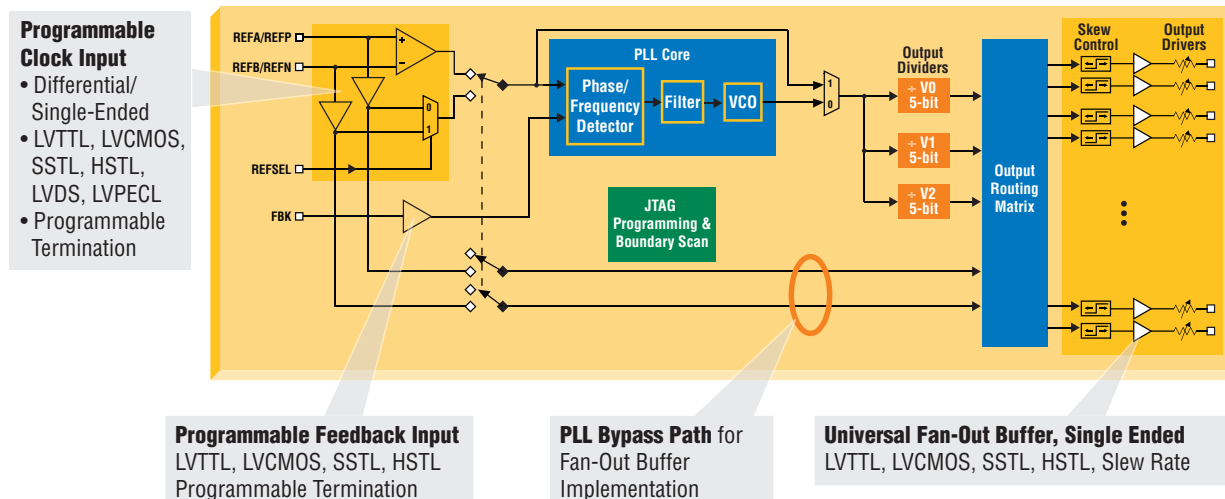
Imagine using a single, low-cost, programmable clock distribution device as a zero delay buffer (ZDB) or a non-zero delay fan-out buffer (FOB), or both, in the same package instead of selecting different clock ICs from multiple vendors! That is what you get with Lattice's revolutionary ispClock™5300S family.

The ispClock5300S architecture is built around a high performance PLL with programmable input, feedback, and output interface standards. Each output's skew can be individually and precisely controlled to compensate for differences in board trace lengths or timing requirements of the receiving devices. Additionally, each output can be individually configured for fan-out buffer or zero-delay buffer operation. The programmable output termination per output feature enables interfacing of the ispClock5300S device to any clock network with standard trace impedance.

### Four Modes of Operation



### ispClock5300S Block Diagram



## Key Features and Benefits

- **Each Output Programmable as FOB or ZDB from the Reference Clock**
  - Single chip replaces a variety of ZDB and FOB ICs
  - Single chip meets most clock distribution needs
- **Programmable Output Interface Standard**
  - Integrates logic translation buffers
  - Used across multiple clock networks
- **Precision Programmable Skew**
  - Minimizes serpentine traces to reduce circuit board area
  - Compensates for unforeseen changes to set-up and hold times
- **Programmable Output Termination**
  - Eliminates external termination resistors to reduce circuit board area
- **Programmable Single-ended or Differential Clock Reference Input**
  - Single chip replaces differential/single-ended input FOB and ZDB ICs
- **High Performance PLL**
  - Low jitter (<12ps)
  - Low skew (<100ps)
- **JTAG Programming and Boundary Scan**
  - Increases test coverage and reduces manufacturing time
- **Five Devices with 4, 8, 12, 16 or 20 Outputs**
  - Covers a wide clock distribution application range

## Design Made Simple with PAC-Designer Software

Lattice's PAC-Designer® software, a PC-based software tool, provides simple and intuitive pull-down menus for configuring all programmable features of the device. In addition, design utilities

like the Skew Editor, Frequency Calculator and Frequency Synthesizer enable easy configuration of various counters and other options. Configurations can be downloaded into ispClock devices from a PC parallel port.

**1. Set Reference and Feedback Clock Interface.**

**2. Set Output Clock Properties.**

**3. Set Input and Output Clock Frequencies.**

**4. Set Individual Clock Output Skews.**

**5. Download and Verify Design with Evaluation Board.**

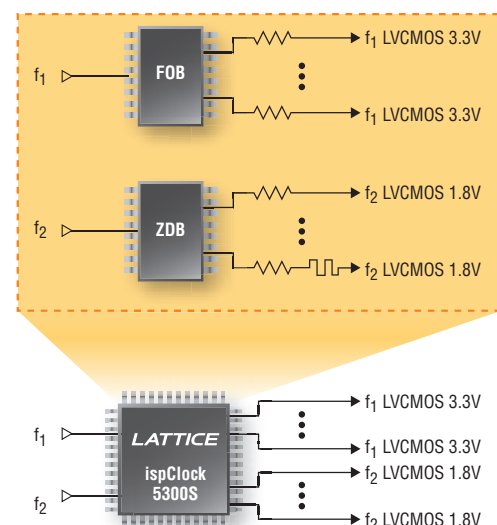
## ispClock5300S Attributes

| Feature                                          | ispClock5300S Device                                                           |       |         |       |       |
|--------------------------------------------------|--------------------------------------------------------------------------------|-------|---------|-------|-------|
|                                                  | 5304S                                                                          | 5308S | 5312S   | 5316S | 5320S |
| Outputs                                          | 4                                                                              | 8     | 12      | 16    | 20    |
| I/O Frequency Ranges                             | 8 to 267MHz (input), 5 to 267MHz (output)                                      |       |         |       |       |
| VCO Operation                                    | 160 to 400 MHz                                                                 |       |         |       |       |
| Spread Spectrum Compatibility                    | Yes                                                                            |       |         |       |       |
| Programmable Input Types                         | LVTTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential SSTL, Differential HSTL |       |         |       |       |
| Programmable Output and Feedback Interface Types | LVTTTL, LVCMOS, SSTL, HSTL                                                     |       |         |       |       |
| PLL Feedback                                     | External/Internal                                                              |       |         |       |       |
| Maximum Output Skew                              | 100ps                                                                          |       |         |       |       |
| Maximum Period Jitter (RMS)                      | 12ps                                                                           |       |         |       |       |
| Maximum Static Phase Offset                      | -40ps to 100ps                                                                 |       |         |       |       |
| Programmable Skew                                | 156ps to 5ns                                                                   |       |         |       |       |
| Programmable Termination                         | 40 to 70Ω & 20Ω Settings                                                       |       |         |       |       |
| Package                                          | 48 TQFP                                                                        |       | 64 TQFP |       |       |

## Application Diagram

The ispClock5300S is a PLD that can be used as a standard clock distribution IC across all designs.

- Integrates fan-out buffers, zero-delay buffers and termination resistors
- No trace snaking necessary
- Offers JTAG boundary scan feature



## Applications Support

1-800-LATTICE (528-8423)  
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